

GPS/Galileo/Glonass/QZSS receiver

Data brief



Features

- STMicroelectronics® 3rd generation positioning receiver with 32 Tracking channels and 2 fast acquisition channels compatible with GPS, Galileo and Glonass systems
- Embedded RF Front-End with separate GPS/Galileo/QZSS and Glonass IF outputs
- Embedded low noise amplifier
- -162 dBm indoor sensitivity (tracking mode)
- Fast TTFF <1 s in Hot start and 35s in Cold Start
- High performance ARM946 MCU (up to 208 MHz)
- 256 Kbyte embedded SRAM
- Real Time Clock (RTC) circuit
- 32-bit Watch-dog timer
- 2 UARTs
- 1 I²C master/slave interface
- 1 External SQI Flash interface
- USB2.0 dual-role full speed (12 MHz) with integrated physical layer transceiver
- 2 Controller Area Network (CAN)
- 3 channels ADC (10 bits)
- 3 Embedded 1.8 V voltage regulators
- I/O level selectable 1.8 V or 3.3 V
- Operating condition:
 - V_{DD12}: 1.2 V ±10%
 - V_{DD18/RF18}: 1.8 V ±5%
 - V_{LPVR}: 1.62 V to 3.6 V
 - V_{ddIO}: 1.8 V ±5%; 3.3 V ±10%

- Package:
 - VFQFPN56 (7x7x0.85 mm) 0.4 mm Pitch
- Ambient temperature range: -40/+85°C
- Aerospace and Defense features
 - Dedicated traceability and part marking
 - Production parts approval documents available
 - Adapted Extended life time and obsolescence management
 - Extended Product Change Notification process
 - Designed and manufactured to meet sub ppm quality goals
 - Advanced mold and frame designs for Superior resilience to harsh environment (acceleration, EMI, thermal, humidity)
 - Single Fabrication, Assembly and Test site
 - Dual internal production source capability

Application

- All types of resistive, inductive and capacitive loads in Aerospace and Defense applications.

Description

RSTA8088GA is a single die standalone positioning receiver IC working on multiple constellations (GPS/Galileo/Glonass/QZSS).

The device qualification includes a set of production flow methodology targeting zero defect per million.

RSTA8088GA, fulfilling high quality and service level market requirements, is the ideal solution for in-dash navigation and OEM telematic application.

The device is offered with a complete GNSS firmware which performs all GNSS operations including tracking, acquisition, navigation and data output.

Table 1. Device summary

| Package | Order codes | |
|----------|-------------|---------------|
| | Tube | Tape and reel |
| VFQFPN56 | RSTA8088GA | RSTA8088GATR |

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1 Overview

RSTA8088GA is a highly integrated System-On-Chip device designed for positioning systems applications.

It combines the high performance of ARM946 microprocessor with embedded enhanced peripherals and I/O capabilities with ST next generation triple-constellation positioning engine. The RF Front-End and Base Band processors are able to support GPS/Galileo and Glonass navigation systems. The device is offered with a complete firmware which performs all positioning operations including tracking, acquisition, navigation and data output with no need of external memories.

It also provides clock generation via PLL, backup logic with real time clock and it supports USB2.0 standard at full speed, (12 Mbps) with on-chip PHY.

RSTA8088GA is software compatible with the ARM processor family. The device is power supplied with 1.8 V and uses three on-chip voltage regulators to internally supply the RF front-End, core logic and the backup logic. In order to reduce the power consumption the chips can be directly powered with 1.2V bypassing the embedded voltage regulators which will be put in power down mode.

I/O lines are compatible with 1.8 V and 3.3 V.

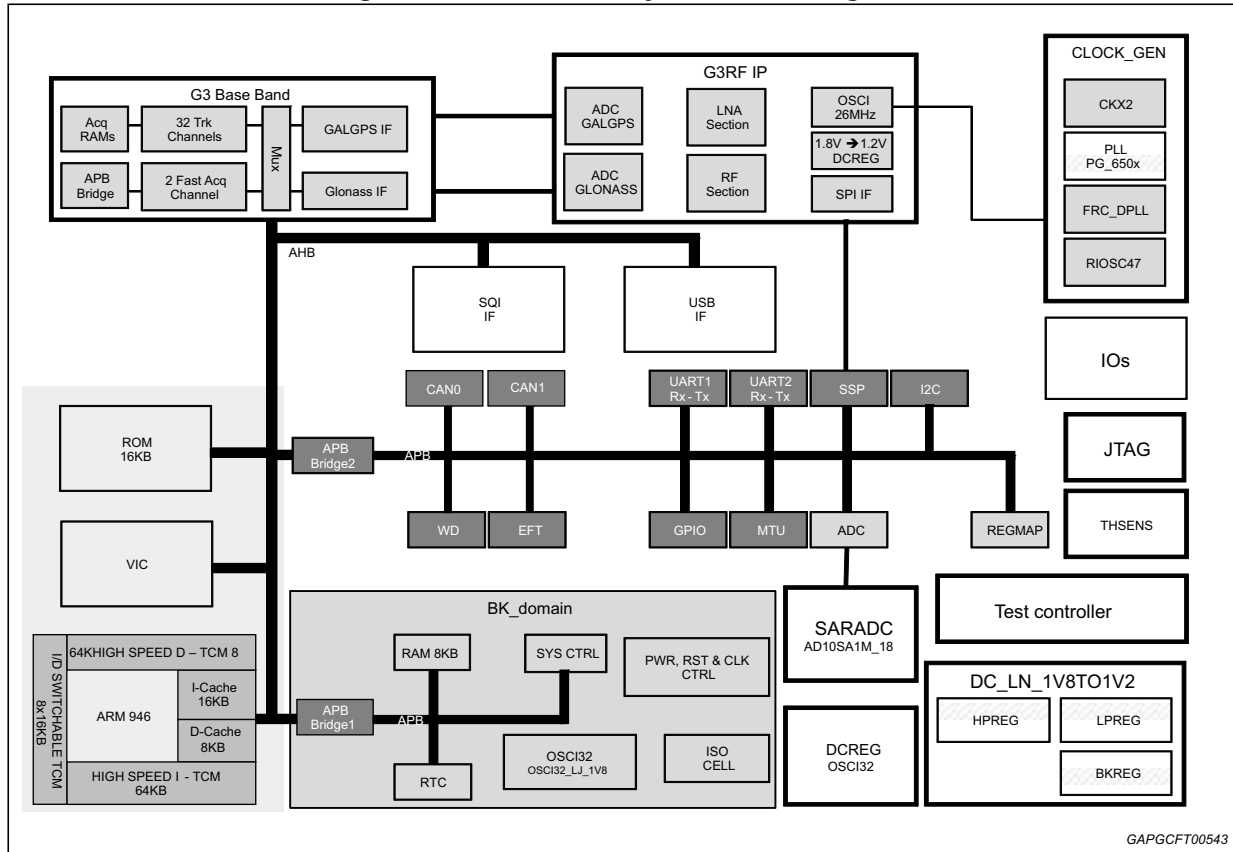
RSTA8088GA, using STMicroelectronics CMOSRF Technology, is housed in either VFQFPN56 (7 x 7 x 0.85 mm) or VFQFPN56 (8 x 8 x 0.85 mm) packages.

RSTA8088GA qualification includes a set of production flow methodology targeting zero defect per million.

2 Pin description

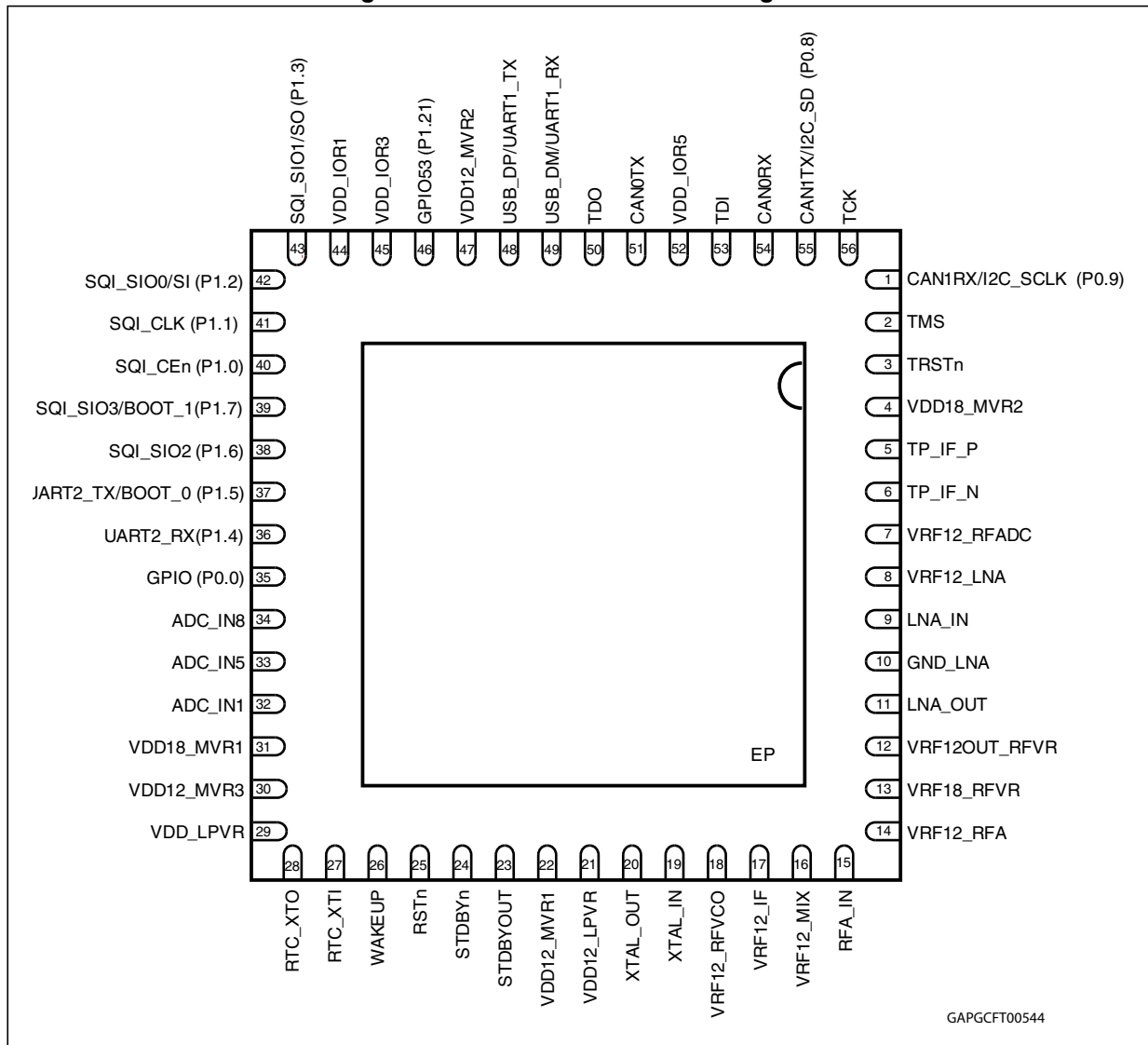
2.1 Block diagram

Figure 1. RSTA8088GA system block diagram



2.2 VFQFPN56 pin configuration

Figure 2. VFQFPN56 connection diagram



GAPGCFT00544

2.3 Power supply pins

Table 2. Power supply pins

| Symbol | I/O | Functions | VFQFN56 |
|------------------|-----|--|----------|
| VDD18_MVR[1,2] | Pwr | Digital supply voltage for main voltage regulator (1.8 V) | 31,4 |
| VDD12_MVR[1,2,3] | Pwr | Digital supply voltage for core circuitry (1.2 V). When using the MVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability. | 22,47,30 |
| VDD_LPVR | Pwr | Digital supply voltage for low power voltage regulator (1.62 - 3.6 V) | 29 |

Table 2. Power supply pins (continued)

| Symbol | I/O | Functions | VFQFN56 |
|---------------|-----|---|---------|
| VDD12_LPVR | Pwr | Digital supply voltage for backup logic (1.2 V). When using the LPVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability. | 21 |
| VDD_IOR1 | Pwr | Digital supply voltage for I/O ring 1 (1.8 or 3.3 V) | 44 |
| VDD_IOR3 | Pwr | Digital supply voltage for I/O ring 3 (1.8 V) | 45 |
| VDD_IOR5 | Pwr | Digital supply voltage for I/O ring 5 (3.3 V) | 52 |
| VRF18_RFVR | Pwr | Analog supply voltage for RF voltage regulator (1.8 V) | 13 |
| VRF12OUT_RFVR | Pwr | RF voltage regulator 1.2 V output | 12 |
| VRF12_LNA | Pwr | Analog supply voltage for LNA (1.2 V) | 8 |
| VRF12_RFA | Pwr | Analog supply voltage for RFA (1.2 V) | 14 |
| VRF12_MIX | Pwr | Analog supply voltage for Mixer (1.2 V) | 16 |
| VRF12_IF | Pwr | Analog supply voltage for IF (1.2 V) | 17 |
| VRF12_RFVCO | Pwr | Analog supply voltage for VCO (1.2 V) | 18 |
| VRF12_RFADC | Pwr | Analog supply voltage for RF ADC (1.2 V) | 7 |
| GND_LNA | GND | Analog supply ground for LNA | 10 |
| GND | GND | Analog and digital supply ground | EP |

2.4 Main function pins

Table 3. Main function pins

| Symbol | I/O voltage | I/O | Functions | VFQFPN56 |
|-----------------|-----------------------|-------|--|-----------|
| STDBYn | 1.2V | I | When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply | 24 |
| STDBYOUT | 1.2V | O | When low, indicates the chip is in Standby Mode. | 23 |
| RSTn | 1.2V | I | Reset Input with Schmitt-Trigger characteristics and noise filter. | 25 |
| WAKEUP | 1.2V | I | WAKEUP from STANDBY mode | 26 |
| RTC_XTI | 1.5V (Max) | I | Input of the 32 kHz oscillator amplifier circuit and input of the internal real time clock circuit. | 27 |
| RTC_XTO | 1.5V (Max) | O | Output of the oscillator amplifier circuit. | 28 |
| ADC_IN[1,5] | 1.4V – 0 Typ Range | I | ADC Analog input [1,5,8] | 32,33, 34 |
| USB_DP/UART1_TX | VDD_IOR5 | USB/O | USB D+ signal / UART1 Tx data | 48 |
| USB_DM/UART1_RX | VDD_IOR5 | USB/I | USB D- signal / UART1 Rx data | 49 |

Table 3. Main function pins (continued)

| Symbol | I/O voltage | I/O | Functions | VFQFPN56 |
|--------|-------------|-----|-----------------------------|----------|
| CAN0TX | VDD_IOR5 | O | CAN0 - transmit data output | 51 |
| CAN0RX | VDD_IOR5 | I | CAN0 - receive data input | 54 |

2.5 Test/emulated dedicated pins

Table 4. Test/emulated dedicated pins

| Symbol | I/O voltage | I/O | Functions | VFQFPN56 |
|---------|-------------|-----|------------------------------------|----------|
| TDO | VDD_IOR5 | O | JTAG test data out | 50 |
| TDI | VDD_IOR5 | I | JTAG test data in | 53 |
| TCK | VDD_IOR5 | I | JTAG test clock | 56 |
| TMS | VDD_IOR5 | I | JTAG test mode select | 2 |
| TRSTn | VDD_IOR5 | I | JTAG test circuit reset | 3 |
| TP_IF_P | VRF12_IF | O | Diff. test point for IF – positive | 5 |
| TP_IF_N | VRF12_IF | O | Diff. test point for IF – negative | 6 |

2.6 RF front-end pins

Table 5. RF front-end pins

| Symbol | I/O voltage | I/O | Functions | VFQFPN56 |
|----------|-------------|-----|--|----------|
| LNA_IN | VRF12_LNA | I | Low noise amplifier input | 9 |
| LNA_OUT | VRF12_LNA | O | Low noise amplifier output | 11 |
| RFA_IN | VRF12_RFA | I | RF amplifier input | 15 |
| XTAL_IN | VRF12_RFDig | I | Input side of crystal oscillator or TCXO input | 19 |
| XTAL_OUT | VRF12_RFDig | O | Output side of crystal oscillator | 20 |

2.7 Port 0 pins

Port 0 consists of a 32-bit bidirectional I/O port (only 3-bit are used in RSTA8088GA).

It can be either used as general purpose Input or Output port, or configured according to the associated alternate functions.

Table 6. Port 0 pins

| Symbol | I/O voltage | I/O | Mode | Functions | VFQFPN56 |
|--------|-------------|-----|---------|-----------------------------------|----------|
| P0.0 | VDD_IOR1 | I | Default | GPIO.0: General Purpose IO | 35 |
| | | I | A | PPS_IN: Pulse Per Second Input | |
| | | O | B | PPS_OUT: Pulse Per Second Output | |
| P0.8 | VDD_IOR5 | O | Default | CAN1TX: CAN1 Transmit Data Output | 55 |
| | | IO | A | GPIO.8: General Purpose IO | |
| | | IO | B | I2C_SD: I2C Serial Data | |
| P0.9 | VDD_IOR5 | I | Default | CAN1RX: CAN1 Receive Data Input | 1 |
| | | IO | A | GPIO.9: General Purpose IO | |
| | | O | B | I2C_SCLK: I2C Clock | |

2.8 Port 1 pins

Port 1 consists of a 32-bit bidirectional I/O port (only 9-bit are used in RSTA8088GA).

It can be either used as general purpose Input or Output port, or configured according to the associated alternate functions.

Table 7. Port 1 pins

| Symbol | I/O Voltage | I/O | Mode | Functions | VFQFPN56 |
|--------|-------------|-----|---------|--|----------|
| P1.0 | VDD_IOR1 | O | Default | SQI_CEN: SQI Flash chip enable | 40 |
| | | I/O | A | GPIO32: general purpose I/O | |
| | | I/O | B | SIGNGGPS: GGPS 3bit coding output (sign) | |
| P1.1 | VDD_IOR1 | O | Default | SQI_CLK: SQI Flash clock | 41 |
| | | I/O | A | GPIO33: general purpose I/O | |
| | | I/O | B | CLOCK_GGPS: GGPS clock out | |
| P1.2 | VDD_IOR1 | I/O | Default | SQI_SIO0/SI: SQI Flash data I/O 0 / ser. I | 42 |
| | | I/O | A | GPIO34: general purpose I/O | |
| | | I/O | B | SIGNGNS: GNS 3bit coding output (sign) | |
| P1.3 | VDD_IOR1 | I/O | Default | SQI_SIO1/SO: SQI Flash data I/O 1 / ser. O | 43 |
| | | I/O | A | GPIO35: general purpose I/O | |
| | | I/O | B | CLOCK_GNS: GNS clock out | |
| P1.4 | VDD_IOR1 | I | Default | UART2_RX: UART 2 Rx data | 36 |
| | | I/O | A | GPIO36: general purpose I/O | |
| P1.5 | VDD_IOR1 | I/O | Default | UART2_TX / BOOT_0: UART 2 Tx data / ARM Boot 0 | 37 |
| | | I/O | A | GPIO37: general purpose I/O | |



Table 7. Port 1 pins (continued)

| Symbol | I/O Voltage | I/O | Mode | Functions | VFQFPN56 |
|--------|-------------|-----|---------|---|----------|
| P1.6 | VDD_IOR1 | I/O | Default | SQI_SIO2: SQI Flash data I/O 2 | 38 |
| | | I/O | A | GPIO38: general purpose I/O | |
| P1.7 | VDD_IOR1 | I/O | Default | SQI_SIO3/BOOT_1: SQI Flash data I/O 3/ARMBoot 1 | 39 |
| | | I/O | A | GPIO39: general purpose I/O | |
| P1.21 | VDD_IOR3 | I/O | A | GPIO53: general purpose I/O | 46 |

3 Package and packing information

3.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

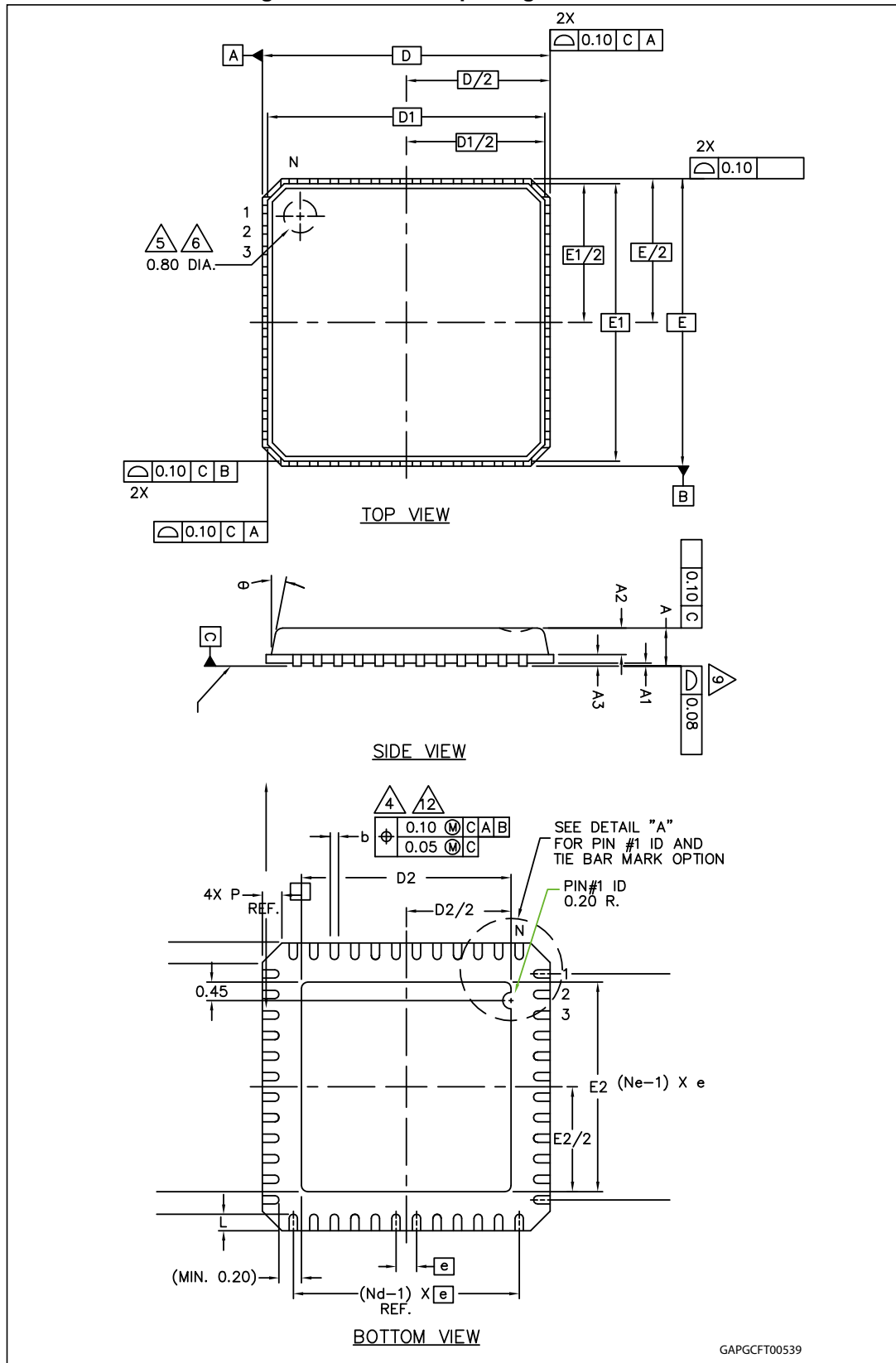
ECOPACK[®] is an ST trademark.

3.2 VFQFPN56 package information

Table 8. VFQFPN56 7 x 7 x 0.85 mm package dimensions

| Symbol | Min. | Typ. | Max |
|--------------------------|----------|------|------|
| Common dimensions | | | |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0 | 0.01 | 0.05 |
| A2 | 0.60 | 0.65 | 0.70 |
| A3 | 0.20 REF | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 7.00 BSC | | |
| D1 | 6.75 BSC | | |
| D2 | 5.0 | 5.1 | 5.2 |
| E | 7.00 BSC | | |
| E1 | 6.75 BSC | | |
| E2 | 5.0 | 5.1 | 5.2 |
| e | 0.40 BSC | | |
| θ | 0° | | 12° |
| L | 0.30 | 0.40 | 0.50 |
| N | 56 | | |
| Nd | 14 | | |
| Ne | 14 | | |
| P | 0.24 | 0.42 | 0.60 |

Figure 3. VFQFPN56 package dimension



4 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 16-Sep-2014 | 1 | Initial release. |

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