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DATA SHEET
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Current-Shunt Monitors, 40 V Common Mode, Unidirectional, Single, Dual, Quad

NCS21673, NCV21673, NCS21674, NCV21674, NCS21675, NCV21675

The NCS21673, NCS21674, and NCS21675 are a series of current sense amplifiers offered in gains of 20, 50, 100, and 200 V/V. These parts can measure voltage across shunts at common mode voltages from −0.1 V to 40 V, independent of supply voltage. This helps measuring of fast transients and allows the same type of part to be used for high side and low side current sensing. These devices can operate from a single 2.7 V to 5.5 V power supply. With a −3 dB BW of up to 350 kHz and a Slew Rate of 2 V/μs typical , the fast detection of current changes is ensured. These parts are available in SOT23−5, Micro8, and TSSOP−14 packages. The multichannel versions (dual and quad) make current sensing in multiple points of a system both space and cost effective.

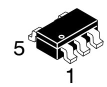
Features

- Wide Common Mode Input Range: −0.1 V to 40 V
- Supply Voltage Range: 2.7 V to 5.5 V
- Low Offset Voltage: ±100 μV
- Low Offset Drift: ±1 μV/°C max
- Low Gain Error: ±1% max
- Low Current Consumption: 300 μA max per channel
- NCV Prefix for Automotive Grade 1 and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

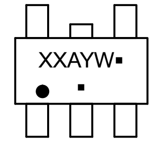
Applications

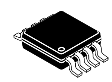
- High−Side Current Sensing
- Low−Side Current Sensing
- Power Management
- Automotive

MARKING DIAGRAMS

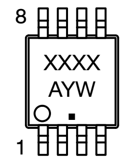


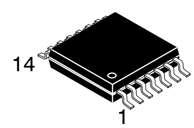
TSOP−5
CASE 483



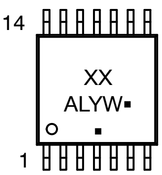


Micro8
CASE 846A−02





TSSOP−14 WB
CASE 948G



XX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

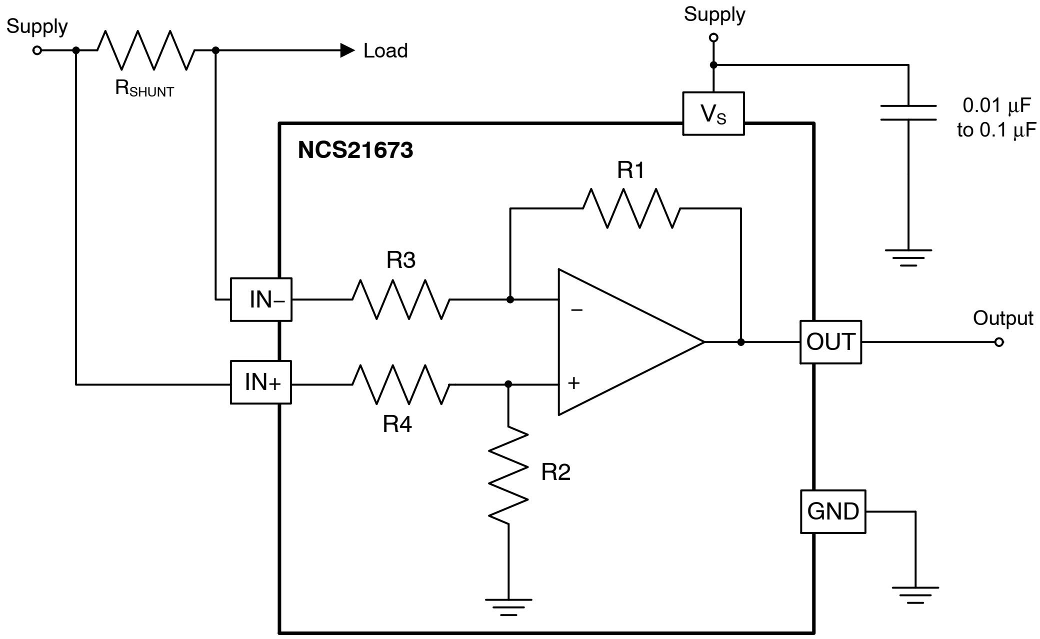
(Note: Microdot may be in either location)

PIN CONNECTIONS

See pin connections on page 2 of this data sheet.

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.



$V_{OUT} = (I_{LOAD} \times R_{SHUNT}) * GAIN$

Figure 1. Example Application Schematic of High−Side Current Sensing

PIN CONNECTIONS

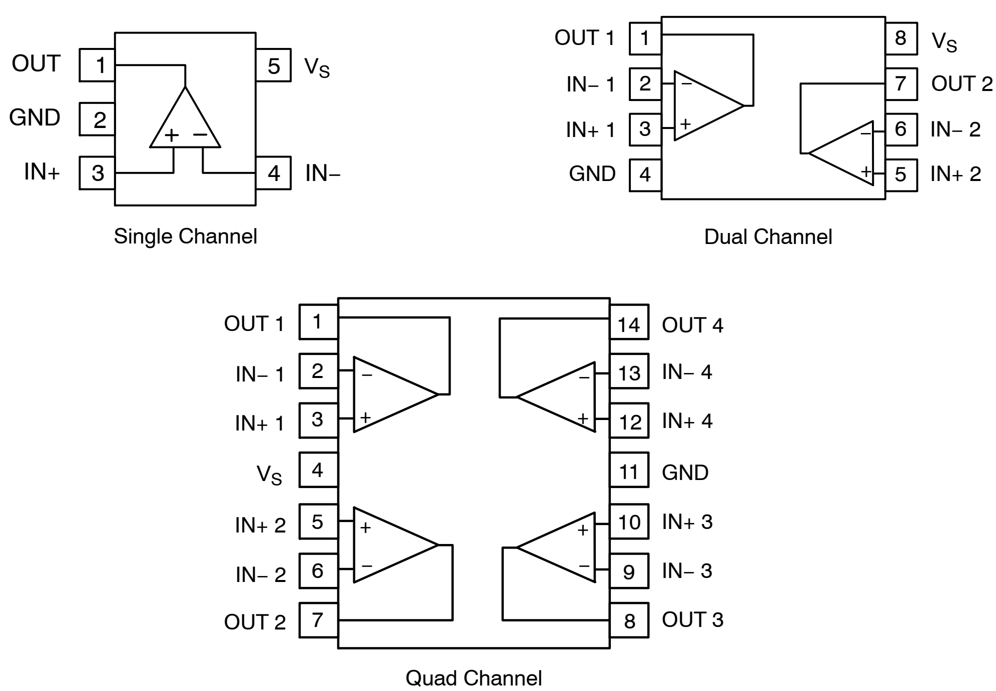


Figure 2. Pin Connections

ORDERING INFORMATION

Device	Channels	Package	Gain	OPN	Marking	Shipping
Industrial and Consumer						
NCS21673	Single	TSOP−5	20	NCS21673SN2G020T1G**	TBD	Tape and Reel 3000/reel
			50	NCS21673SN2G050T1G**	TBD	
			100	NCS21673SN2G100T1G**	TBD	
			200	NCS21673SN2G200T1G**	TBD	
NCS21674	Dual	Micro8	20	NCS21674DMG020R2G**	G020	Tape and Reel 4000/reel
			50	NCS21674DMG050R2G**	G050	
			100	NCS21674DMG100R2G**	G100	
			200	NCS21674DMG200R2G	G200	
NCS21675	Quad	TSSOP−14	20	NCS21675DTBG020R2G**	TBD	Tape and Reel 2500/reel
			50	NCS21675DTBG050R2G**	TBD	
			100	NCS21675DTBG100R2G**	TBD	
			200	NCS21675DTBG200R2G**	TBD	
Automotive Qualified						
NCV21673*	Single	TSOP−5	20	NCV21673SN2G020T1G**	TBD	Tape and Reel 3000/reel
			50	NCV21673SN2G050T1G**	TBD	
			100	NCV21673SN2G100T1G**	TBD	
			200	NCV21673SN2G200T1G**	TBD	
NCV21674*	Dual	Micro8	20	NCV21674DMG020R2G**	G020	Tape and Reel 4000/reel
			50	NCV21674DMG050R2G**	G050	
			100	NCV21674DMG100R2G**	G100	
			200	NCV21674DMG200R2G**	G200	
NCV21675*	Quad	TSSOP−14	20	NCV21675DTBG020R2G**	TBD	Tape and Reel 2500/reel
			50	NCV21675DTBG050R2G**	TBD	
			100	NCV21675DTBG100R2G**	TBD	
			200	NCV21675DTBG200R2G**	TBD	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
**In Development

MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply Voltage (Note 1)		V_S	−0.3 to 5.5	V
Analog Inputs	Differential (V_{IN+})−($V_{IN−}$) (Note 2)	V_{IN+}, $V_{IN−}$	±42	V
	Common−Mode (Note 2)		−0.3 to +42	
Output (Note 2)		V_{OUT}	GND−0.3 to (V_s) +0.3	V
Input Current into Any Pin (Note 2)		I_{IN}	±10	mA
Maximum Junction Temperature		$T_{J(max)}$	+150	°C
Storage Temperature Range		T_{STG}	−65 to +150	°C
ESD Capability, Human Body Model (Note 3)		HBM	±2000	V
Charged Device Model (Note 3)		CDM	±1000	V
Latch−up Current (Note 4)			±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for safe operating parameters
2. Input voltage at any pin may exceed the voltage shown if current at that pin is limited to ±10 mA
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard JS−001−2017
   ESD Charged Device Model tested per JEDEC standard JS−002−2014
4. Latch−up Current tested per JEDEC standard: JESD78E

THERMAL CHARACTERISTICS

Parameter	Symbol	Package	Value	Unit
Thermal Resistance, Junction−to−Air (Notes 5, 6)	θ_{JA}	TSOP−5 / SOT23−5	210	°C/W
		Micro8 / MSOP−8	195	
		TSSOP−14	TBD	

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for safe operating parameters
6. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Conditions	Min	Max	Unit
Ambient Temperature	T_A	NCS prefix	−40	125	°C
		NCV prefix	−40	150*	
Common Mode Input Voltage	V_{CM}	Ta = −40°C to +125°C	−0.1	40	V
Supply Voltage	V_S	Ta = −40°C to +125°C	2.7	5.5	V
		Ta = 0°C to +85°C	1.8	5.5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

*During operation at Ta = 150°C, also the limitation for junction temperature (Tj(max) = 150°C) has to be considered.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_{SENSE} = (V_{IN+}) – ($V_{IN–}$).; V_S = 5 V, V_{IN+} = 12 V, unless otherwise noted. **Boldface** limits apply over the specified temperature range, T_A = –40°C to 125°C unless otherwise noted, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input							
Common Mode Rejection Ratio	CMRR	V_{IN+} = –0.1 V to 40 V, V_{SENSE} = 0 mV	G = 20	84	100		dB
				84			
			G = 50	84	100		
				84			
			G = 100	84	100		
				84			
			G = 200	84	100		
				84			
Input Offset Voltage	V_{OS}	T_A = 25°C, V_{IN+} = 12 V	G = 20		±100	±500	μV
			G = 50		±100	±500	
			G = 100		±100	±500	
			G = 200		±100	±500	
		T_A = 25°C, V_{IN+} = 0 V	G = 20		±25	TBD	
			G = 50		±25	TBD	
			G = 100		±25	TBD	
			G = 200		±25	±210	
Input Offset Voltage Drift vs. Temperature	dV_{OS}/dT	T_A = –40°C to +125°C			0.2	1	μV/°C
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V, V_{SENSE} = 10 mV			±8	**±40**	μV/V
Input Bias Current	I_{IB}	V_{IN+} = 0 V			1		μA
		V_{IN+} = 12 V			100		
Input Offset Current	I_{IO}	V_{IN+} = 12 V, V_{SENSE} = 10 mV			15		μA
Output							
Gain	G	G = 20			20		V/V
		G = 50			50		
		G = 100			100		
		G = 200			200		
Gain Error		T_A = 25°C			±0.1		%
		T_A = –40°C to +125°C				**±1**	
Gain Error vs Temperature		T_A = –40°C to +125°C			1.5	**20**	ppm/°C
Nonlinearity Error					±0.01		%
Maximum Capacitive Load	C_L	No sustained oscillation			1		nF
Settling Time to 1%					5		μs
Voltage Output							
Output Voltage High, Swing from V_S Supply Rail	$V_S – V_{OH}$	R_L = 10 kΩ to GND, T_A = 25°C			0.02		V
		R_L = 10 kΩ to GND, T_A = –40°C to 125°C				**0.03**	
Output Voltage Low, Swing from GND	V_{OL} – GND	R_L = 10 kΩ to GND, T_A = 25°C			0.0005		V
		R_L = 10 kΩ to GND, T_A = –40°C to 125°C				**0.005**	

ELECTRICAL CHARACTERISTICS (continued)
At T_A = +25°C, V_{SENSE} = (V_{IN+}) – ($V_{IN–}$).; V_S = 5 V, V_{IN+} = 12 V, unless otherwise noted. **Boldface** limits apply over the specified temperature range, T_A = –40°C to 125°C unless otherwise noted, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Frequency Response							
Bandwidth (f_{-3dB})	BW	C_L = 25 pF	G = 20		350		kHz
			G = 50		210		
			G = 100		150		
			G = 200		105		
Slew Rate	SR				2		V/µs
Noise							
Voltage Noise Density	e_n	G = 50 or higher			40		nV/√Hz
		G = 20			TBD		
Power Supply							
Quiescent Current per Channel	I_Q	T_A = 25°C			195	260	µA
		T_A = –40°C to +125°C				**300**	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS (T_A = 25°C, VS = 5 V, and VIN+ = 12 V unless otherwise noted)

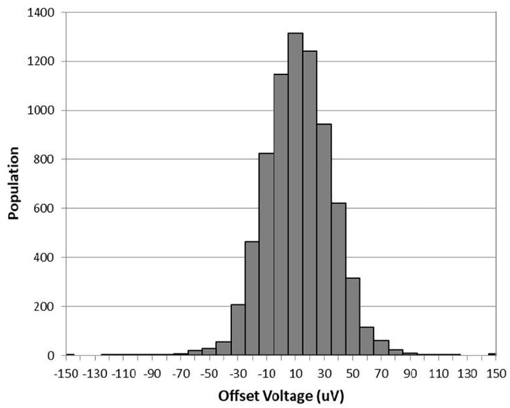


Figure 3. Input Offset Production Distribution G200

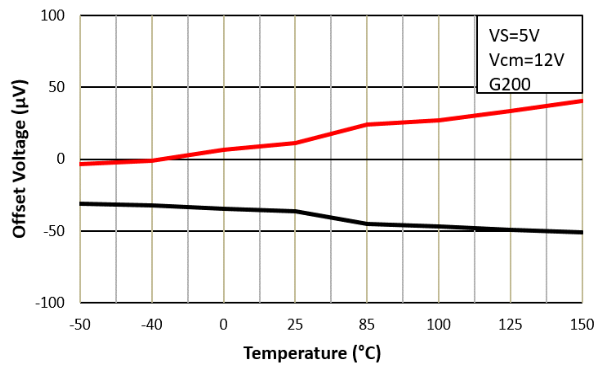


Figure 4. Offset Voltage vs. Temperature

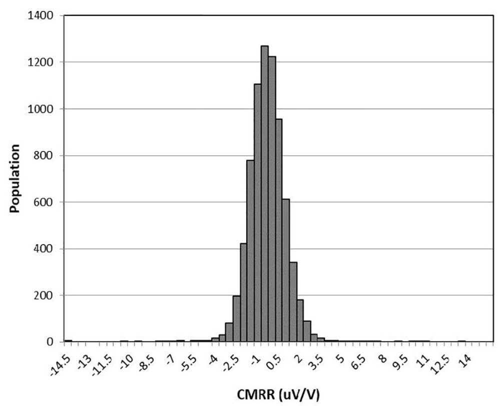


Figure 5. CMRR Production Distribution G200

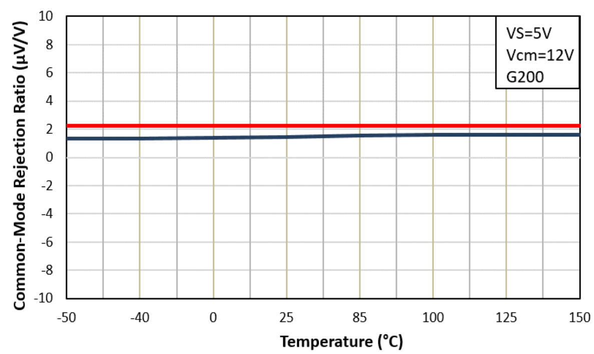


Figure 6. CMRR vs. Temperature

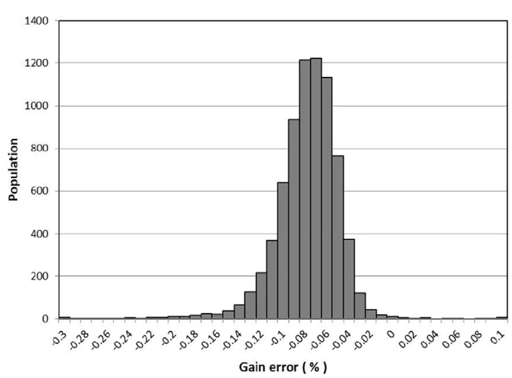


Figure 7. Gain Error Production Distribution G200

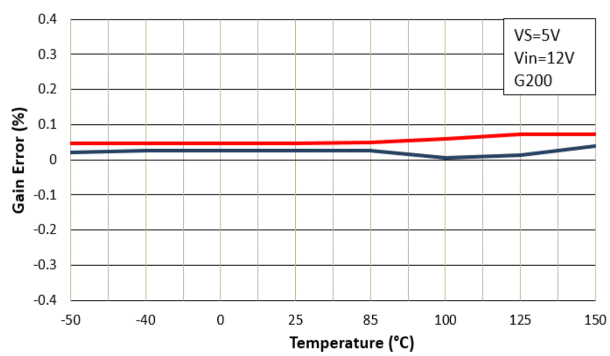


Figure 8. Gain Error vs. Temperature

TYPICAL CHARACTERISTICS (T_A = 25°C, VS = 5 V, and VIN+ = 12 V unless otherwise noted) (continued)

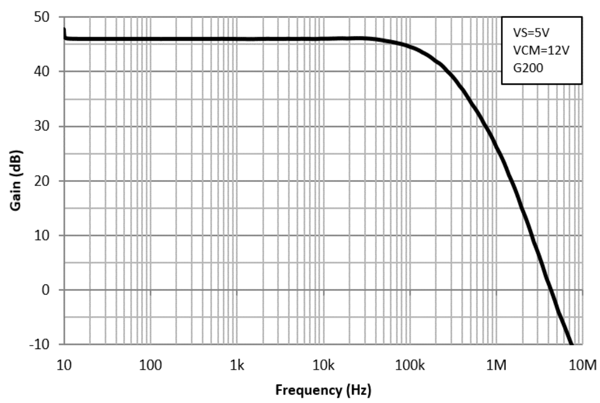


Figure 9. Gain vs. Frequency

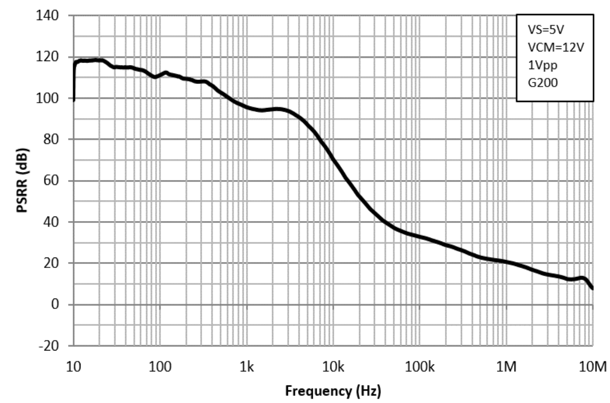


Figure 10. Power Supply Rejection Ration vs. Frequency

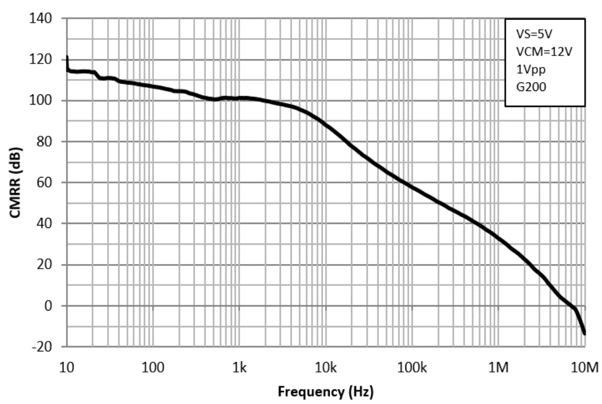


Figure 11. Common Mode Rejection Ratio vs. Frequency

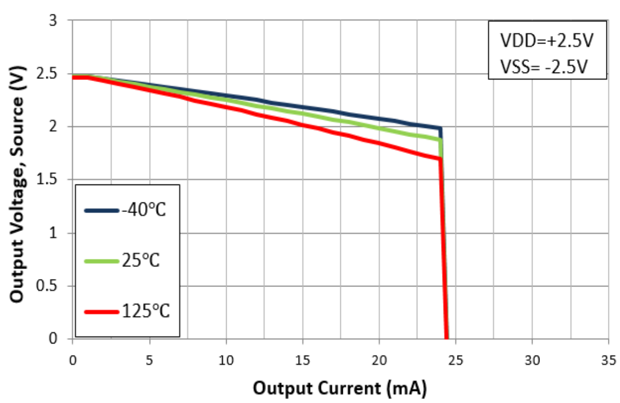


Figure 12. Output High Swing vs. Output Current

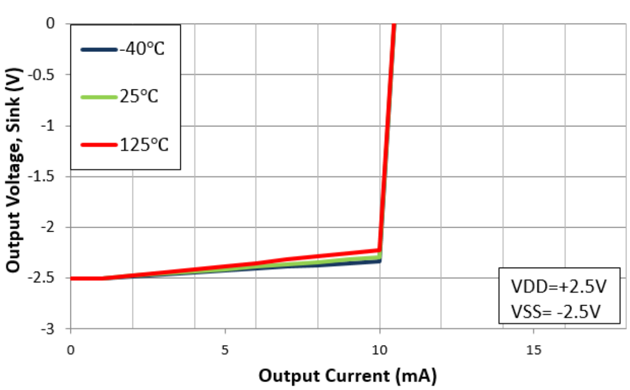


Figure 13. Output Low Swing vs. Output Current

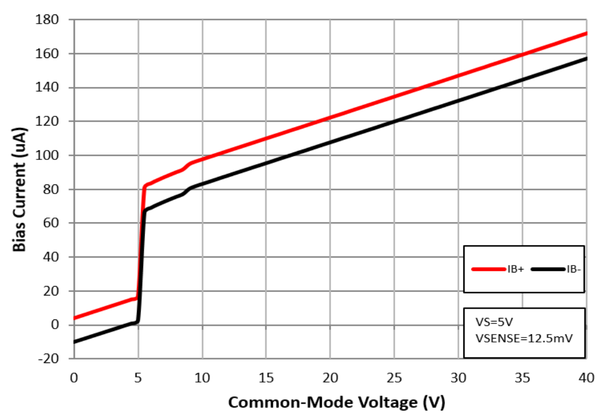


Figure 14. Input Bias Current vs. Common−Mode Voltage

TYPICAL CHARACTERISTICS (T_A = 25°C, VS = 5 V, and VIN+ = 12 V unless otherwise noted) (continued)

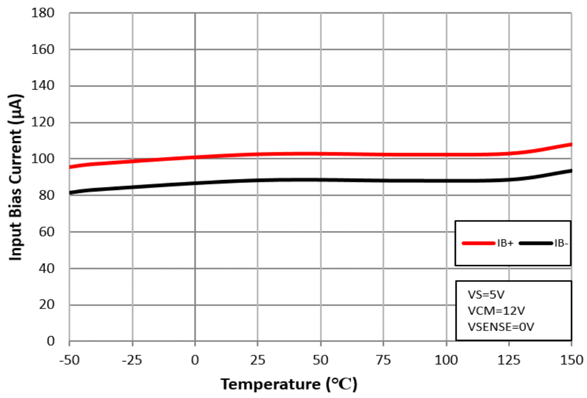


Figure 15. Input Bias Current vs. Temperature

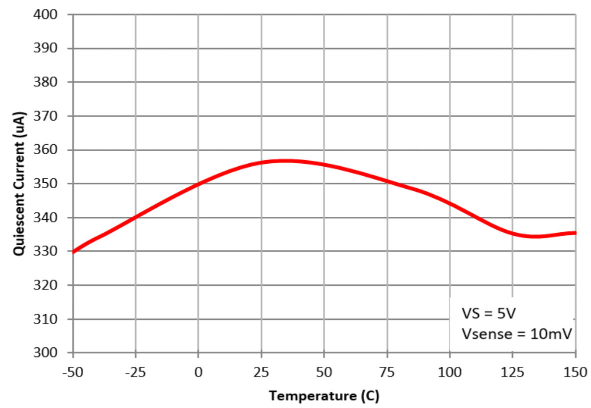


Figure 16. Quiescent Current vs. Temperature

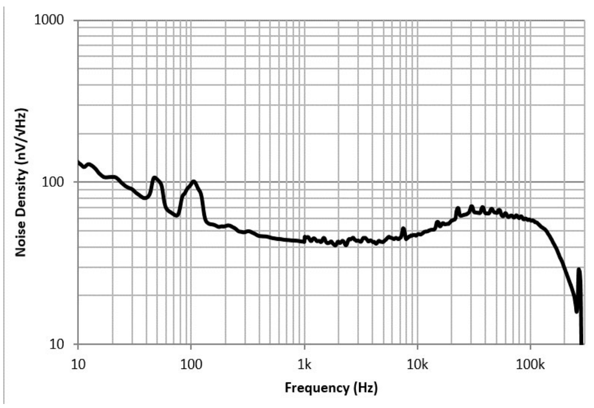


Figure 17. Input−Referred Voltage Noise vs. Frequency

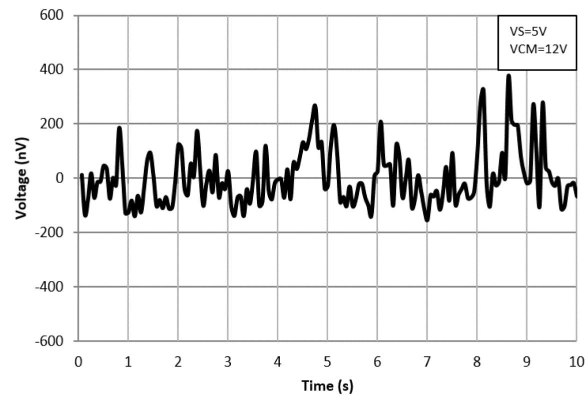


Figure 18. 0.1−Hz to 10−Hz Voltage Noise (Referred−to−Input)

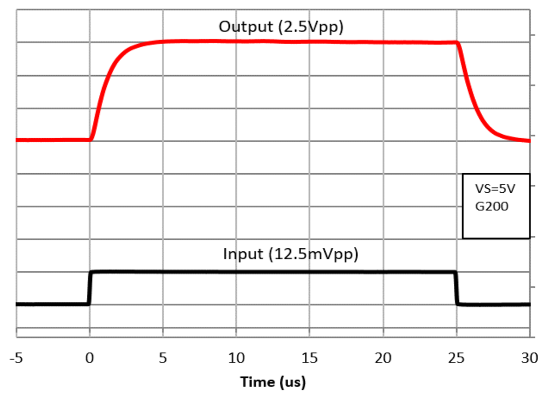


Figure 19. Input Signal Step response

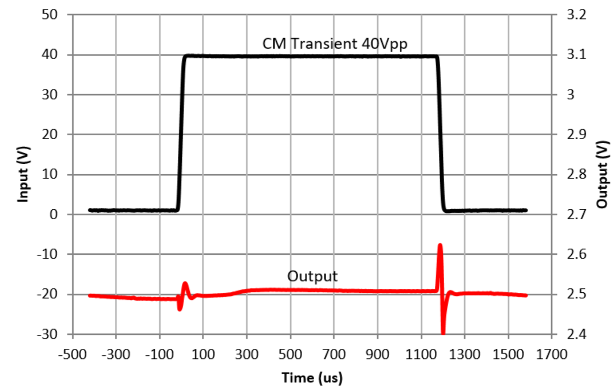


Figure 20. Common−Mode Voltage Transient Response

TYPICAL CHARACTERISTICS (T_A = 25°C, VS = 5 V, and VIN+ = 12 V unless otherwise noted) (continued)

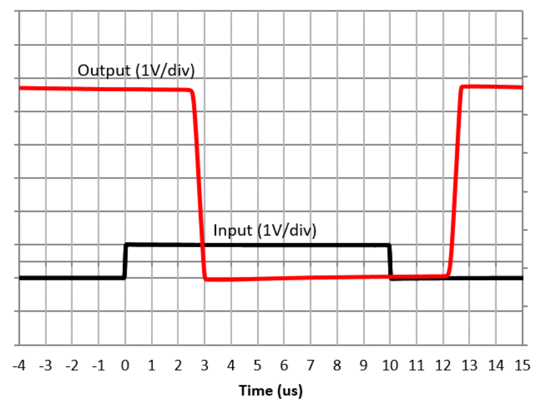


Figure 21. Inverting Differential Input Overload

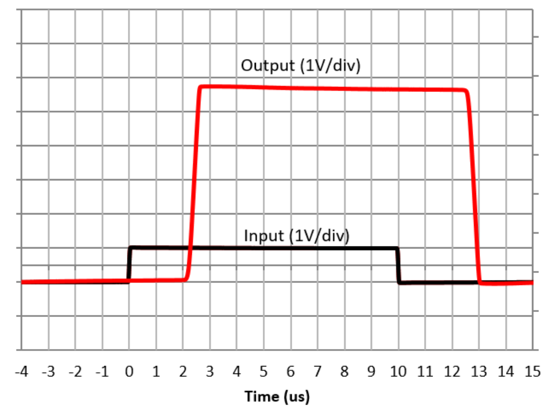


Figure 22. Noninverting Differential Input Overload

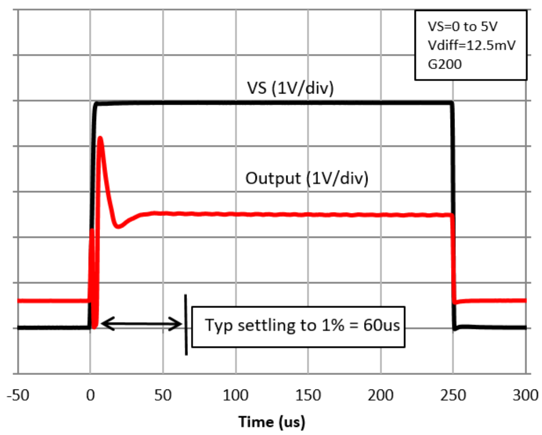


Figure 23. Start−Up Response

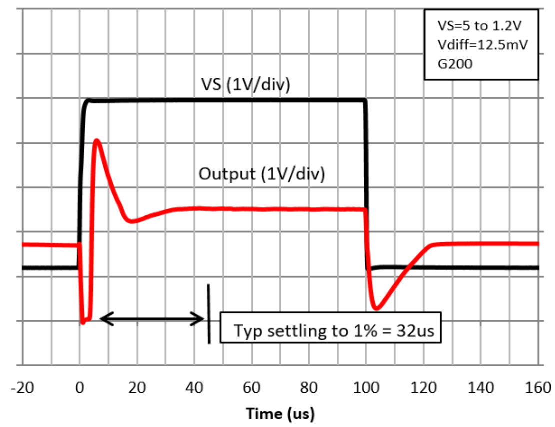


Figure 24. Brownout Recovery

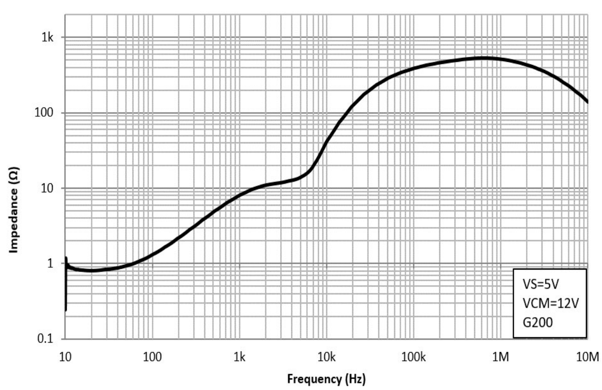


Figure 25. Output Impedance vs. Frequency

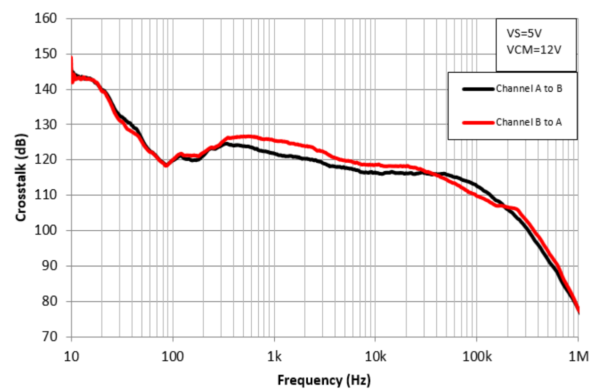


Figure 26. Channel Separation vs. Frequency

TYPICAL CHARACTERISTICS (T_A = 25°C, VS = 5 V, and VIN+ = 12 V unless otherwise noted) (continued)

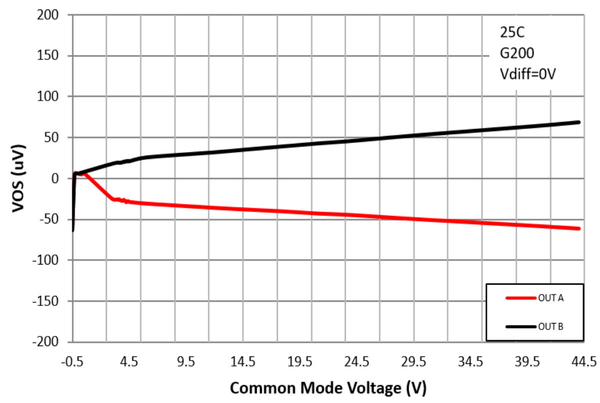


Figure 27. Output Voltage vs. Common−Mode Voltage

APPLICATION INFORMATION

Current Sensing Techniques

NCS(V)21673, NCS(V)21674, and NCS(V)21675 are current sense amplifiers featuring a wide common mode voltage range that spans from −0.1 V to 40 V independent of the supply voltage. These amplifiers can be configured for low−side and high−side current sensing.

Unidirectional Operation

These current sense amplifiers monitor unidirectional current flow. In unidirectional current sensing, the measured load current always flows in the same direction. Common applications for unidirectional operation include power supplies and load current monitoring. In this configuration, the IN+ pin should be connected to the high side of the sense resistor, while the IN− pin should be connected to the low side of the sense resistor.

Input Filtering

As shunt resistors decrease in value, shunt inductance can significantly affect frequency response. At values below 1 mΩ, the shunt inductance causes a zero in the transfer function that often results in corner frequencies in the low 100's of kHz. This inductance increases the amplitude of high frequency spike transient events on the current sensing line that can overload the front end of any shunt current sensing IC. This problem must be solved by the external filtering at the input of the amplifier. Note that all current sensing IC's are vulnerable to this problem, regardless of manufacturer claims. Filtering is required at the input of the device to resolve this problem, even if the spike frequencies are above the rated −3 dB bandwidth of the device.

Ideally, select the capacitor to exactly match the time constant of the shunt resistor and its inductance; alternatively, select the capacitor to provide a pole below that point. Make the input filter time constant equal to or larger than the shunt and its inductance time constant:

$$\frac{L_{SHUNT}}{R_{SHUNT}} \le R_{FILT}C_{FILT}$$

While this time constant can be the product of any R_{FILT} and C_{FILT} values, the designer needs to take into account that the R_{FILT} resistors are connected in series with the internal feedback resistors R3 and R4, hence changing the amplifier's overall gain. Also, the opamp's input currents (IIB) create a voltage drop across the filtering resistors, which is added to the differential voltage seen by the opamp's inputs and modifies the output value. A good practice is to keep the filtering resistors in the range of a few ohms then size the filtering capacitor accordingly.

Selecting the Shunt Resistor

The desired accuracy of the current measurement determines the precision, shunt size, and the resistor value. The larger the resistor value, the more accurate the measurement possible, but a large resistor value also results in greater current loss.

For the most accurate measurements, use four−terminal current sense resistors. They provide two terminals for the current path in the application circuit, and a second pair for the voltage detection path of the sense amplifier. This technique is also known as *Kelvin Sensing*. This insures that the voltage measured by the sense amplifier is the actual voltage across the resistor and does not include the small resistance of a combined connection. When using non−Kelvin shunts, follow manufacturer recommendations on how to lay out the sensing traces closely.

Gain Options

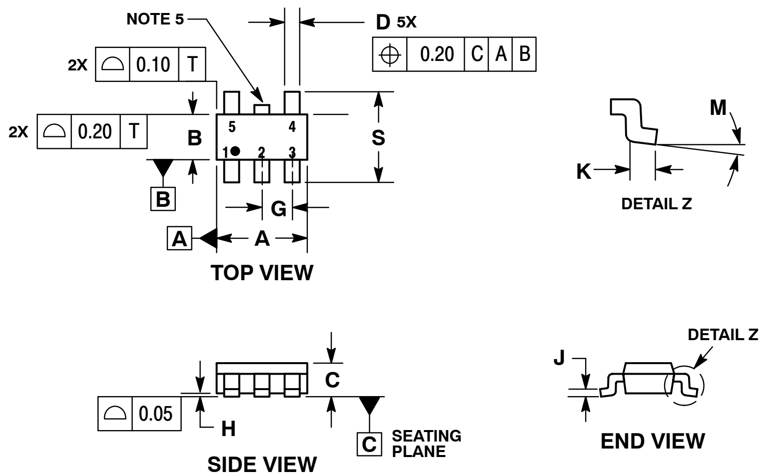
The gain is set by integrated, precision, ratio−matched resistors. These current sense amplifiers are available in gain options of 20 V/V, 50 V/V, 100 V/V, and 200 V/V. Adding external resistors to adjust the gain can contribute to the overall system error and is not recommended for multiple reasons. First, the series resistors mismatch increase the overall gain error and temperature coefficient, and lower the CMRR. Second, the IIB flowing through the external resistors change the differential voltage seen by the opamp's input. Last but not least, while the internal resistors are well matched in terms of ratio, they have a high tolerance in their absolute value so the resulting gain value may not match the expectations.

Shutdown

While the NCS21673/4/5 series do not include a shutdown feature, a simple MOSFET, power switch, or logic gate can be used to switch off power and eliminate quiescent current. Note that the input pins connected to the shunt resistor will always have a current flow via the input and feedback resistors (total resistance of each leg always is approx. 400 kΩ). Also note that when powered, the shunt input pins will exhibit the specified and well−matched bias current. The shunt input pins support the rated common mode voltage even when the power is not applied.

PACKAGE DIMENSIONS

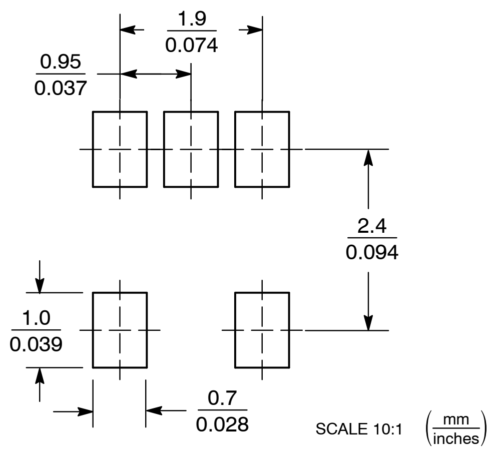
TSOP−5
CASE 483
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

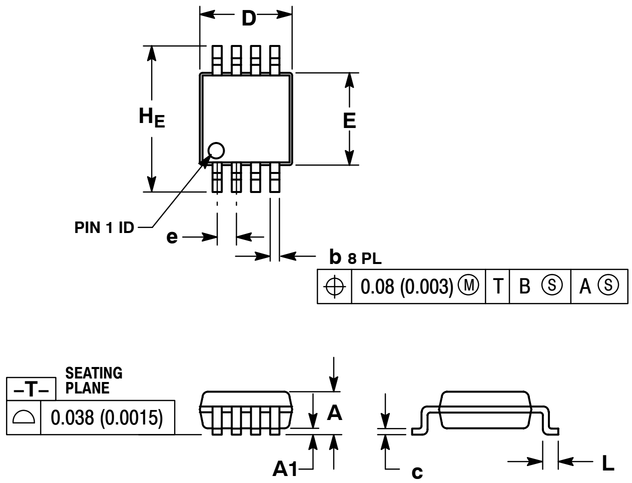
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

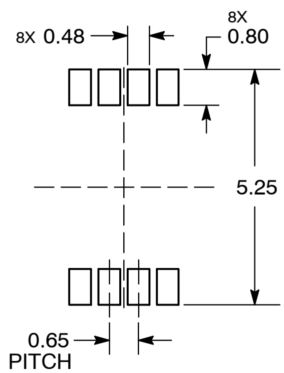
Micro8™
CASE 846A−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65 BSC			0.026 BSC	
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

RECOMMENDED SOLDERING FOOTPRINT*

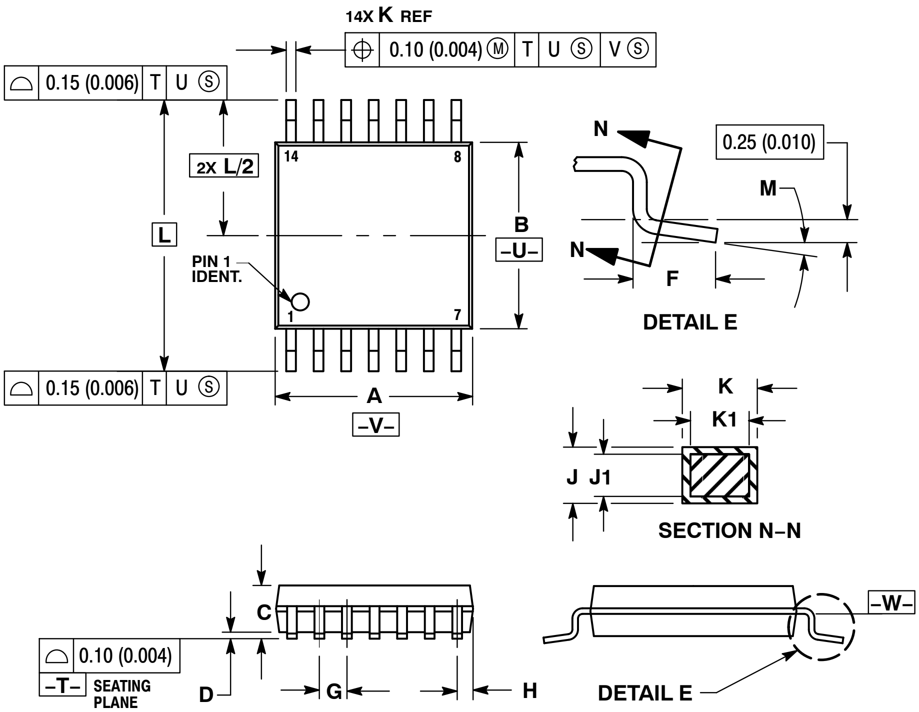


DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

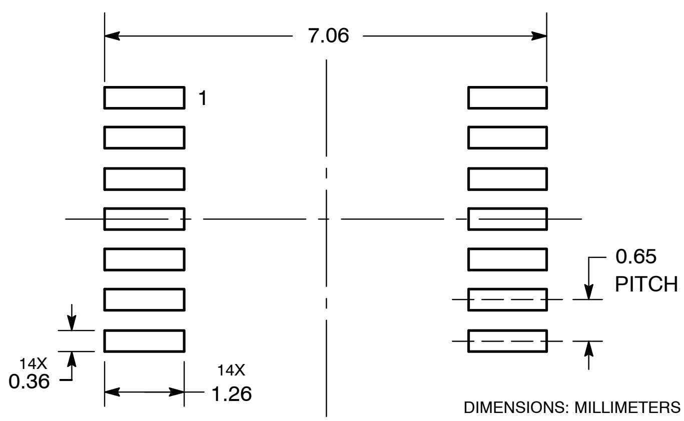
TSSOP−14 WB
CASE 948G
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



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