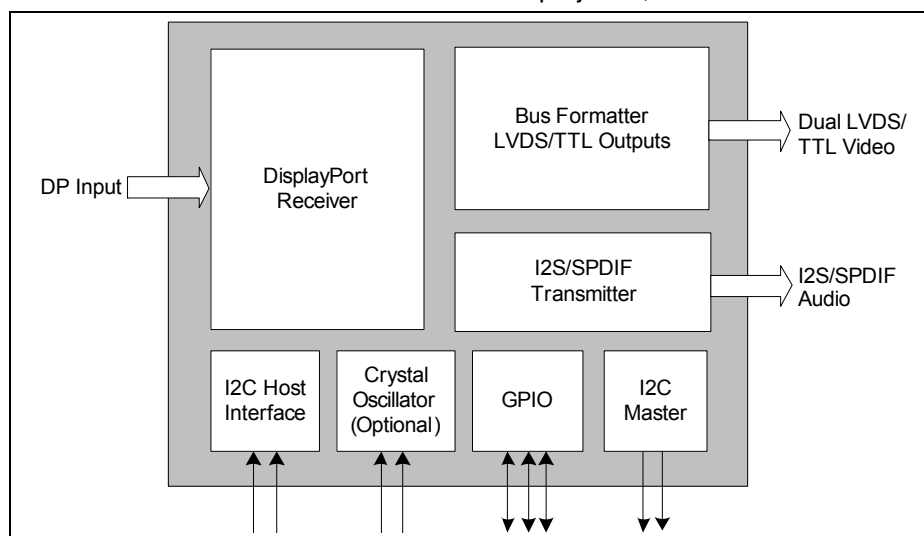


Features

- Enhanced DisplayPort® (DP) receiver
 - DP 1.1a compliant
 - Embedded DisplayPort (eDP) compliant
 - 1 or 2 lanes
- Higher bandwidth “Turbo mode” (3.24 Gbps per lane), supports:
 - 1920 x 1080 (FHD) 60 Hz/10-bit color video standard timings and 7.1 Ch audio
 - 1920 x1200 (WUXGA), 60 Hz color graphics and 7.1 Ch audio
- Interface compatibility with wide range of display controller ICs
 - LVTTTL (60 wide) and LVDS (dual bus) video interface
 - 8-Ch I2S and SPDIF audio interface
- Robust AUX channel
 - Link service, maintenance
 - I2C-over-AUX (MCCS, DDC)
 - IR, full duplex UART protocol
- Configurable through I2C host interface
- Supports HDCP 1.3 with on-chip keys
- HDCP repeater capability
 - Acts as upstream receiver
- AUX to I2C bridge for EDID, MCCS pass through
- Spread spectrum on DisplayPort, LVDS, and TTL interfaces for EMI reduction
- Supports deep color and color format conversion
 - RGB/YCC (4:4:4) – 10-bit color
 - YCC (4:2:2/4:2:0) – 12-bit color
 - RGB (4:4:4) to YCC (4:4:4) conversion and vice-versa
- Supports HBR/“Turbo” speed over HBR/RBR-rated long cables (15 m and more)
- Low power operation; 20 mW standby
- Package
 - 164 LFBGA (12 x 12 mm / 0.8 mm)
- Power supply voltages
 - 3.3 V I/O; 1.2 V core

Applications

- Digital TV, LCD monitor, mobile display, projector, etc.



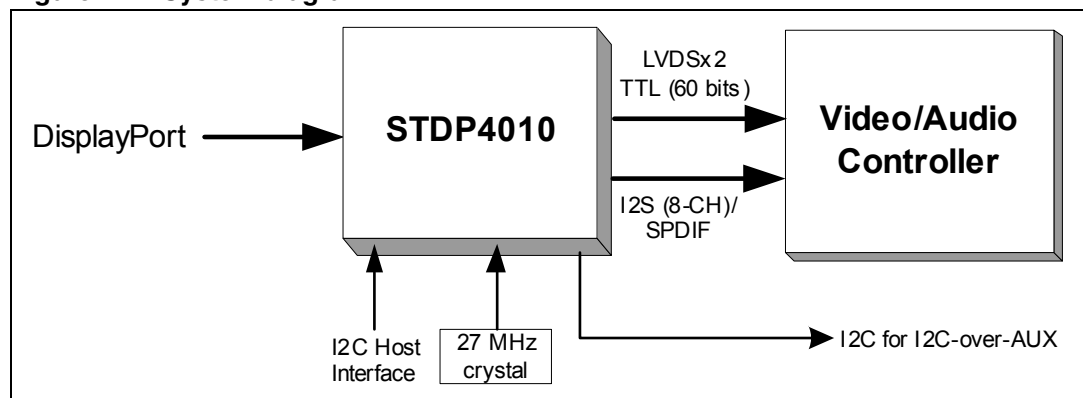
1 Description

The STDP4010 is a DisplayPort receiver IC for the secure reception of high-bandwidth uncompressed digital audio-video signals targeted for applications such as DTV, LCD monitor, projector, and other types of display systems. STDP4010 is a VESA DP 1.1a and eDP compliant device, implementing a single link DisplayPort input port comprising two main lanes, auxiliary channel, and HPD. In addition to the standard HBR (2.7 Gbps) and RBR (1.62 Gbps) speeds, this device supports “turbo” speed of 3.24 Gbps per lane with a total link bandwidth of 12.96 Gbps. The higher bandwidth provides unique benefits to users over other commercial DP receivers for embedded applications by offering additional margin to support higher color depth, resolution, and refresh rate. For example, STDP4010 supports FHD non-reduced blanking video (1080p 30-bit color per pixel) at 60 Hz, plus 7.1 Ch audio in two-box TV applications. The advanced equalizer built in this device offers guaranteed performance over long reach cables. The auxiliary channel in STDP4010 acts as a bidirectional communication link, supporting application-specific protocols such as MCCS, DDC, UART, IR, as well as the dedicated DisplayPort link training and device management functions.

The STDP4010 supports RGB and YCC video color formats with color depth of 12 (YCC 4:2:2 only), 10, and 8 bits. This device offers LVDS and LVTTTL output interfaces configurable to map a wide range of display controller products. The dual LVDS interface supports video signals up to 200 MHz pixel rate with flexible channel and lane swapping options. The 60-bit LVTTTL output ports can be mapped to transfer video data either in two pixels per clock or single pixel per clock up to 150 MHz pixel rate. The STDP4010 also supports both compressed and uncompressed audio formats. The extracted audio signal is transferred on a digital audio output bus. This device comprises four I2S audio output ports, supporting up to 8 channel LPCM audio and a single wire SPDIF output for encoded audio. The STDP4010 features HDCP 1.3 content protection scheme with an embedded key option for secure reception of digital audio-video content. In addition, it supports the HDCP repeater function and, thus acts as an upstream receiver suitable for two-box TV and DP to HDMI/DVI converter applications.

The STDP4010 is configurable from an external host controller through I2C host interface. This device also includes general purpose inputs/outputs for controlling system components. The STDP4010 features a color space converter (RGB to YCC and YCC to RGB) for flexible interface with external video processing devices.

Figure 1. System diagram



2 Benefits

- ST products offer proven interoperability with DP graphics controller and chipsets from all major graphics vendors
- 20% higher link bandwidth compared to other commercial DP receivers, supports FHD 60 Hz/10-bit non-reduced blank timing for embedded applications
- Supports both external (DP) and embedded (eDP) applications
- HDCP repeater capability, applicable for two-box TV and DP to HDMI/DVI converters
- Embedded HDCP keys
- On-chip microprocessor enables stand-alone operation for customized applications
- Flexible interface to ease system design – DP 1 or 2 lane configuration, LVDS/LVTTL port, YCC/RGB color format
- Low EMI
- Low power

3 Feature attributes

- Video
 - Up to 1920 x 1200-60 Hz, FHD 60 Hz at 10-bits color
 - 8/10/12 bits per color option
 - RGB/YCC color format
- Audio
 - 8-Ch I2S; word length up to 64 x Fs; bit depth up to 32 bits, sample rate up to 192 kHz
 - SPDIF; 2-Ch LPCM, AC3, DTS, bit depth up to 24 bits, sample rate up to 192 kHz
- Input interface
 - DP 1.1a (2 lanes, AUX, HPD); supported link speed 3.24 Gbps, 2.7 Gbps, 1.62 Gbps
- Output interface
 - Video: TTL 60/48 bits wide; dual LVDS 8/10 per color
 - Audio: I2S 8-Ch, SPDIF x1
- Spread spectrum
 - Supported on DP input and LVDS/TTL outputs
- AUX capabilities
 - UART, I2C-over-AUX (MCCS, DDC, etc.) IR
- HDCP
 - On-chip keys, HDCP repeater
- Color format conversion
 - RGB 4:4:4 to YCC 4:4:4 and vice-versa
- Dithering
 - 12 bpc to 10 bpc and 10 bpc to 8 bpc
- System configuration
 - I2C host interface for control by an external system microprocessor
- Package
 - 164 LFBGA (12 x 12 mm), 1 mm thickness, 0.8 pitch
- Power
 - Sub 900 mW max, 20 mW standby
- ESD
 - 2 KV HBM, 200 V MM, 750 V CDM

4 Ordering information

Table 1. Order codes

Part number	Description
STDP4010-AD	164 LFBGA (12 x 12 mm)

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
05-Dec-2012	1	Initial release.

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