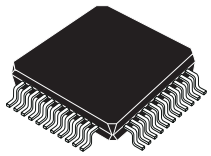
TDA7703

Highly integrated tuner for AM/FM car radio

Target specification

Features

- Fully integrated VCO for world tuning
- AM/FM mixers with high image rejection
- Integrated AM-LNA and AM-PINDIODE
- Automatic self alignment for image rejection
- Digital IF signal processing, high performance and drift-free
- Integrated IF-filters with high selectivity, high dynamic range and FM adaptive bandwidth control
- High performance stereodecoder with noiseblanker
- I^2C bus controlled
- Single 5 V supply
- LQFP44 package



LQFP44

Description

The TDA7703 highly integrated tuner (HIT44) is part of a family of tuners for carradio applications.

It contains mixers and IF amplifiers for AM and FM, fully integrated VCO and PLL synthesizer, IF-processing including adaptive bandwidth control (FM), stereo decoder on a single chip.

The utilization of digital signal processing results in numerous advantages against today's tuners:

- Very low number of external components
- Very small space occupation and easy application
- Very high selectivity due to digital filters
- High flexibility by software control
- Automatic image rejection alignment.

Table 1. Device summary

Order code	Package	Packing
TDA7703	LQFP44 (10x10x1.4mm)	Tray
TDA7703TR	LQFP44 (10x10x1.4mm)	Tape and reel

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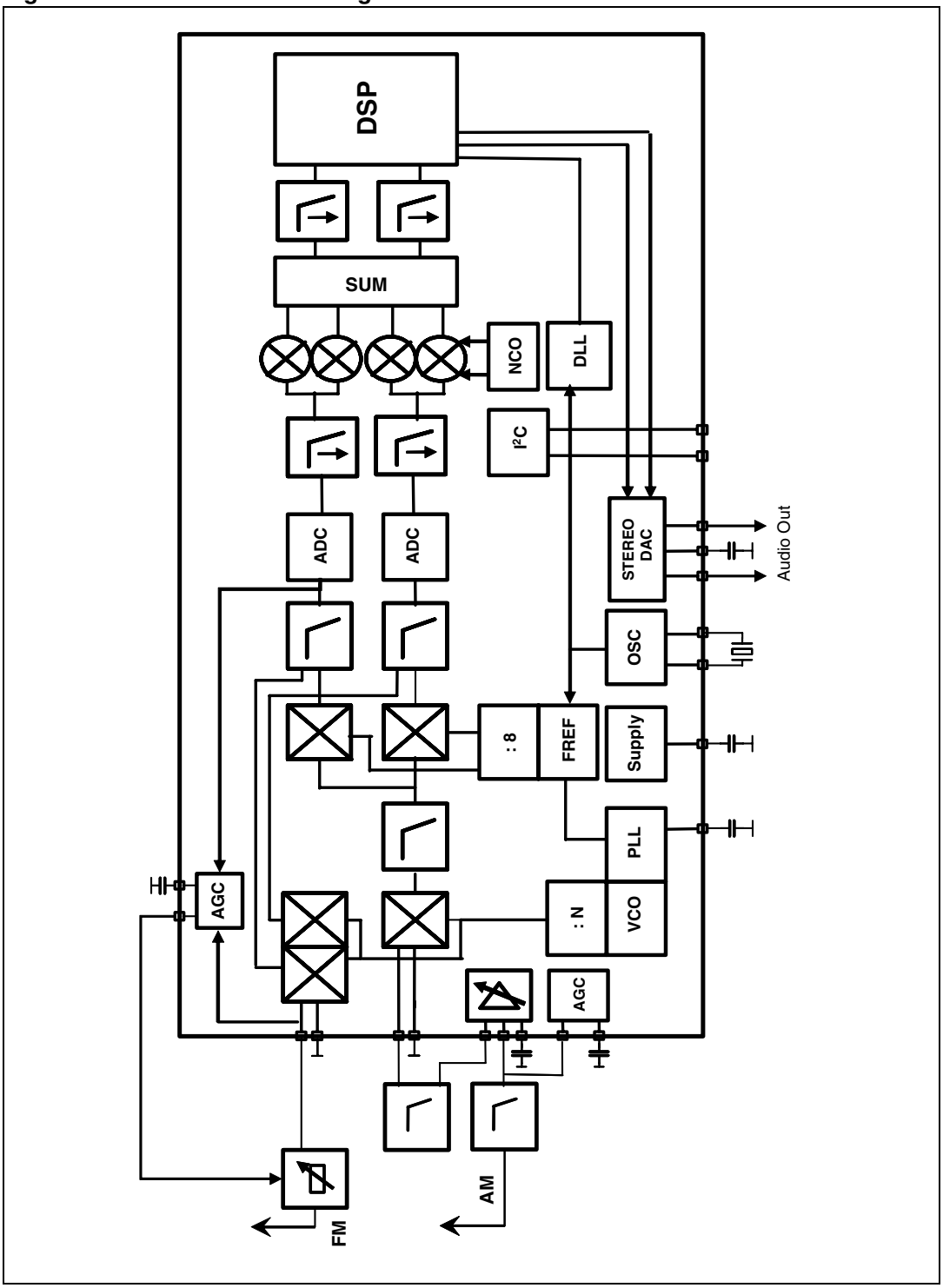
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Functional block diagram



1.2 Pin description

Figure 2. Pin connection (top view)

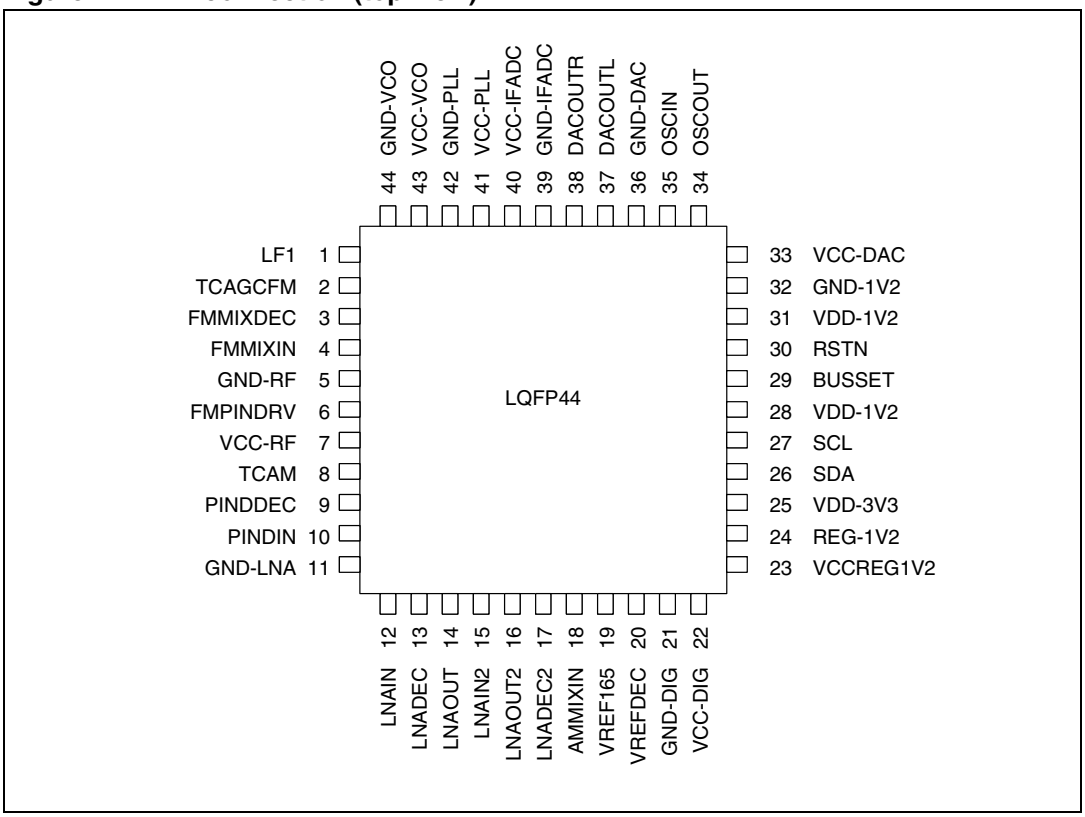


Table 2. Pin description

Pin #	Pin name	Description
1	LF1	PLL loopfilter output
2	TCAGCFM	FM AGC time constant
3	FMMIXDEC	FM mixer decoupling
4	FMIXIN	FM mixer input
5	GND-RF	RF Ground
6	FMPINDRV	FM AGC PIN diode driver
7	VCC-RF	5 V supply for RF section
8	TCAM	AM AGC time constant
9	PINDDEC	AM AGC internal PIN diode decoupling
10	PINDIN	AM AGC internal PIN diode input
11	GND-LNA	GND of AM LNA, AM internal PIN diode , AM mixer, IF
12	LNAIN	AM LNA input
13	LNADEC	AM LNA decoupling
14	LNAOUT	AM LNA output first stage

Table 2. Pin description (continued)

Pin #	Pin name	Description
15	LNAIN2	AM LNA input 2nd stage
16	LNAOUT2	AM LNA output
17	LNADEC2	AM LNA decoupling 2nd stage
18	AMMIXIN	AM mixer input
19	VREF165	1.65 V reference voltage decoupling
20	VREFDEC	3.3 V reference voltage decoupling
21	GND-DIG	Digital GND
22	VCC-DIG	5 V supply for digital logic
23	VCCREG1V2	VCC of 1.2 V regulator
24	REG1V2	1.2 V regulator output
25	VDD-3V3	3.3 V VDD output / decoupling
26	SDA	I^2C bus data
27	SCL	I^2C bus clock
28	VDD-1V2	1.2 V DSP supply
29	BUSSET	Bus communication setup
30	RSTN	Reset pin (active low)
31	VDD-1V2	1.2 V DSP supply
32	GND-1V2	Digital GND for 1.2 V VDD
33	VCC-DAC	5 V supply of audio DAC
34	OSCOUT	Xtal osc output
35	OSCIN	Xtal osc input
36	GND-DAC	Audio DAC GND
37	DACOUTL	Audio output left
38	DACOUTR	Audio output right
39	GND-IFADC	IF ADC GND
40	VCC-IFADC	5 V supply of IF ADC
41	VCC-PLL	5 V supply of PLL
42	GND-PLL	PLL GND
43	VCC-VCO	5 V supply of VCO
44	GND-VCO	VCO GND

2 Function description

2.1 FM - mixer

The FM image-rejection mixer is optimized for best performance with a passive wide-band prestage.

The input frequency is downconverted to low IF with high image rejection.

2.2 FM - AGC

The programmable RFAGC senses the mixer input whereas the IFAGC senses the IFADC input to avoid overload.

The PIN diode driver is able to drive external PIN diodes with a current value as high as 15mA.

The time constant of the FM-AGC is defined by an external capacitor.

2.3 AM - LNA

The AM-LNA is integrated with low noise and high IIP2 and IIP3. The gain of the LNA is controlled by the AGC. The maximum gain is set with an external resistor, typically 28 dB with 1.5 kΩ.

2.4 AM - AGC

The programmable AM-RF-AGC senses the mixer inputs and controls the internal PIN diode and LNA gain.

First the LNA gain is reduced by about 10dB, then the PIN diodes are activated to attenuate the signal.

The time constant of the AM-AGC is defined with an external capacitor and programmable internal currents.

2.5 AM - mixer

The AM mixer converts RF to low IF with high image rejection.

2.6 IF A/D converters

A high performance IQ-IFADC converts the IF-signal to digital IF for subsequent digital signal processing.

2.7 Audio D/A converters

A stereo DAC provides the left / right audio signals after IF-processing and stereodecoding by the DSP.

2.8 VCO

The VCO is fully integrated without any external tuning component. It covers all FM frequency bands including EU, US, Japan, EastEU and AM-bands including LW and MW.

2.9 PLL

The high speed tuning PLL is able to settle within about 300 µs.

The frequency step can be as low as 5 kHz in FM and 500 Hz in AM.

2.10 Crystal oscillator

The device works with a 37.05 MHz fundamental tone crystal, and can be used also with a 3rd overtone 37.05 MHz crystal.

2.11 DSP

The DSP and its hardware accelerators perform all the digital signal processing. The main program is fixed in ROM. Control parameters are copied in RAM and are accessible and modifiable there, thus allowing parametric performance optimization.

It performs:

- digital down-conversion of IF
- bandwidth selection with variable controlled bandwidth
- FM noiseblanking
- FM/AM demodulation with softmute, high-cut, weak signal processing and quality detection
- FM stereo decoding with stereo blend

2.12 IO interface pins

The TDA7703 has the following IO pins:

SDA	pin 26	serial communication with µP
SCL	pin 27	serial communication with µP
BUSSET	pin 29	serial communication with µP
RSTN	pin 30	reset pin driven by µP

All the inputs are voltage-tolerant up to 3.5 V . The outputs can drive currents up to 0.5 mA from the internal 3.3 V supply line.

2.13 Serial interface

The device is controlled with a standard I^2C bus interface.

Through the serial bus the processing parameters can be modifed and the signal quality parameters can be read out.

The operation of the device is handled through high level commands sent by the main car-radio µP through the serial interface, which allow to simplify the operations carried out in the main µP. The high level commands include among others:

- set frequency (which allows to avoid computing the PLL divider factors);
- start seek (the seek operation can be carried out by the TDA7703 in a completely autonomous fashion).

The serial bus communication configuration is set by forcing pin 29 (BUSSET) to ground when the RSTN line transitions from low to high (when RSTN is low, the IC is in reset mode).

The voltage level forced to pin 29 must be released to start the system operation a suitable time after the RSTN line has gone high. The I^2C address is 0xC2 (write) / 0xC3 (read).

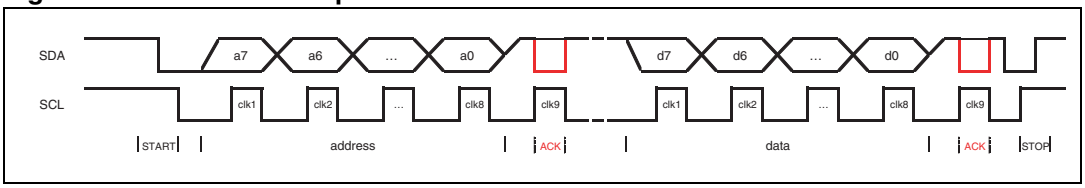
The status of pin 29 during the reset phase can be set to low by not forcing any voltage on it from outside, as a 50 kΩ internal pull-down resistors is present.

To make sure the boot mode is correctly latched up at start-up, it is advisable to keep the RSTN line low until the IC supply pins have reached their steady state, and then for an additional time T_{reset} (see *Section 3.4.6*).

I^2C requires two signals: clock (SCL) and data (SDA - bidirectional). The protocol requires an acknowledge after any 8-bit transmission.

A "write" communication example is shown in the figure below, for an unspecified number of data bytes (see Communication Protocol Manual for frame structure description):

Figure 3. I^2C "write" sequence



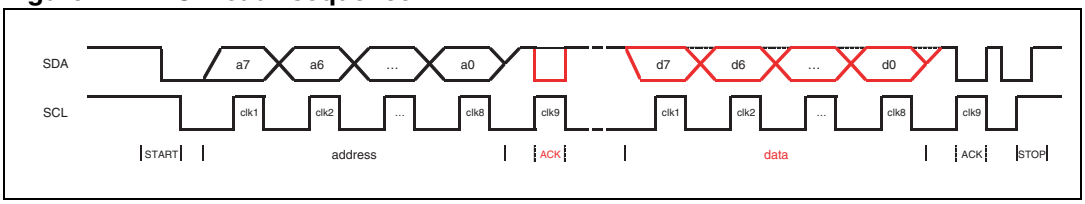
The sequence consists of the following phases:

- START: SDA line transitioning from H to L with SCL fixed H. This signifies a new transmission is starting;
- data latching: on the rising SCL edge. The SDA line can transition only when SCL is low (otherwise its transitions are interpreted as either a START or a STOP transition);
- ACKnowledge: on the 9th SCL pulse the µP keeps the SDA line H, and the TDA7703 pulls it down if communication has been successful. Lack of the acknowledge pulse generation from the TDA7703 means that the communication has failed;
- a chip address byte must be sent at the beginning of the transmission. The value is C2 for "write";
- as many data bytes as needed can follow the address before the communication is terminated. See the next section for details on the frame format;
- STOP: SDA line transitioning from L to H with SCL H. This signifies the end of the transmission.

Red lines represent transmissions from the TDA7703 to the µP.

A "read" communication example is shown in the figure below, for an unspecified number of data bytes (see later on for frame structure decription):

Figure 4. I^{2}C "read" sequence



The sequence is very similar to the "write" one and has the same constraints for start, stop, data latching. The differences follow:

- a chip address must always be sent by the µP to the TDA7703; the address must be C3;
- a header is transmitted after the chip address (the same happens for "write") before data are transferred from the TDA7703 to the µP. See the Communication Protocol Manual for details on the frame format;
- when data are transmitted from the TDA7703 to the µP, the µP keeps the SDA line H;
- the ACKnowledge pulse is generated by the µP for those data bytes that are sent by the TDA7703 to the µP. Failure of the µP to generate an ACK pulse on the 9th CLK pulse has the same effect on the TDA7703 as a STOP.

The max. clock speed is 500 kbit/s.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CC}	Supply voltage				5.5	V
T_{stg}	Storage temperature		-55		150	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Test condition	Value	Units
$R_{Th\ j\text{-}case}$	Thermal resistance junction to case	LQFP44 10x10, double-layer JEDEC PCB	55	°C/W

3.3 General key parameters

Table 5. General key parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CC}	5 V supply voltage		4.7	5	5.25	V
I_{CC}	Supply current @ 5 V			220	295	mA
T_{amb}	Ambient temperature range		-30		75	°C
$V_{VCCREG12}$	VCCREG12 supply voltage	see note(1)	2			V
V_{1V2}	Digital core 1.2V supply voltage	when supplied externally see note (2)	1.08	1.2	1.32	V
I_{1V2}	Digital core 1.2 V supply current	V_{1V2} = 1.08 V see note (2)			120	mA
		V_{1V2} = 1.2 V see note (2)		80	135	mA
		V_{1V2} = 1.32 V see note (2)			150	mA

1. In the typical application supplied from 5V with a series resistor.
2. When the 1.2 V supply is applied externally, and not using the internal 1.2 V regulator.

3.4 Electrical characteristics

V_{CC} = 5 V; T_{amb} = 27 °C; unless otherwise specified.

3.4.1 FM - section

Table 6. FM - section

Symbol	Parameter	Test condition	Min	Typ	Max	Units
FM IMR mixer						
R_{in}	Input resistance		90	130	170	kΩ
IIP3	3rd order intercept point	up to $V_{in/tone}$ = 85 dBµV		121		dBµV
FM AGC						
RFAGC-Thr	RFAGC threshold, referred to mixer input; RF level	min setting		85		dBµV
		max setting		91		
	Threshold steps			2		dB
	Threshold error		-1.5		1.5	dB
	Threshold temperature drift			0.016		dB/K
IFAGC-Thr	IFAGC threshold, referred to mixer input; at tuned frequency RF level	min setting		77		dBµV
		max setting		81		
	Threshold steps			2		dB
	Threshold error		-1.5		1.5	dB
	Threshold temperature drift			0.016		dB/K
	Pin diode source current	see note(1)	12			mA
	Pin diode sink current		3		20	µA
	Pin diode source current in constant current mode	see note(1)	0.4			mA

1. The current is generated by a PTAT (Proportional To Absolute Temperature) source, and has therefore a temperature dependency described by: ΔI/Io = ΔT/To, with Io being the current at ambient temperature (25 °C) and To the ambient temperature (25°C) expressed in Kelvin, that is 298 K.

3.4.2 AM - section

Table 7. AM - section

Symbol	Parameter	Test condition	Min	Typ	Max	Units
AM IMR Mixer						
R_{in}	Input resistance		20	30	45	kΩ
IIP3	3rd order intercept point	up to $V_{in/tone}$ = 90 dBµV		129		dBµV
IIP2	2nd order intercept point	up to $V_{in/tone}$ = 90 dBµV		158		dBµV
LO hsupp	LO harmonic suppression	N=2,3,4,5,6		100		dB
		N=7,9		85		
AM LNA						
Gain	Voltage gain	Max Gain, R_{ext} = 1.5 kΩ	24	28	31	dB
		Min Gain (AGC controlled)		12		
R_{in}	Input resistance			1000		kΩ
C_{in}	Input capacitance			20		pF
IIP3	3rd order intercept point	@ maximum LNA gain		125		dBµV
IIP2	2nd order intercept point	@ maximum LNA gain		143		dBµV
AM PIN diode						
IIP2	2nd order intercept point	Full attenuation, C_{source} = 80 pF, f=1 MHz		140		dBµV
R_{min}	Minimum resistance			50	80	Ω
C_{in}	Input capacitance	High ohmic		12		pF
AM AGC						
AGC-Thr	Referred to mixer input RF level	min setting		87		dBµV
		max setting		93		
Thr-steps	Threshold steps			1		dB
	Threshold error		-2.5		2.5	
	Threshold temperature drift		-3		3	

3.4.3 VCO

Table 8. VCO

Symbol	Parameter	Test condition	Min	Typ	Max	Units
F_{VCO}	Frequency range VCO		1100		1550	MHz
PN	Phase noise of LO	Locked VCO; values referred @ 100MHz @ 100 Hz @ 1 kHz @ 10 kHz		 -100 -115 -115		dBc/Hz
dev	Deviation error (rms)	FM reception, deemphasis 50µs, f_{audio}=20Hz...20kHz		5		Hz

3.4.4 Phase locked loop

Table 9. Phase locked loop

Symbol	Parameter	Test condition	Min	Typ	Max	Units
T_{settle}	Settling time FM	$\Delta f < 10$ kHz		300		µs
FM step	FM frequency step			5		kHz
AM step	AM frequency step			500		Hz

3.4.5 Audio DAC

Table 10. Audio DAC

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{out}	Output voltage	AM 90% modulation; FM 75 kHz deviation. 400 Hz audio frequency		300		mVrms
BW	Bandwidth	1 dB attenuation		15		KHz
R_{out}	Output resistance		600	750	900	Ω

3.4.6 IO interface pins

Table 11. IO interface pins

Symbol	Parameter	Test condition	Min	Typ	Max	Units
	High level output voltage	I_{out} = 500µA	2.9	3.2		V
	Low level output voltage	I_{out} = -1mA		0.1	0.3	V
	Input voltage range		0		3.5	V
	High level input voltage		2.0			V
	Low level input voltage				0.8	V
T_{reset}	Reset time	Minimum time during which pin RSTN must be low so as to reset the device	10			µs
T_{latch}	Boot mode configuration latch time	Minimum time during which the voltage applied at pin 29 must be kept in order to latch the correct boot mode (serial bus configuration)	10			µs

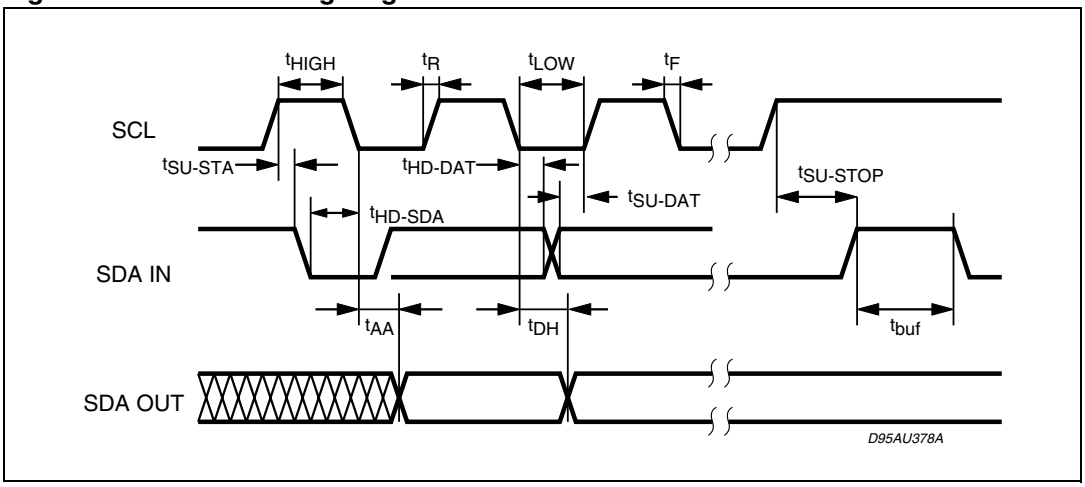
3.4.7 I²C interface

The parameters of the following table are defined as in *Figure 5*.

Table 12. I²C interface

Symbol	Parameter	Test condition	Min	Typ	Max	Units
f_{SCL}	SCL Clock frequency				500	kHz
t_{AA}	SCL low to SDA data valid		0.3			µs
t_{buf}	time the bus must be kept free before a new transmisison		1.3			µs
t_{HD-STA}	START condition hold time		0.6			µs
t_{LOW}	Clock low period		1.3			µs
t_{HIGH}	Clock high period		0.6			µs
t_{SU-SDA}	START condition setup time		0.1			µs
t_{HD-DAT}	Data input hold time		0.3		0.9	µs
t_{SU-DAT}	Data input setup time		0.1			µs
t_R	SDA & SCL rise time				0.3	µs
t_F	SDA & SCL fall time				0.3	µs
$t_{SU-STOP}$	Stop condition setup time		0.6			µs
t_{DH}	Data out time				0.3	µs

Figure 5. I²C bus timing diagram



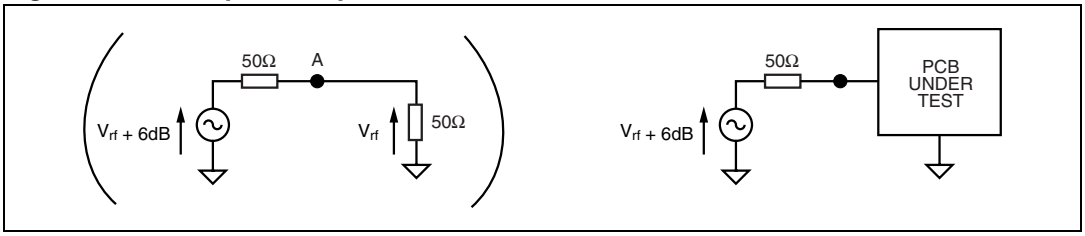
3.5 Overall system performance

All measurements obtained with application of *Figure 9* unless otherwise specified.

3.5.1 FM overall system performance

Antenna level equivalence: 0 dBµV = 1 μV_{rms} (Antenna terminal voltage with 50 Ω source).

Figure 6. FM input set-up



Input level referred to signal generator loaded with 50 Ω (V_{rf}, node 'A'); no antenna dummy; AM input not connected. F_{rf} = 98.1 MHz, V_{rf} = 60 dBµV, mono modulation, f_{dev} = 40 kHz, f_{audio} = 1 kHz. De-emphasis = 50 µs. Unless otherwise specified

Table 13. FM overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range FM Eu	(can be modified by the user)	87.5		108	MHz
Tuning step FM Eu			100		kHz
Tuning range FM US		87.5		107.9	MHz
Tuning step FM US			200		kHz
Tuning range FM Jp		76		90	MHz
Tuning step FM Jp			100		kHz
Tuning range FM EEu		65		74	MHz
Tuning step FM EEu			100		kHz
Sensitivity	S/N =26dB		-3	0	dBµV
Ultimate S/N	@ 60 dBµV, mono	72	75		dB
	@ 60 dBµV, Deviation = 75 kHz, mono	77	80		dB
	@ 60 dBµV, stereo	70	73		dB
Distortion	Deviation= 75 kHz		0.15		%
Max deviation	THD=3%	120			kHz
Adjacent channel selectivity (V_u/V_d)	ΔF=100 kHz, SINAD=30 dB desired 40 dBµV, dev=40kHz, 400Hz undesired. dev=40kHz, 1KHz		13		dB
Alternate channel selectivity (V_u/V_d)	ΔF=200 kHz, SINAD=30 dB desired 40 dBµV, dev=40 kHz, 400 Hz undesired. dev=40kHz, 1kHz		62		dB

Table 13. FM overall system performance (continued)

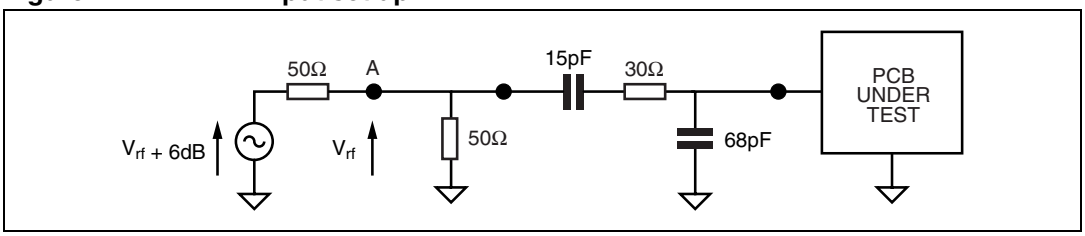
Parameter	Test condition	Min	Typ	Max	Units
Max. strong signal interferer (V_u/V_d)	Desired = 40 dBµV SINAD = 30dB Undesired ΔF = 5MHz dev = 40kHz, 1kHz		75		dB
3 signal performance (V_{u1} & V_{u2}/V_d)(1)	Desired = 40 dBµV, dev=40kHz, 400Hz, SINAD=30dB Undesired1 =±400kHz, dev=40kHz, 1 kHz Undesired2=±800kHz, no mod		62		dB
	Desired = 40 dBµV, dev=40kHz, 400Hz, SINAD=30dB Undesired1 =±1MHz, dev=40kHz, 1 kHz Undesired2=±2MHz, no mod		65		dB
AM suppression	m=30%		70		dB
Image rejection			80		dB
Logarithmic field strength indicator	@40 dBµV read “FM_Smeter_log”	-0.33 (equiv. to 37 dBµV)	-0.3	-0.27 (equiv. to 43 dBµV)	-

1. Signal levels referred to combiner output.

3.5.2 AM MW overall system performance

Antenna level equivalence: 0 dBµV = 1 μV_{rms}.

Figure 7. AM MW input set up



Level referred to SG output before antenna dummy (V_{rf}, node 'A'); capacitive dummy 15pF+68pF, FM input not connected. F_{rf} = 999 kHz (1000 kHz for US), V_{rf} =74 dBµV, mod = 30%, f_{audio} =400 Hz, unless otherwise specified.

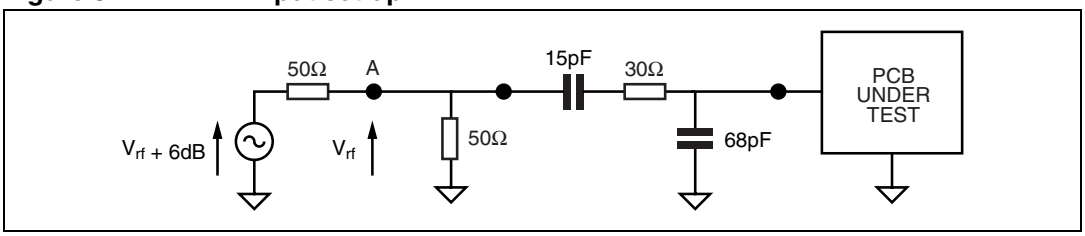
Table 14. AM MW overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range MW Eu/Jp	(can be modified by the user)	531		1629	kHz
Tuning step MW Eu/Jp	(can be modified by the user)		9		kHz
Tuning range MW US	(can be modified by the user)	530		1710	kHz
Tuning step MW US	(can be modified by the user)		10		kHz
Sensitivity	S/N = 20 dB		29	32	dBµV
Ultimate S/N	@ 80 dBµV	63	66		dB
AGC F.O.M.	Ref.=74 dBµV -10dB drop point	50	62	65	dB
Distortion	m = 80 %		0.1		%
Adjacent channel selectivity	ΔF=9 kHz, V_{audio} = -10 dBr (relative to ΔF = 0 kHz), m=30%, 1 kHz		97		dB
Alternate channel selectivity	ΔF=18 kHz, V_{audio} = -10 dBr (relative to ΔF = 0 kHz), m=30%, 1kHz		97		dB
Image rejection			80		dB
Logarithmic field strength indicator	@60 dBµV read “AM_Smeter_log”	0.50 (equiv. to 57 dBµV)	0.47	0.43 (equiv. to 63 dBµV)	-

3.5.3 AM LW overall system performance

Antenna level equivalence: 0dBµV = 1µV_{rms}

Figure 8. AM LW input set-up



Level referred to SG output before antenna dummy (V_{rf}, node 'A'); capacitive dummy 15pF+68pF; FM input not connected. F_{rf} = 216 kHz, V_{rf} =74 dBµV, mod = 30 %, f_{audio} = 400 Hz, unless otherwise specified.

Table 15. AM LW overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range LW	(can be modified by the user)	144		288	kHz
Tuning step LW	(can be modified by the user)		1		kHz
Sensitivity	S/N =20dB		31	34	dBµV
Ultimate S/N	@ 80 dBµV	63	66		dB
AGC F.O.M.	Ref.=74 dBµV -10dB drop point	50	62	65	dB
Distortion	m = 80 %		0.1		%
Image rejection			80		dB

4 Front-end processing

All the parameters in this section refer to the programmability of the FE part of the device (registers). The part of the registers that are not described here have either fixed values or values written by the tuner drivers, and are described in the proper technical documentation (Communication Protocol manual).

Table 16. Register 0x00

Register number																							Register definition
MSB																						LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								AM AGC mode
										0														LNA and PIN diode
										1														PIN diode only
																								AM AGC time constant
								0	0															slow (125 ms with 1 µF)
								0	1															medium (25 ms with 1 µF)
								1	1															fast (5 ms with 1 µF)
																								AM AGC threshold @ mixin
					0	0	0																	90 dBµV
					0	0	1																	91 dBµV
					0	1	0																	92 dBµV
					0	1	1																	93 dBµV
					1	0	0																	90 dBµV
					1	0	1																	89 dBµV
					1	1	0																	88 dBµV
					1	1	1																	87 dBµV
																								AM AGC attack time constant
			0																					normal
			1																					fast

Table 17. Register 0x01

Register number																						Register definition
MSB																					LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								FM mixer gain
								0																high
								1																low
																								FM AGC time constant
		0																						normal
		1																						fast
																								FM AGC output mode
0	0																							normal
0	1																							constant 15 mA
1	0																							constant 1 mA

Table 18. Register 0x02

Register number																						Register definition
MSB																					LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								FM RF AGC threshold @ mixin
																						0	0	87 dBµV
																						0	1	89 dBµV
																						1	0	91 dBµV
																						1	1	93 dBµV
																								FM iF AGC threshold @ IFADC in
																				0	0			120 dBµV
																				0	1			122 dBµV
																				1	0			124 dBµV

5 Weak signal processing

All the parameters in this section refer to the programmability of the DSP part of the device. The typical values are those set by default parameters (start-up without parametric change from main µP); the max and the min values refer to the programmability range. The values are referred to the typical application. Wherever the possible values are a discrete set, all the possible programmable values are displayed.

5.1 FM IF-processing

5.1.1 Dynamic channel selection filter (DISS)

Table 19. Dynamic channel selection filter (DISS)
(discrete set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
DISS BW	IF filter #2	response: - 3dB	-	±80	-	kHz
	IF filter #1		-	±60	-	kHz
	IF filter #0		-	±40	-	kHz

5.1.2 Soft mute

Table 20. Soft mute
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
SMsp	Start point vs. field strength	audio atten = 1 dB read “FM_softmute” no adjacent channel present	0	6	20	dBµV
SMep	End point vs. field strength	audio atten = SMd + 1 dB read “FM_softmute” no adjacent channel present	-6	-6	10	dBµV
SMd	Depth		-30	-15	0	dB
SMtauatt	Field strength LPF cut-off frequency for soft mute activation		0.1	100	4000	Hz
SMtaurel	Field strength LPF cut-off frequency for soft mute release		0.1	1	4000	Hz

5.1.3 Adjacent channel mute

Table 21. Adjacent channel mute
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
ACMd	Depth		SMd	0	0	dB

5.1.4 Stereo blend

Table 22. Stereo blend
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
MaxSep	Maximum stereo separation	field strength = 80 dBµV, pilot deviation = 6.75 kHz	0	40	50	dB
SBFSsp	Start point vs. field strength	separation = MaxSep - 1 dB no multipath present	20	50	60	dBµV
SBFSep	End point vs. field strength	separation = 1 dB no multipath present	20	30	60	dBµV
SBFStM2S	Field strength-related transition time from mono to stereo	V_{rf} step-like variation from 20 dBµV to 80 dBµV	0.001	3	20	s
SBFStS2M	Field strength-related transition time from stereo to mono	V_{rf} step-like variation from 80 dBµV to 20 dBµV	0.001	0.5	20	s
SBMPsp	Start point vs. multipath	separation = MaxSep - 1 dB equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	10	80	%
SBMPep	End point vs. multipath	separation = 1 dB equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	30	80	%
SBMPtM2S	Multipath -related transition time from mono to stereo	V_{rf} step-like variation from 20 dBµV to 80 dBµV	0.001	1	20	s
SBMPtS2M	Multipath -related transition time from stereo to mono	V_{rf} step-like variation from 80 dBµV to 20 dBµV	0.001	0.001	20	s
Pil ThrM2S	Pilot detector stereo threshold	Threshold on pilot tone deviation for mono-stereo transition	0.8	2.74	7	kHz
Pil ThrHyst	Pilot detector threshold hysteresis	Difference in pil. det. deviation threshold for stereo to mono transition compared to PilThrM2S	-	0.01	-	kHz

5.1.5 High cut control

Table 23. High cut control
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
HCFSsp	Start point vs. field strength	minimum RF level for widest HC filter (filter # 7) no multipath present	0	50	50	dBµV
HCFSep	End point vs. field strength	maximum RF level for narrowest HC filter (filter # 0) no multipath present	0	30	40	dBµV
HCFStW2N	Field strength-related transition time from wide to narrow band	V_{rf} step-like variation from 60 dBµV to 10 dBµV	(1)			-
HCFStN2W	Field strength-related transition time from narrow to wide band	V_{rf} step-like variation from 0 dBµV to 60 dBµV	(1)	14	100	s
HCMPsp	Start point vs. multipath	minimum RF level for widest HC filter (filter # 7) equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	10	150 (2)	%
HCMPep	End point vs. multipath	maximum RF level for narrowest HC filter (filter # 0) equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	30	150 (2)	%
HCMPtN2W	Multipath -related transition time from narrow to wide band	V_{rf} step-like variation from 20 dBµV to 80 dBµV	0.001	0.001	20	s
HCMPtW2N	Multipath -related transition time from wide to narrow	V_{rf} step-like variation from 80 dBµV to 20 dBµV	0.001	0.001	20	s
HCmaxBW	Maximum cut-off frequency of high cut filter bank	Filter #7, -3 dB response frequency, input signal with pre-emphasis	HCmin BW	14	18	kHz
HCminBW	Minimum cut-off frequency of high cut filter bank	Filter #0, -3 dB response frequency, input signal with pre-emphasis	0.1	3	HCma xBW	kHz
HCnumFilt	Number of discrete HC filters	-	-	8 (3)	-	-

1. Depends only on field strength filter time constant.
2. Means that 100% equivalent 19 kHz AM modulation depth will not achieve full band narrowing.
3. Intermediate filters (#6 - #1) cut-off frequencies exponentially spaced between HCmaxBW and HCminBW.

Table 24. De-emphasis filter
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
DEtc	De-emphasis time constant 1		-	50	-	µs
	De-emphasis time constant 2		-	75	-	

5.1.6 Stereo decoder

Table 25. Stereo decoder

Symbol	Parameter	Test condition	Min	Typ	Max	Units
PilSup	Pilot signal suppression	Pilot 9%, 19 kHz, ref=40 kHz	-	60	-	dB
SubcSup	Subcarrier suppression	f = 38 kHz	-	70	-	dB
		f = 57 kHz	-	70	-	dB
		f = 76 kHz	-	80	-	dB

5.2 AM IF-processing

5.2.1 Channel selection filter

Table 26. Channel selection filter

Symbol	Parameter	Test condition	Min	Typ	Max	Units
CSF BW	Channel selection filter BW	response: - 3dB	-	±3.7	-	kHz

5.2.2 Soft mute

Table 27. Soft mute
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
SMsp	Start point vs. field strength	audio atten = 1 dB read “FM_softmute” no adjacent channel present	0	25	40	dBµV
SMep	End point vs. field strength	audio atten = SMd + 1 dB read “FM_softmute” no adjacent channel present	0	0	30	dBµV
SMd	Depth		-40	-24	0	dB
SMtauatt	Transition time for field strength-dependent soft mute activation		0.001	0.1	10	s
SMtaurel	Transition time for field strength-dependent soft mute release		0.001	3	10	s

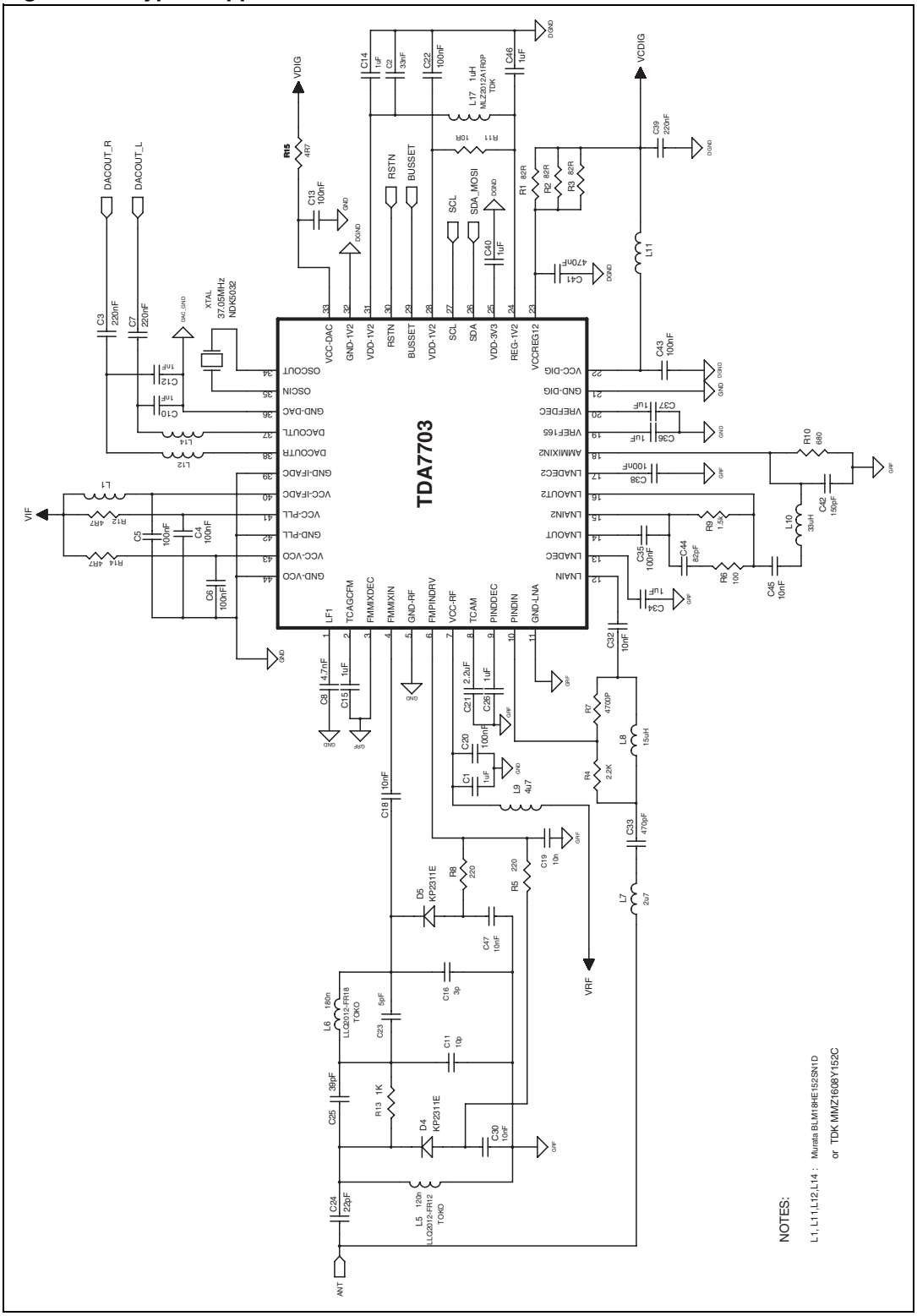
5.2.3 High cut control

Table 28. High cut control
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
HCFSsp	Start point vs. field strength	minimum RF level for widest HC filter (filter # 7) no multipath present	0	40	50	dBµV
HCFSep	End point vs. field strength	maximum RF level for narrowest HC filter (filter # 0) no multipath present	0	30	50	dBµV
HCFStW2N	Field strength-related transition time from wide to narrow band	V_{rf} step-like variation from 60 dBµV to 10 dBµV	0.001	0.2	20	s
HCFStN2W	Field strength-related transition time from narrow to wide band	V_{rf} step-like variation from 0 dBµV to 60 dBµV	0.001	10	20	s
HCnumFilt	Number of discrete HC filters		-	8	-	-

6 Application schematic

Figure 9. Typical application schematic



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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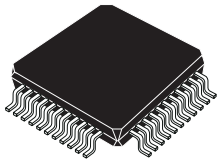
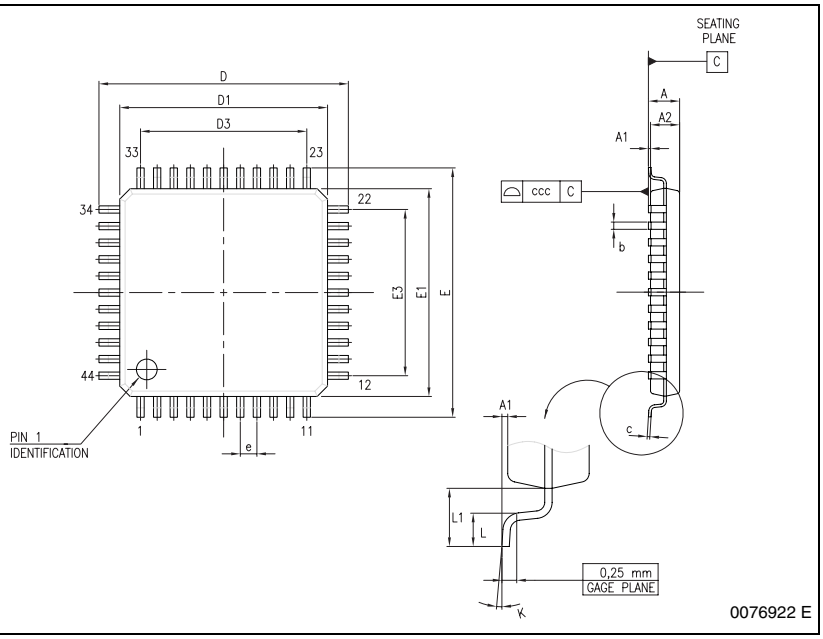
Figure 10. LQFP44 (10x10x1.4mm) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					
ccc			0.10			0.0039

OUTLINE AND MECHANICAL DATA



LQFP44 (10 x 10 x 1.4mm)



8 Revision history

Table 29. Document revision history

Date	Revision	Changes
24-Apr-2009	1	Initial release.

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