| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add device type 02. Add package Y. Add radiation features. Editorial changes throughout. - drw | 01-06-29 | Raymond Monnin |
| B | Add device type 03. - drw | 01-08-29 | Raymond Monnin |
| C | Add appendix A, die requirements. Editorial changes throughout. - drw | 03-05-15 | Raymond Monnin |
| D | Change to appendix A, figure A-1. - drw | 03-06-05 | Raymond Monnin |
| E | Add case outline X for vendor CAGE 27014. -rrp | 03-06-10 | Raymond Monnin |
| F | Add device types 04 and 05. Editorial changes throughout. - drw | 04-08-25 | Raymond Monnin |
| G | Sheet 6, table I, $I_{CCZ}$ test for device types 04 and 05, change from 2.7 mA max to 3.0 mA max. - drw | 04-10-25 | Raymond Monnin |
| H | Make clarifications to 1.5, 4.4.4.1, 4.4.4.2, and A.1.2. Add a footnote to 1.5. Add paragraph 3.1.1. - ro | 09-05-05 | Joseph D. Rodenbeck |
| J | Add device type 06. Add vendor CAGE F8859. Add paragraphs 2.2, 4.4.4.1.1, and Table IB and Table IIB. Under Table IIA device class V column; add subgroup1 to Interim electrical parameters, add subgroups 7, 8, 9, 10, 11 to Group C end point electrical parameters, and add subgroups 7, 9 to Group E end point electrical parameters. - ro | 10-06-28 | Charles F. Saffle |
| K | Add device type 07, case outline Z, figure A-2, and Neutron testing paragraph. Delete device class M references. - ro | 14-06-18 | Charles F. Saffle |
| L | Under paragraph 1.3, make change to the device type 07 Output voltage maximum limit. - ro | 15-02-23 | Charles F. Saffle |
| M | Add device type 08 and add delta burn-in parameters to Table IIB. Add note under figure A-1. - ro | 15-10-22 | Charles F. Saffle |

| REV | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | M | M | M | M | M | M | M | M | M | M | M | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | | | | | | | | | |

| REV STATUS | REV | M | M | M | M | M | M | M | M | M | M | M | M | M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
DAN WONNELL

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**http://www.landandmaritime.dla.mil**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAYMOND MONNIN

APPROVED BY
RAYMOND MONNIN

DRAWING APPROVAL DATE
99-05-26

REVISION LEVEL
M

MICROCIRCUIT, LINEAR, CMOS, 3 VOLT LVDS QUAD DIFFERENTIAL LINE DRIVER, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-98651** |

SHEET 1 OF 25

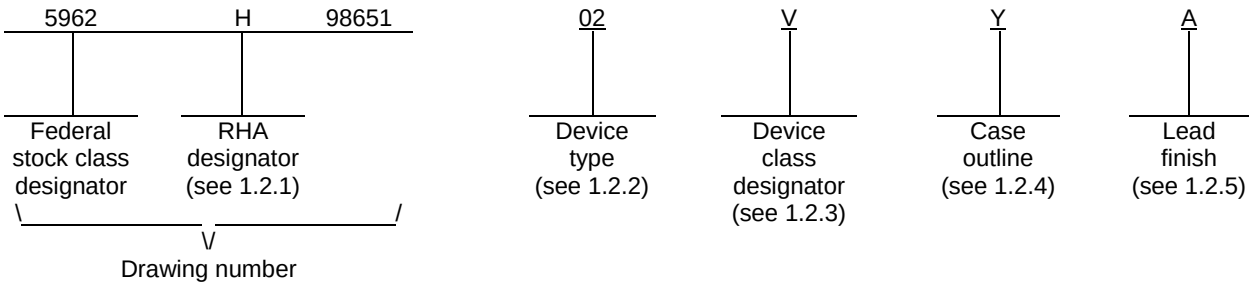
DSCC FORM 2233
APR 97

5962-E033-16

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | DS90LV031A | 3 V LVDS quad CMOS differential line driver |
| 02 | UT54LVDS031LV | Radiation hardened, 3 V LVDS quad CMOS differential line driver |
| 03 | UT54LVDS031LV | Radiation hardened, 3 V LVDS quad CMOS differential line driver |
| 04 | UT54LVDS031LVE | Radiation hardened, 3 V LVDS quad CMOS differential line driver, with enhanced AC parameters |
| 05 | UT54LVDS031LVE | Radiation hardened, 3 V LVDS quad CMOS differential line driver, with enhanced AC parameters |
| 06 | STLVDS31 | Radiation hardened, 3 V LVDS quad CMOS differential line driver |
| 07 | RHFLVDS31 | Radiation hardened, 3 V LVDS quad CMOS differential line driver, with enhanced AC parameters |
| 08 | RHFLVDS31 | Radiation hardened, 3 V LVDS quad CMOS differential line driver |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| F | GDFP2-F16 or CDFP3-F16 | 16 | Flat pack |
| X | GDFP1-G16 | 16 | Flat pack with gullwing leads |
| Y | CDFP4-F16 | 16 | Flat pack |
| Z | CDFP4-F16 | 16 | Flat pack with grounded lid |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage ($V_{CC}$) :
- Device types 01, 02, 03, 04, 05 ..... -0.3 V to +4 V
- Device type 06 ..... -0.3 V to +4.5 V
- Device types 07, 08 ..... -0.3 V to +4.8 V

Input voltage ($D_{IN}$) :
- Device types 01, 02, 03, 04, 05, 06 ..... -0.3 V to ($V_{CC}$ + 0.3 V) 2/
- Device types 07, 08 ..... -0.3 V to +4.8 V

Enable input voltage (EN, $\overline{EN}$ ) :
- Device types 01, 02, 03, 04, 05, 06 ..... -0.3 V to ($V_{CC}$ + 0.3 V)
- Device type 07, 08 ..... -0.3 V to +4.8 V

Output voltage ($D_{OUT+}$, $D_{OUT-}$) :
- Device types 01, 02, 03, 04, 05, 06 ..... -0.3 V to 3.9 V
- Device types 07, 08 ..... -0.3 V to 4.8 V

Storage temperature range ..... -65°C to +150°C

Maximum power dissipation ($P_D$):
- Cases F and X ..... 845 mW 3/
- Case Y ..... 1250 mW
- Case Z ..... 1.04 W

Lead temperature (soldering, 4 seconds) ..... +260°C

Junction temperature ($T_J$) ..... +150°C 4/

Thermal resistance, junction-to-case ($\theta_{JC}$):
- Cases F, X and Z ..... 22°C/W
- Case Y ..... 20°C/W

Thermal resistance, junction-to-ambient ($\theta_{JA}$):
- Cases F and X ..... 148°C/W
- Cases Y and Z ..... 120°C/W

1.4 Recommended operating conditions.

Supply voltage ($V_{CC}$) ..... 3.0 V to 3.6 V

Ambient operating temperature range ($T_A$) ..... -55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For device types 02, 03, 04, 05, and 06, maximum voltage on any pin during cold spare ($V_{DD}$ = $V_{SS}$) –0.3 V to 4.3 V.

3/ At $T_A$ > +25°C, the derating factor for cases F and X is 6.8 mW/°C and case Z is 8.32 mW/°C.

4/ For device types 02, 03, 04, 05, and 06, the maximum junction temperature may be increased to +175°C during burn-in and life test.

1.5 Radiation features.

Maximum total dose available:
Device types 02 and 04 (effective dose rate = 1 rad(Si)/s) ..... 1 Mrads(Si) 5/
Device types 03 and 05 (effective dose rate = 10 rad(Si)/s) ..... 100 krads(Si) 5/
Device type 06 (dose rate = 50 – 300 rads (Si)/s) ..... 100 krads(Si) 6/
Device types 07 and 08 (dose rate = 50 – 300 rads (Si)/s) ..... 300 krads(Si) 6/

Neutron irradiation :
Device types 02, 03, 04, and 05 only ..... $1 \times 10^{13}$ neutrons/cm$^2$ 7/

Single event effects (SEE):
Device types 02, 03, 04 and 05 only
No SEL at effective LET (see 4.4.4.4) ..... $\leq$ 100 MeV/mg/cm$^2$
Device types 07 and 08 only
No SEL at effective LET (see 4.4.4.4) ..... $\leq$ 120 MeV/mg/cm$^2$

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

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5/ Device types 02, 03, 04, 05 are irradiated at dose rate = 50 – 300 rads(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and are guaranteed to the maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad(Si)/s for device types 02 and 04 and 10 rads(Si)/s for device types 03 and 05 per MIL-STD-883, method 1019, condition A section 3.11.2. The total dose specification for these devices only applies to the specified effective dose rate, or lower, environment.
6/ The device types 06, 07 and 08 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A.
7/ Guaranteed, but not tested.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output voltage high | $V_{OH}$ | $R_L = 100\ \Omega$ | 1, 2, 3 | 01 | | 1.85 | V |
| | | | | 02, 03, 04, 05, 06, 07, 08 | | 1.65 | |
| Output voltage low | $V_{OL}$ | $R_L = 100\ \Omega$ | 1, 2, 3 | 01 | 0.9 | | V |
| | | | | 02, 03, 04, 05, 06, 07, 08 | 0.925 | | |
| Input voltage high | $V_{IH}$ | 3/ | 1, 2, 3 | 01, 02, 03, 04, 05, 06, 07, 08 | 2.0 | $V_{CC}$ | V |
| Input voltage low | $V_{IL}$ | 3/ | 1, 2, 3 | 01, 02, 03, 04, 05, 06, 07, 08 | GND | 0.8 | V |
| Input current | $I_{IN}$ | $V_{IN} = V_{CC}$, GND, 2.5 V or 0.4 V, $V_{CC} = 3.6$ V | 1, 2, 3 | 01 | -10 | 10 | µA |
| | | $V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.6$ V | | 02, 03, 04, 05 | -10 | 10 | |
| Input current low | $I_{IL}$ | $V_{IN}$ = GND, $V_{CC} = 3.6$ V | 1,2,3 | 06, 07, 08 | -10 | 10 | µA |
| Input current high | $I_{IH}$ | $V_{IN} = V_{CC}$ , $V_{CC} = 3.6$ V | 1,2,3 | 06, 07, 08 | -10 | 10 | µA |
| Differential output voltage | $V_{OD1}$ | $R_L = 100\ \Omega$ | 1, 2, 3 | 01 | 250 | 450 | mV |
| | | | | 02, 03, 04, 05, 06, 07, 08 | 250 | 400 | |
| Offset voltage | $V_{OS}$ | $R_L = 100\ \Omega$ | 1, 2, 3 | 01 | 1.125 | 1.625 | V |
| | | | | 02, 03, 04, 05, 06, 07, 08 | 1.125 | 1.45 | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Change in magnitude of $V_{OD1}$ for complementary output states | $DV_{OD1}$ | $R_L$ = 100 Ω | 1, 2, 3 | 01 | | 50 | mV |
| | | | | 02, 03, 04, 05, 06 | | 35 | |
| | | | | 07, 08 | | 10 | |
| Change in magnitude of $V_{OS}$ for complementary output states | $DV_{OS}$ | $R_L$ = 100 Ω | 1, 2, 3 | 01 | | 50 | mV |
| | | | | 02, 03, 04, 05, 06 | | 25 | |
| | | | | 07, 08 | | 15 | |
| Input clamp voltage | $V_I$ | $I_{IN}$ = -8 mA, $V_{CC}$ = 3.0 V | 1, 2, 3 | 01 | | -1.5 | V |
| | | $I_{IN}$ = +18 mA | | 02, 03, 04, 05, 06, 07, 08 | -1.5 | | |
| Output short circuit current | $I_{OS}$ | ENABLED, $D_{IN} = V_{CC}$, $D_{OUT}+$ = 0 V or $D_{IN}$ = GND, $D_{OUT}-$ = 0 V | 1, 2, 3 | 01 | -9.0 | | mA |
| | | | | 02, 03, 04, 05 | -9.0 | | |
| | | $D_{OUT}+$ = 0 V or $D_{IN}$ = GND, $D_{OUT}-$ = 0 V | | 06, 07, 08 | -9.0 | | |
| Power-off leakage | $I_{OFF}$ | $V_{OUT}$ = 0 V or 3.6 V, $V_{CC}$ = 0 V or $V_{CC}$ = open | 1, 2, 3 | 01 | -20 | 20 | μA |
| | | $V_{OUT}$ = 0 V or 3.6 V | | 06 | -20 | 20 | |
| | | $V_{IN}$ = 3.6 V, $V_{CC}$ = 0 V | | 02, 03, 04, 05, 06 | -20 | 20 | |
| | | | | 07, 08 | -10 | 10 | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output tri-state current | $I_O$ | EN = 0.8 V, $\overline{EN}$ = 2.0 V, $V_{OUT}$ = 0 V or $V_{CC}$, $V_{CC}$ = 3.6 V | 1, 2, 3 | 01 | -10 | 10 | µA |
| | | EN = 0.0 V, $\overline{EN}$ = 3.6 V, $V_{OUT}$ = 0 V or $V_{CC}$, $V_{CC}$ = 3.6 V | | 02, 03, 04, 05 | -10 | 10 | |
| Low impedance output current | $I_{OZL}$ | $V_{OUT}$ = 0 V, $V_{CC}$ = $V_{CC}$, EN = 0.0 V, $\overline{EN}$ = 3.6 V | 1,2,3 | 06, 07, 08 | -10 | 10 | µA |
| High impedance output current | $I_{OZH}$ | $V_{OUT}$ = 3.6 V, $V_{CC}$ = $V_{CC}$, EN = 0.0 V, $\overline{EN}$ = 3.6 V | 1,2,3 | 06, 07, 08 | -10 | 10 | µA |
| Drivers enabled supply current, no load | $I_{CC}$ | $D_{IN}$ = $V_{CC}$ or GND | 1, 2, 3 | 01,06 | | 18 | mA |
| Drivers enabled supply current, loaded | $I_{CCL}$ | $R_L$ = 100 Ω all channels, $D_{IN}$ = $V_{CC}$ or GND all inputs | 1, 2, 3 | 01, 08 | | 35 | mA |
| | | | | 02, 03, 07 | | 20 | |
| | | | | 04, 05 | | 18 | |
| | | | | 06 | | 25 | |
| Drivers disabled supply current, loaded or no load | $I_{CCZ}$ | $D_{IN}$ = $V_{CC}$ or GND, EN = GND, $\overline{EN}$ = $V_{CC}$ | 1, 2, 3 | 01 | | 12 | mA |
| | | | | 02, 03, 06, 07, 08 | | 4 | |
| | | | | 04, 05 | | 3.0 | |
| Functional test | FT | See 4.4.1c | 7, 8 | All | | | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Differential propagation delay, high to low | $t_{PHLD}$ | See figure 2 | 9, 10, 11 | 01, 08 | 0.3 | 3.5 | ns |
| | | | | 02, 03, 06 | 0.3 | 3.0 | |
| | | | | 04, 05 | 0.8 | 1.5 | |
| | | | | 07 | 0.5 | 1.5 | |
| Differential propagation delay, low to high | $t_{PLHD}$ | See figure 2 | 9, 10, 11 | 01, 08 | 0.3 | 3.5 | ns |
| | | | | 02, 03, 06 | 0.3 | 3.0 | |
| | | | | 04, 05 | 0.8 | 1.5 | |
| | | | | 07 | 0.5 | 1.5 | |
| Differential skew | $t_{SKD}$ | | 9, 10, 11 | 01 | | 1.5 | ns |
| | | | | 02, 03, 06 | | 0.4 | |
| | | | | 04, 05 | | 0.31 | |
| | | | | 07 | | 0.3 | |
| | | | | 08 | | 0.6 | |
| Channel to channel skew | $t_{SK1}$ | 4/ | 9, 10, 11 | 01 | | 1.75 | ns |
| | | | | 02, 03, 06 | | 0.5 | |
| | | | | 04, 05, 07 | | 0.28 | |
| | | | | 08 | | 0.6 | |
| Chip to chip skew | $t_{SK2}$ | 5/ | 9, 10, 11 | 01 | | 3.2 | ns |
| | | | | 02, 03, 06 | | 2.7 | |
| | | | | 04, 05, 07 | | 0.7 | |
| | | | | 08 | | 3.0 | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Disable time high to Z | $t_{PHZ}$ | | 9, 10, 11 | 02, 03, 06 | | 5.0 | ns |
| | | | | 04, 05, 07 | | 2.8 | |
| | | | | 08 | | 12 | |
| Disable time low to Z | $t_{PLZ}$ | | 9, 10, 11 | 02, 03, 06 | | 5.0 | ns |
| | | | | 04, 05, 07 | | 2.8 | |
| | | | | 08 | | 12 | |
| Enable time Z to high | $t_{PZH}$ | | 9, 10, 11 | 02, 03 | | 7.0 | ns |
| | | | | 04, 05, 07 | | 2.5 | |
| | | | | 06 | | 8.5 | |
| | | | | 08 | | 12 | |
| Enable time Z to low | $t_{PZL}$ | | 9, 10, 11 | 02, 03 | | 7.0 | ns |
| | | | | 04, 05, 07 | | 2.5 | |
| | | | | 06 | | 8.5 | |
| | | | | 08 | | 12 | |

1/ Device types 02 and 04 supplied to this drawing will meet all levels M, D, P, L, R, F, G, H of irradiation. However, device types 02 and 04 are only tested at the 'H' level. Device types 03, 05, and 06 supplied to this drawing will meet all levels M, D, P, L, R of irradiation. However, device types 03, 05, and 06 are only tested at the 'R' level. Device type 07 supplied to this drawing will meet all levels M, D, P, L, R, F of irradiation. However, device types 07 and 08 are only tested at the L, R, and F level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

2/ Unless otherwise specified, Device type 01 DC parameters: $V_{CC} = 3.0$ V and 3.6 V; AC parameters: $V_{CC} = 3.0$ V, 3.3 V and 3.6 V, $R_L = 100\Omega$ between outputs, $C_L = 20$ pF each output to GND.
Device types 02, 03, 04, 05, 06, 07, 08 DC parameters: $V_{CC} = 3.0$ V and 3.6 V, $R_L = 100\Omega$ between outputs, $C_L = 10$ pF each output to GND.

3/ The $V_{IH}$ and $V_{IL}$ tests are not required and shall be applied as forcing functions for the $V_{OL}$ and $V_{OH}$ tests.

4/ Channel to channel skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.

5/ Chip to chip skew is defined as the difference between the minimum and maximum specified differential propagation delays.

TABLE IB. SEP test limits. 1/ 2/

| Device types | SEP | Temperature ($T_C$) | Bias $V_{CC}$ = 3.0 V for latch up (SEL) test no latch up effective linear energy transfer (LET) |
|---|---|---|---|
| 02, 03, 04, 05 | No SEL | +125°C | LET $\leq$ 100 MeV-cm$^2$/mg |
| 07, 08 | No SEL | +125°C | LET $\leq$ 120 MeV-cm$^2$/mg |

1/ For SEP test conditions, see 4.4.4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

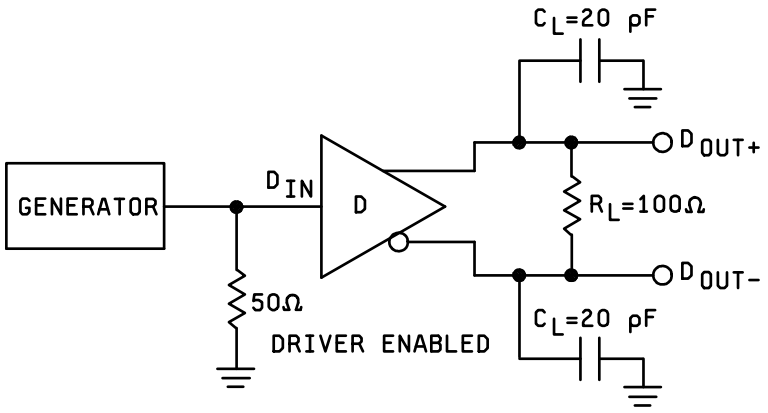
a. Tests shall be as specified in table IIA herein.

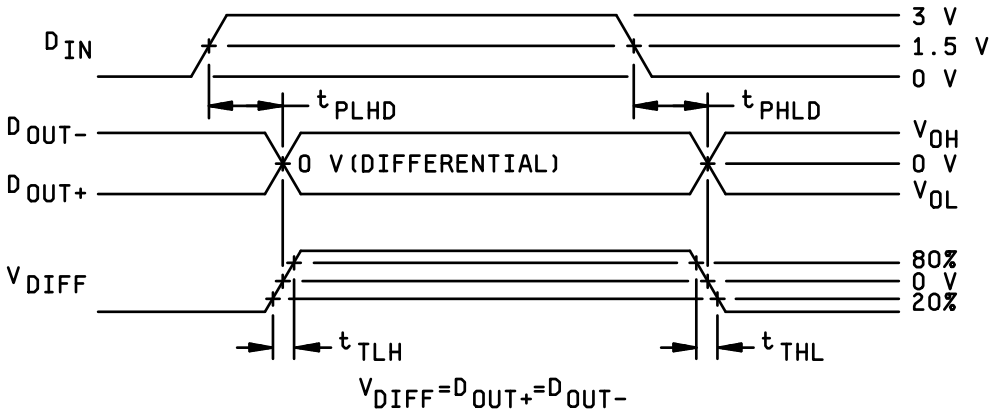
b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

| Device types | 01, 02, 03, 04, 05, 06, 07, 08 |
|---|---|
| Case outlines | F, X, Y and Z |
| Terminal number | Terminal symbol |
| 1 | INPUT A |
| 2 | OUTPUT A+ |
| 3 | OUTPUT A- |
| 4 | ENABLE |
| 5 | OUTPUT B- |
| 6 | OUTPUT B+ |
| 7 | INPUT B |
| 8 | GND |
| 9 | INPUT C |
| 10 | OUTPUT C+ |
| 11 | OUTPUT C- |
| 12 | $\overline{\text{ENABLE}}$ |
| 13 | OUTPUT D- |
| 14 | OUTPUT D+ |
| 15 | INPUT D |
| 16 | $V_{CC}$ |

FIGURE 1. Terminal connections.

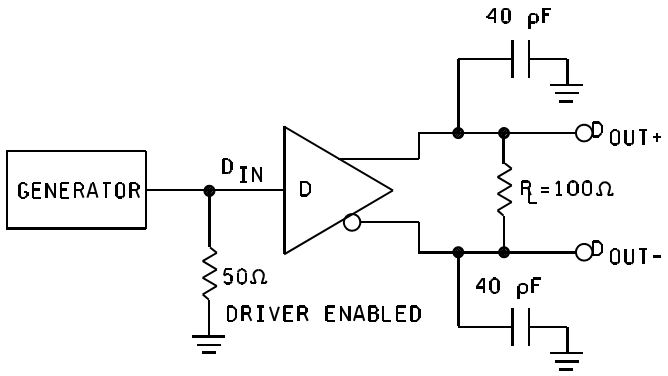


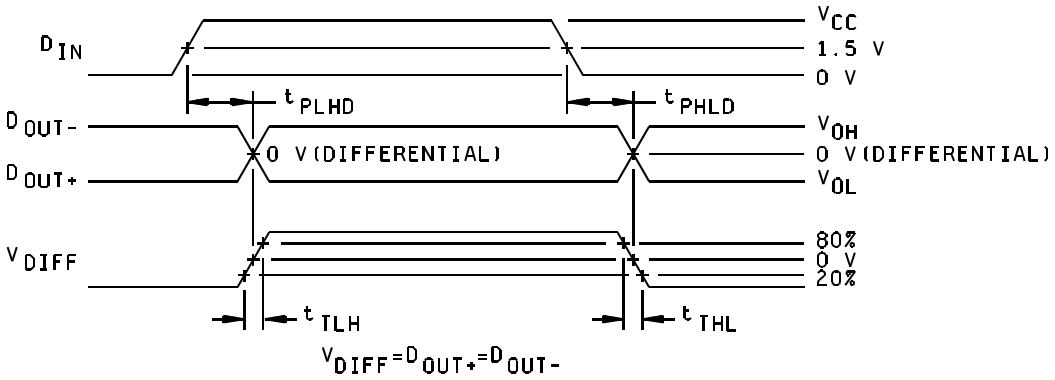




NOTE: Generator characteristics:
f = 1 MHz
$Z_O = 50\Omega$
$t_r$ = 1 ns
$t_f$ = 1 ns

(Device type 01)

FIGURE 2. Propagation delay waveforms and test circuit.




(Device types 02, 03, 04, 05, 06 with $C_L$ = 40 pF. Device types 07 and 08 with $C_L$ = 10 pF).

FIGURE 2. Propagation delay waveforms and test circuit – continued.

TABLE IIA. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|
| | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | --- | 1 |
| Final electrical parameters (see 4.2) | 1, 2, 3, 7, 1/ 8, 9, 10, 11 | 1, 2, 3, 2/ 3/ 7, 8, 9, 10, 11 |
| Group A test requirements (see 4.4) | 1, 2, 3, 7, 8, 9, 10, 11 | 1, 2, 3, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3, 7, 8, 3/ 9, 10, 11 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. $T_A$ = +25°C. 1/ 2/

| Device type | Parameters | Symbol | Delta limits |
|---|---|---|---|
| 02, 03, 04, 05 | Drivers enabled supply current, loaded | $I_{CCL}$ | ±1.8 mA |
| 06 | Input current low | $I_{IL}$ | ±150 nA |
| | Input current high | $I_{IH}$ | ±150 nA |
| | Low impedance output current | $I_{OZL}$ | ±1 µA |
| | High impedance output current | $I_{OZH}$ | ±1 µA |
| | Drivers enabled supply current, no loads | $I_{CC}$ | ±1 mA |
| 06, 07, 08 | Drivers enabled supply current, loaded | $I_{CCL}$ | ±1 mA |
| | Drivers disabled supply current, loaded or no load | $I_{CCZ}$ | ±0.4 mA |

1/ Deltas are performed at room temperature.
2/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. For device types 02, 03, 04, 05, 06, 07, and 08 only, total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and as specified herein (see 1.5).

4.4.4.1.1 Accelerated annealing test. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in Table IIA herein at $T_A$ = +25 ºC ±5 ºC after an exposure of 2 x $10^{12}$ neutrons/$cm^2$ (minimum).

4.4.4.3 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (See 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ $10^7$ ions/$cm^2$.

c. The flux shall be between $10^2$ and $10^5$ ions/$cm^2$/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be 25°C for the latchup measurements.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b. Occurrence of upsets (SEU).

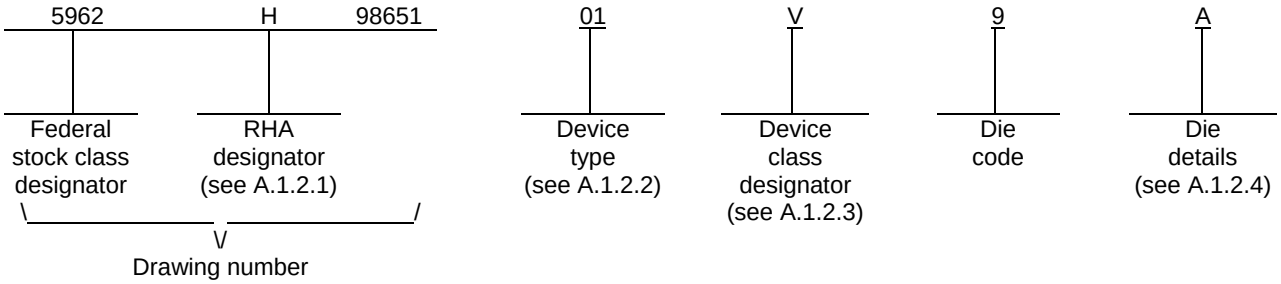
c. Occurrence of latchup (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-98651

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:




A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

| Device type | Generic number | Circuit function |
|---|---|---|
| 02 | UT54LVDS031LV | Radiation hardened (dose rate ≤ 1 rad(Si)/s), 3 V LVDS quad CMOS differential line driver |
| 03 | UT54LVDS031LV | Radiation hardened (dose rate ≤ 10 rad(Si)/s), 3 V LVDS quad CMOS differential line driver |
| 04 | UT54LVDS031LVE | Radiation hardened (dose rate ≤ 1 rad(Si)/s), 3 V LVDS quad CMOS differential line driver, with enhanced AC parameters |
| 05 | UT54LVDS031LVE | Radiation hardened (dose rate ≤ 10 rad(Si)/s), 3 V LVDS quad CMOS differential line driver, with enhanced AC parameters |
| 07 | RHFLVDS31 | Radiation hardened 3 V LVDS quad CMOS differential line driver, with enhanced AC parameters |
| 08 | RHFLVDS31 | Radiation hardened 3 V LVDS quad CMOS differential line driver |

A.1.2.3 Device class designator.

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to the die requirements of MIL-PRF-38535 |

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

| Die type | Figure number |
|---|---|
| 02, 03, 04, 05 | A-1 |
| 07, 08 | A-2 |

A.1.2.4.2 Die bonding pad locations and electrical functions.

| Die type | Figure number |
|---|---|
| 02, 03, 04, 05 | A-1 |
| 07, 08 | A-2 |

A.1.2.4.3 Interface materials.

| Die type | Figure number |
|---|---|
| 02, 03, 04, 05 | A-1 |
| 07, 08 | A-2 |

A.1.2.4.4 Assembly related information.

| Die type | Figure number |
|---|---|
| 02, 03, 04, 05 | A-1 |
| 07, 08 | A-2 |

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3, and 4.4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

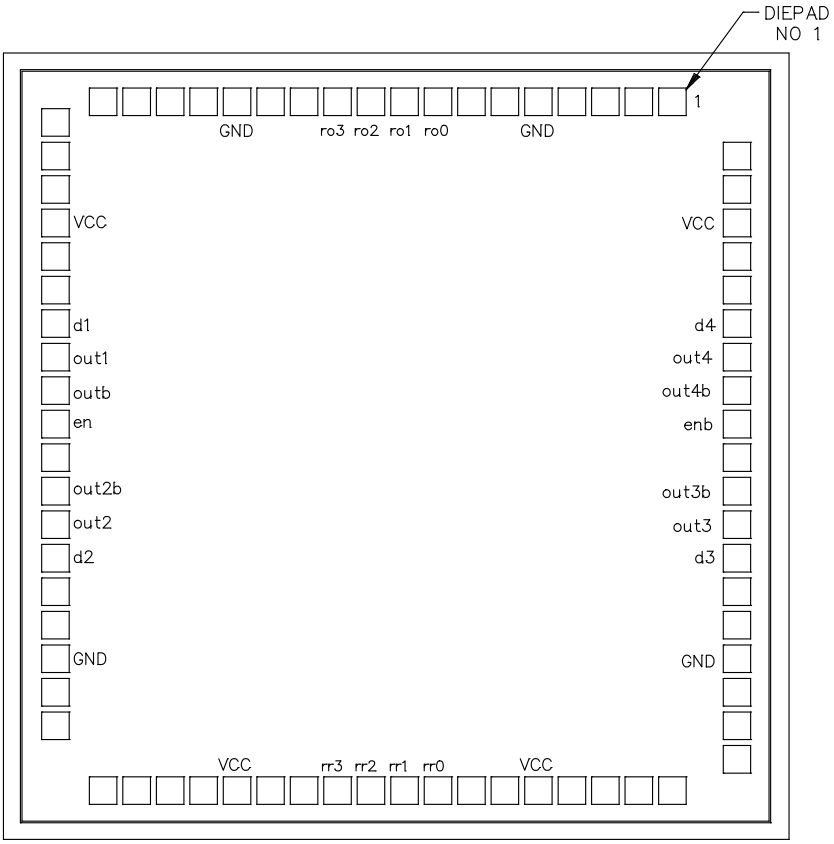
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.




NOTE: On a wafer lot basis, the die manufacturer will determine the bonding for die pads ro3, r02, ro1, ro0, rr3, rr2, rr1, rr0. These pads must be bonded to $V_{CC}$ or GND per the die manufacturer provided bonding instructions. Die pad one located counter clockwise next to fiducial "1" die marking. Die pads count counter clockwise with every fifth die pad fiducially marked.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 0.085 inch x 0.085 inch
Die thickness: 17.5 +/-0.5 mils

Interface materials.
Top metallization: Al 99.5%, Cu 0.5% + barrier + W plugs
Backside metallization: None

Glassivation.
Type: $Sio_2/Si_3N_4$
Thickness: 2600 Å < Thickness < 10,000 Å

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: $V_{SS}$/Ground
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

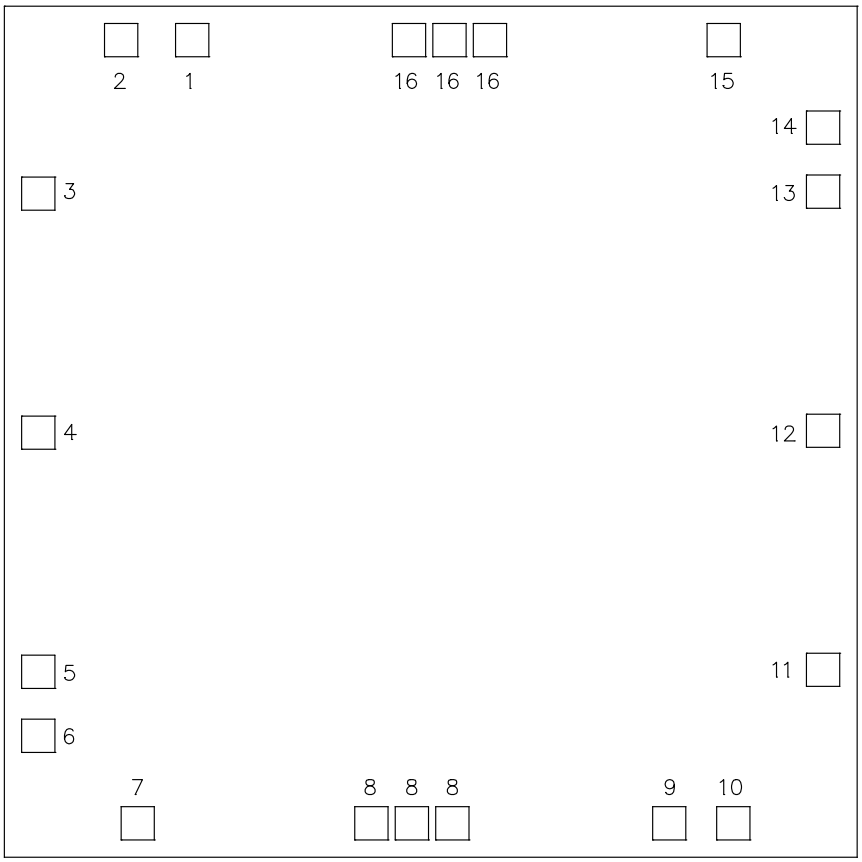
Units: Mils
Origin (0,0) = die Center

| Die Pad | X center | Y center | Signal Name |
|---|---|---|---|
| 1 | 29.3 | 35.9 | N/C |
| 2 | 25.7 | 35.9 | N/C |
| 3 | 22.2 | 35.9 | N/C |
| 4 | 18.6 | 35.9 | N/C |
| 5 | 15.1 | 35.9 | GND |
| 6 | 11.5 | 35.9 | N/C |
| 7 | 8.0 | 35.9 | N/C |
| 8 | 4.5 | 35.9 | Note 1 |
| 9 | 0.9 | 35.9 | Note 1 |
| 10 | -2.6 | 35.9 | Note 1 |
| 11 | -6.2 | 35.9 | Note 1 |
| 12 | -9.7 | 35.9 | N/C |
| 13 | -13.3 | 35.9 | N/C |
| 14 | -16.8 | 35.9 | GND |
| 15 | -20.4 | 35.9 | N/C |
| 16 | -23.9 | 35.9 | N/C |
| 17 | -27.4 | 35.9 | N/C |
| 18 | -31.0 | 35.9 | N/C |
| 19 | -35.9 | 34.2 | N/C |
| 20 | -35.9 | 30.7 | N/C |
| 21 | -35.9 | 27.1 | N/C |
| 22 | -35.9 | 23.6 | VDD |
| 23 | -35.9 | 20.0 | N/C |
| 24 | -35.9 | 16.5 | N/C |
| 25 | -35.9 | 12.9 | DIN1 |
| 26 | -35.9 | 9.4 | DOUT1+ |
| 27 | -35.9 | 5.9 | DOUT1- |
| 28 | -35.9 | 2.3 | EN |
| 29 | -35.9 | -1.2 | N/C |
| 30 | -35.9 | -4.8 | DOUT2- |
| 31 | -35.9 | -8.3 | DOUT2+ |
| 32 | -35.9 | -11.9 | DIN2 |
| 33 | -35.9 | -15.4 | N/C |
| 34 | -35.9 | -19.0 | N/C |
| 35 | -35.9 | -22.5 | VSS |
| 36 | -35.9 | -26.0 | N/C |
| 37 | -35.9 | -29.6 | N/C |

| Die Pad | X center | Y center | Signal Name |
|---|---|---|---|
| 38 | -31.0 | -35.9 | N/C |
| 39 | -27.4 | -35.9 | N/C |
| 40 | -23.9 | -35.9 | N/C |
| 41 | -20.4 | -35.9 | N/C |
| 42 | -16.8 | -35.9 | VDD |
| 43 | -13.3 | -35.9 | N/C |
| 44 | -9.7 | -35.9 | N/C |
| 45 | -6.2 | -35.9 | Note 1 |
| 46 | -2.6 | -35.9 | Note 1 |
| 47 | 0.9 | -35.9 | Note 1 |
| 48 | 4.5 | -35.9 | Note 1 |
| 49 | 8.0 | -35.9 | N/C |
| 50 | 11.5 | -35.9 | N/C |
| 51 | 15.1 | -35.9 | VDD |
| 52 | 18.6 | -35.9 | N/C |
| 53 | 22.2 | -35.9 | N/C |
| 54 | 25.7 | -35.9 | N/C |
| 55 | 29.3 | -35.9 | N/C |
| 56 | 35.9 | -33.1 | N/C |
| 57 | 35.9 | -29.6 | N/C |
| 58 | 35.9 | -26.0 | N/C |
| 59 | 35.9 | -22.5 | VSS |
| 60 | 35.9 | -19.0 | N/C |
| 61 | 35.9 | -15.4 | N/C |
| 62 | 35.9 | -11.9 | DIN3 |
| 63 | 35.9 | -8.3 | DOUT3+ |
| 64 | 35.9 | -4.8 | DOUT3- |
| 65 | 35.9 | -1.2 | N/C |
| 66 | 35.9 | 2.3 | EN/ |
| 67 | 35.9 | 5.9 | DOUT4- |
| 68 | 35.9 | 9.4 | DOUT4+ |
| 69 | 35.9 | 12.9 | DIN4 |
| 70 | 35.9 | 16.5 | N/C |
| 71 | 35.9 | 20.0 | N/C |
| 72 | 35.9 | 23.6 | VDD |
| 73 | 35.9 | 27.1 | N/C |
| 74 | 35.9 | 30.7 | N/C |

NOTE 1: Contact factory for bonding information on these pads.

FIGURE A-1. Die bonding pad locations and electrical functions – continued.




Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 0.0826 inch x 0.0826 inch
Die thickness: 280 μm ± 25 μm

Interface materials.
Top metallization: Al 99.5%, Cu 0.5%
Backside metallization: None

Glassivation.
Type: Phosphorous Silicon Glass (PSG) 5000 Å, Nitride (SiN) 6000 Å

Substrate: Silicon

Assembly related information.
Substrate potential: $V_{SS}$/Ground
Special assembly instructions: None

FIGURE A-2. Die bonding pad locations and electrical functions.

| Die pad | Signal name | Pad placements | | Pad dimensions | |
|---|---|---|---|---|---|
| | | X = | Y = | X = | Y = |
| 1 | A1 | -577.46 | 980.0 | 80.0 | 80.0 |
| 2 | Y1 | -737.5 | 980.0 | 80.0 | 80.0 |
| 3 | Z1 | -908.0 | 595.88 | 80.0 | 80.0 |
| 4 | G | -980.0 | 0.23 | 80.0 | 80.0 |
| 5 | Z2 | -980.0 | -595.44 | 80.0 | 80.0 |
| 6 | Y2 | -980.0 | -745.88 | 80.0 | 80.0 |
| 7 | A2 | -737.5 | -980.0 | 80.0 | 80.0 |
| 8 | AGND | -153.45 | -980.0 | 80.0 | 80.0 |
| 8 | AGND | -53.45 | -980.0 | 80.0 | 80.0 |
| 8 | AGND | 46.55 | -980.0 | 80.0 | 80.0 |
| 9 | A3 | 577.46 | -980.0 | 80.0 | 80.0 |
| 10 | Y3 | 737.5 | -980.0 | 80.0 | 80.0 |
| 11 | Z3 | 980.0 | -595.44 | 80.0 | 80.0 |
| 12 | Gb | 980.0 | -95.15 | 80.0 | 80.0 |
| 13 | Z4 | 980.0 | 595.88 | 80.0 | 80.0 |
| 14 | Y4 | 980.0 | 745.88 | 80.0 | 80.0 |
| 15 | A4 | 737.5 | 980.0 | 80.0 | 80.0 |
| 16 | VCCA | 160.95 | 980.0 | 80.0 | 80.0 |
| 16 | VCCA | 60.95 | 980.0 | 80.0 | 80.0 |
| 16 | VCCA | -39.05 | 980.0 | 80.0 | 80.0 |

NOTES:
1. All dimensions are in microns.
2. Pad placement values correspond to each pad center coordinates.
3. Pad placement origin is the center of the die.

FIGURE A-2. Die bonding pad locations and electrical functions – continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-10-22

Approved sources of supply for SMD 5962-98651 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9865101QFA | 27014 | DS90LV031AW-QML |
| 5962-9865101QXA | 3/ | DS90LV031AWGQML |
| 5962H9865102Q9A | 65342 | UT54LVDS031LV_QDIE |
| 5962H9865102QYA | 65342 | UT54LVDS031LVUCA |
| 5962H9865102QYC | 65342 | UT54LVDS031LVUCC |
| 5962H9865102V9A | 65342 | UT54LVDS031LV_VDIE |
| 5962H9865102VYA | 65342 | UT54LVDS031LVUCA |
| 5962H9865102VYC | 65342 | UT54LVDS031LVUCC |
| 5962R9865103Q9A | 65342 | UT54LVDS031LV_QDIE |
| 5962R9865103QYA | 65342 | UT54LVDS031LVUCA |
| 5962R9865103QYC | 65342 | UT54LVDS031LVUCC |
| 5962R9865103V9A | 65342 | UT54LVDS031LV_VDIE |
| 5962R9865103VYA | 65342 | UT54LVDS031LVUCA |
| 5962R9865103VYC | 65342 | UT54LVDS031LVUCC |
| 5962H9865104Q9A | 65342 | UT54LVDS031LVE_QDIE |
| 5962H9865104QYA | 65342 | UT54LVDS031LVEUCA |
| 5962H9865104QYC | 65342 | UT54LVDS031LVEUCC |
| 5962H9865104V9A | 65342 | UT54LVDS031LVE_VDIE |
| 5962H9865104VYA | 65342 | UT54LVDS031LVEUCA |
| 5962H9865104VYC | 65342 | UT54LVDS031LVEUCC |
| 5962R9865105Q9A | 65342 | UT54LVDS031LVE_QDIE |
| 5962R9865105QYA | 65342 | UT54LVDS031LVEUCA |
| 5962R9865105QYC | 65342 | UT54LVDS031LVEUCC |
| 5962R9865105V9A | 65342 | UT54LVDS031LVE_VDIE |
| 5962R9865105VYA | 65342 | UT54LVDS031LVEUCA |
| 5962R9865105VYC | 65342 | UT54LVDS031LVEUCC |

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962R9865106VYC | F8859 | RH-LVDS31K |
| 5962F9865107VZC | F8859 | RHFLVDS31AK01V |
| 5962F9865107VZA | F8859 | RHFLVDS31AK02V |
| 5962F9865107V9A | F8859 | RHFLVDS31AD2V |
| 5962F9865108VZC | F8859 | RHFLVDS315K01V |
| 5962F9865108VZA | F8859 | RHFLVDS315K02V |
| 5962F9865108V9A | F8859 | RHFLVDS315D2V |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 27014 | National Semiconductor<br>2900 Semiconductor Dr<br>PO Box 58090<br>Santa Clara, CA 95052-8090 |
| 65342 | Aeroflex Colorado Springs, Inc.<br>4350 Centennial Blvd.<br>Colorado Springs, CO 80907-3486 |
| F8859 | ST Microelectronics<br>3 rue de Suisse<br>CS 60816<br>35208 RENNES cedex2-FRANCE |