



74LCX373

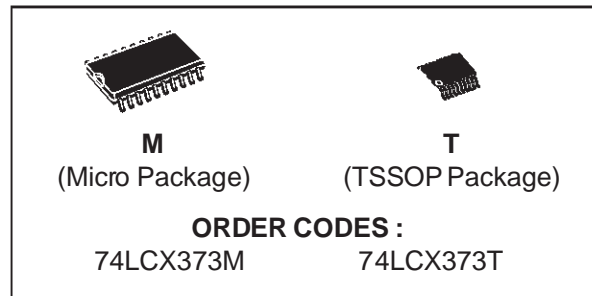
OCTAL D-TYPE LATCH NON INVERTING (3-STATE) WITH 5V TOLERANT INPUTS AND OUTPUTS

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED: $t_{PD} = 8 \text{ ns (MAX.)}$ at $V_{CC} = 3V$
- POWER-DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24 \text{ mA (MIN)}$
- PCI BUS LEVELS GUARANTEED AT 24mA
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2.0V \text{ to } 3.6V$ (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 373
- LATCH-UP PERFORMANCE EXCEEDS 500mA
- ESD PERFORMANCE:
HBM > 2000V; MM > 200V

DESCRIPTION

The LCX373 is a low VOLTAGE CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs.

These 8 bit D-Type latches are controlled by a



latch enable input (LE) and an output enable input (\overline{OE}).

While the LE input is held at a high level, the Q outputs will follow the data input precisely.

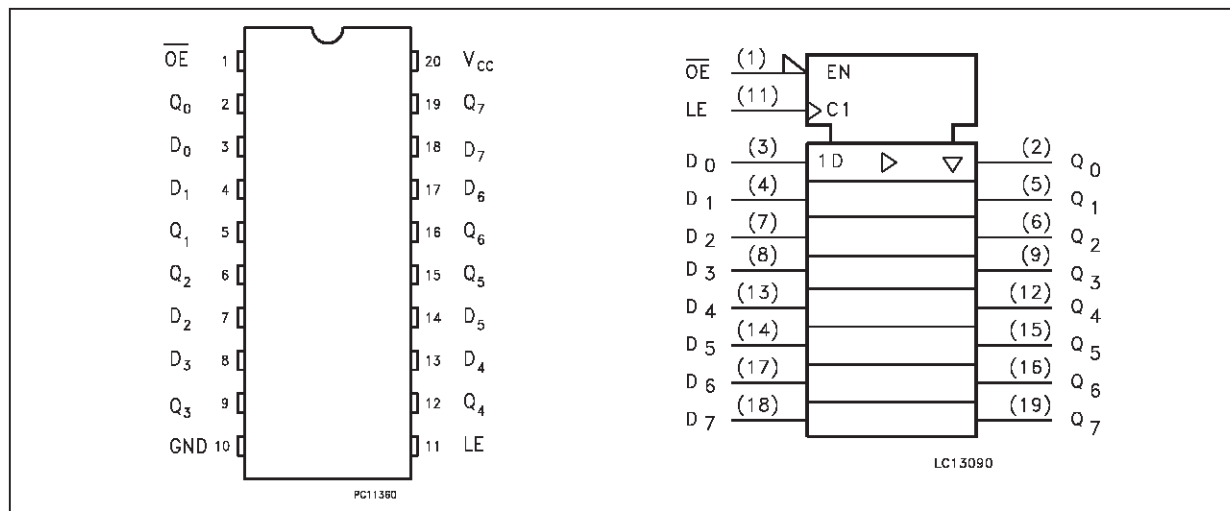
When the LE is taken low, the Q outputs will be latched precisely at the logic level of D input data.

While the \overline{OE} input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

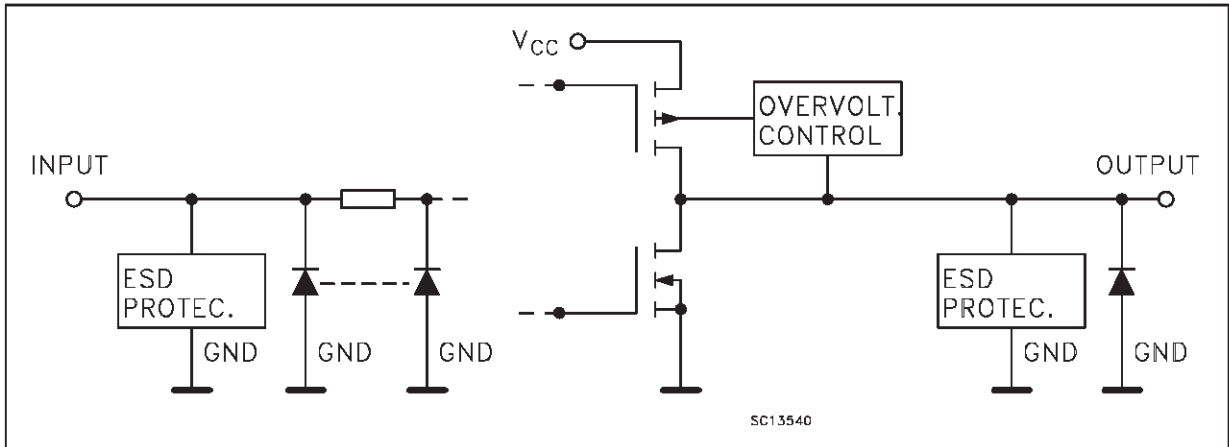
It has same speed performance at 3.3V than 5V, AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

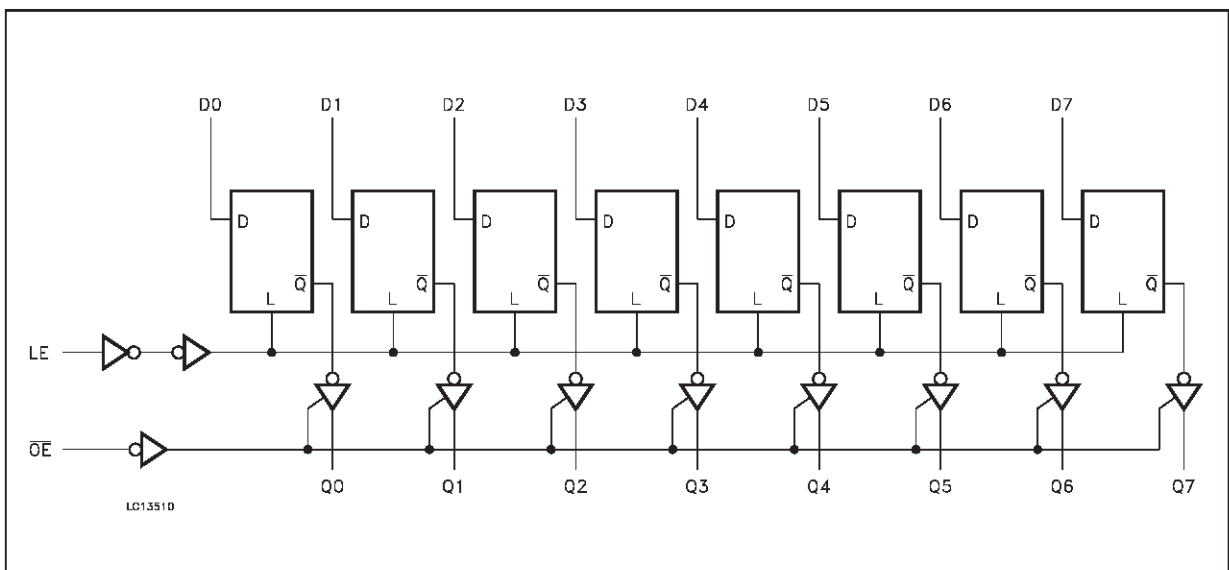
PIN No	SYMBOL	NAME AND FUNCTION
1	\overline{OE}	3 State Output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 17, 18	D0 to D7	Data Inputs
3, 4, 7, 8, 13, 14, 17, 18	Q0 to Q7	3 State Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS
\overline{OE}	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE *
L	H	L	L
L	H	H	H

X: Don't care
 Z: High impedance
 * Q output are latched at the time when the LE input is taken LOW.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage (OFF state)	-0.5 to +7.0	V
V _O	DC Output Voltage (High or Low State) (note1)	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 50	mA
I _{OK}	DC Output Diode Current (note2)	± 50	mA
I _O	DC Output Source/Sink Current	± 50	mA
I _{CC}	DC Supply Current per Supply Pin	± 100	mA
I _{GND}	DC Ground Current per Supply Pin	± 100	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

1) I_O absolute maximum rating must be observed

2) V_O < GND, V_O > V_{CC}

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage (note 1)	2.0 to 3.6	V
V _I	Input Voltage	0 to 5.5	V
V _O	Output Voltage (OFF state)	0 to 5.5	V
V _O	Output Voltage (High or Low State)	0 to V _{CC}	V
I _{OH} , I _{OL}	High or Low Level Output Current (V _{CC} = 3.0 to 3.6V)	± 24	mA
I _{OH} , I _{OL}	High or Low Level Output Current (V _{CC} = 2.7 to 3.0V)	± 12	mA
T _{op}	Operating Temperature:	-40 to +85	°C
dt/dv	Input Transition Rise or Fall Rate (V _{CC} = 3.0V) (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.5V to 3.6V

2) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value		Unit
		V _{CC} (V)		-40 to 85 °C		
				Min.	Max.	
V _{IH}	High Level Input Voltage	2.7 to 3.6		2.0		V
V _{IL}	Low Level Input Voltage				0.8	V
V _{OH}	High Level Output Voltage	2.7 to 3.6	V _I = V _{IH} or V _{IL}	I _O =-100 μA	V _{CC} -0.2	V
		2.7		I _O =-12 mA	2.2	
		3.0		I _O =-18 mA	2.4	
				I _O =-24 mA	2.2	
V _{OL}	Low Level Output Voltage	2.7 to 3.6	V _I = V _{IH} or V _{IL}	I _O =100 μA	0.2	V
		2.7		I _O =12 mA	0.4	
		3.0		I _O =16 mA	0.4	
		3.0		I _O =24 mA	0.55	
I _I	Input Leakage Current	2.7 to 3.6	V _I = 0 to 5.5 V		±5	μA
I _{OZ}	3 State Output Leakage Current	2.7 to 3.6	V _I = V _{IH} or V _{IL} V _O = 0 to 5.5V		±5	μA
I _{off}	Power Off Leakage Current	0	V _I or V _O = 5.5V		100	μA
I _{CC}	Quiescent Supply Current	2.7 to 3.6	V _I = V _{CC} or GND		10	μA
			V _I or V _O = 3.6 to 5.5V		±10	
ΔI _{CC}	ICC incr. per input	2.7 to 3.6	V _{IH} = V _{CC} -0.6V		500	μA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1)	3.3	C _L = 50 pF V _{IL} = 0 V V _{IH} = 3.3V		0.8		V
V _{OLV}					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 2.5 \text{ ns}$)

Symbol	Parameter	Test Condition		Value		Unit
		V_{CC} (V)	Waveform	-40 to 85 °C		
				Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time Dn to Qn	2.7 3.0 to 3.6	3	1.5 1.5	9.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay Time LE to Qn	2.7 3.0 to 3.6	1	1.5 1.5	9.5 8.5	ns
t_{PZL} t_{PZH}	Output Enable Time to HIGH and LOW level	2.7 3.0 to 3.6	2	1.5 1.5	9.5 8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time from HIGH and LOW level	2.7 3.0 to 3.6	2	1.5 1.5	8.5 7.5	ns
t_s	Setup Time, HIGH or LOW level Dn to LE	2.7 3.0 to 3.6	1	2.5 2.5		ns
t_h	Hold Time, HIGH or LOW level Dn to LE	2.7 3.0 to 3.6	1	1.5 1.5		ns
t_w	LE Pulse Width, HIGH	2.7 3.0 to 3.6	1	3.3 3.3		ns
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1, 2)	3.0 to 3.6			1.0	ns

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHr}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLr}|$)

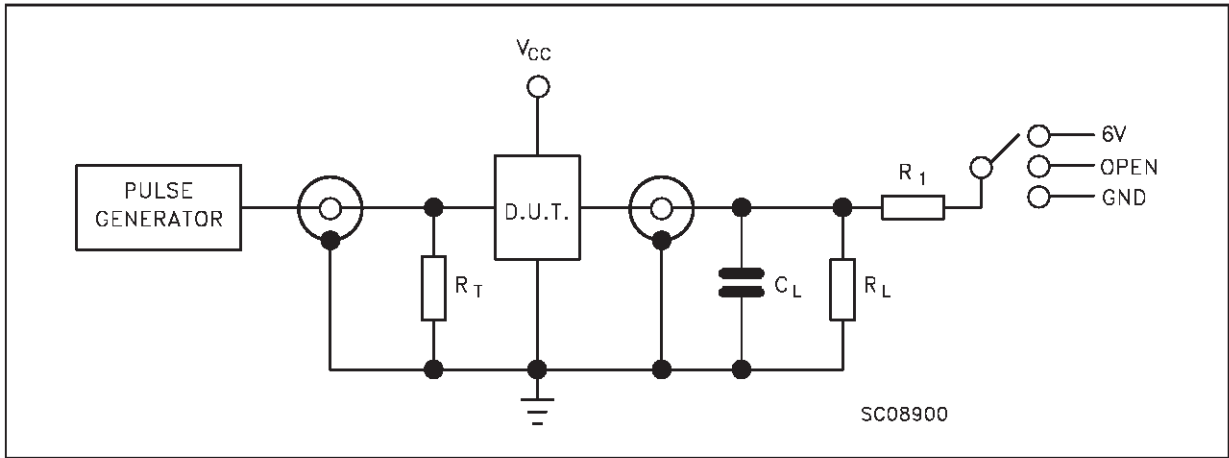
2) Parameter guaranteed by design

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V_{CC} (V)		$T_A = 25 \text{ °C}$			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance	3.3	$V_{IN} = 0 \text{ to } V_{CC}$		6		pF
C_{OUT}	Output Capacitance	3.3	$V_{IN} = 0 \text{ to } V_{CC}$		12		pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	$f_{IN} = 10\text{MHz}$ $V_{IN} = 0 \text{ or } V_{CC}$		50		pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per L/natcht)

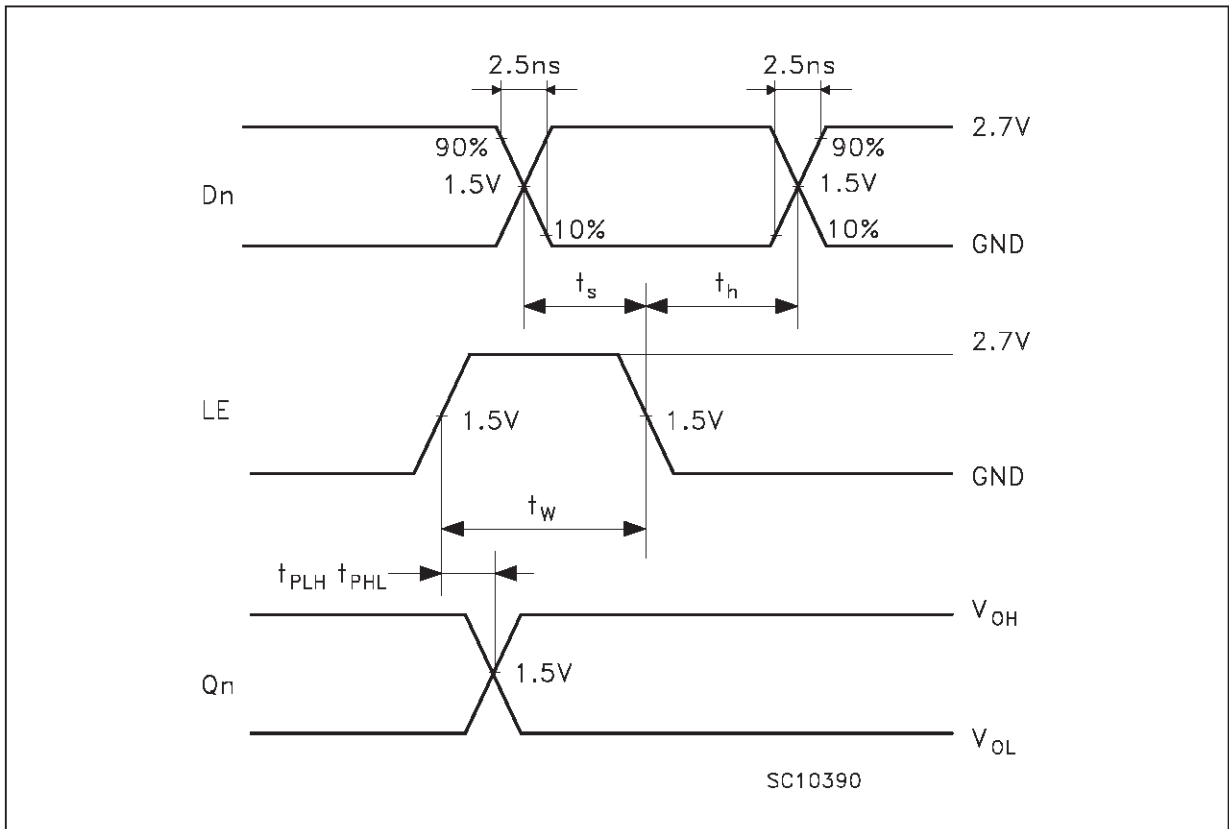
TEST CIRCUIT

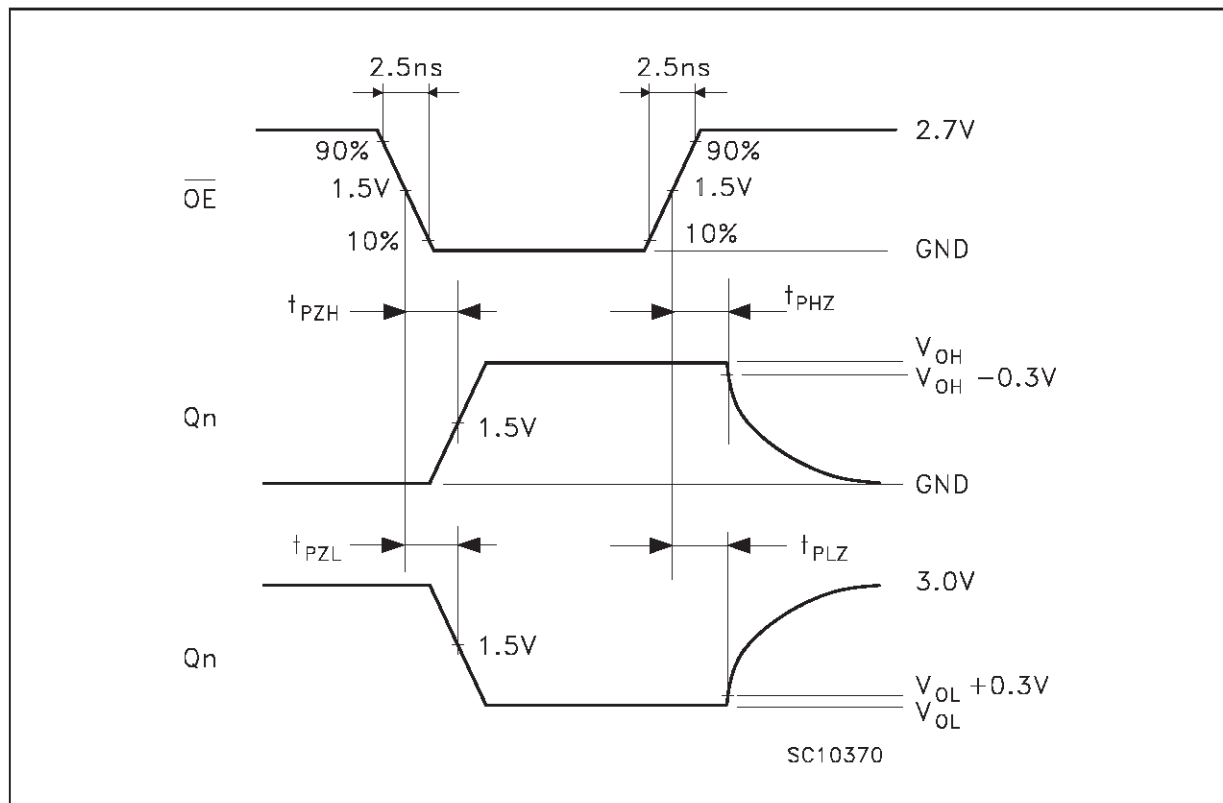
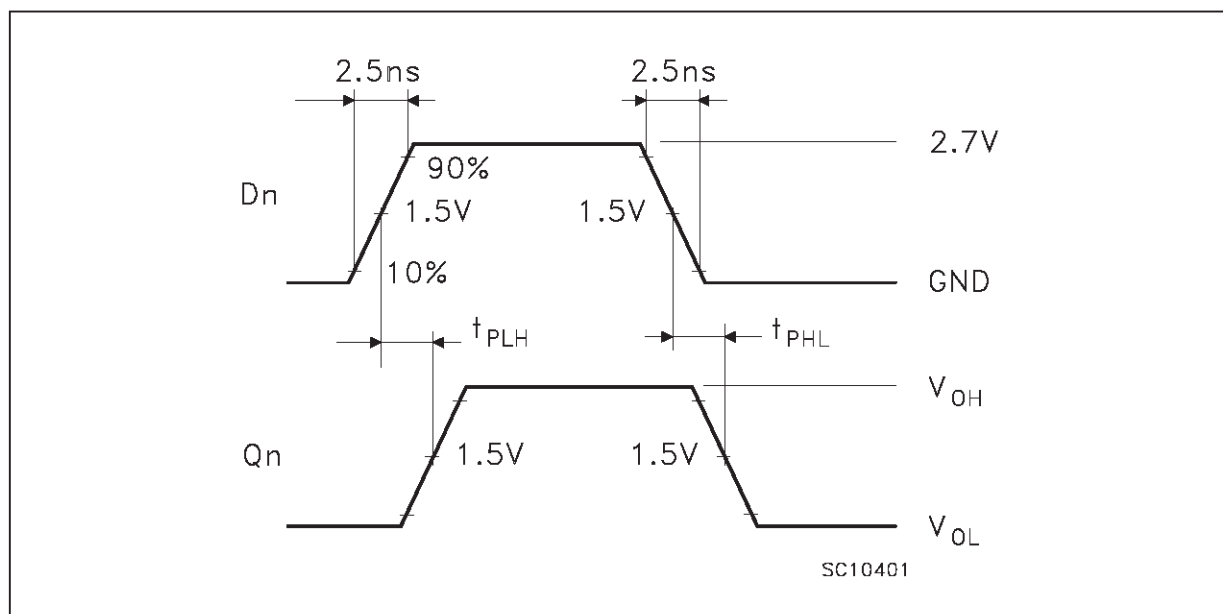


TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V
t_{PZH} , t_{PHZ}	GND

C_L = 50 pF or equivalent (includes jig and probe capacitance)
 R_L = R_1 = 500Ω or equivalent
 R_T = Z_{out} of pulse generator (typically 50Ω)

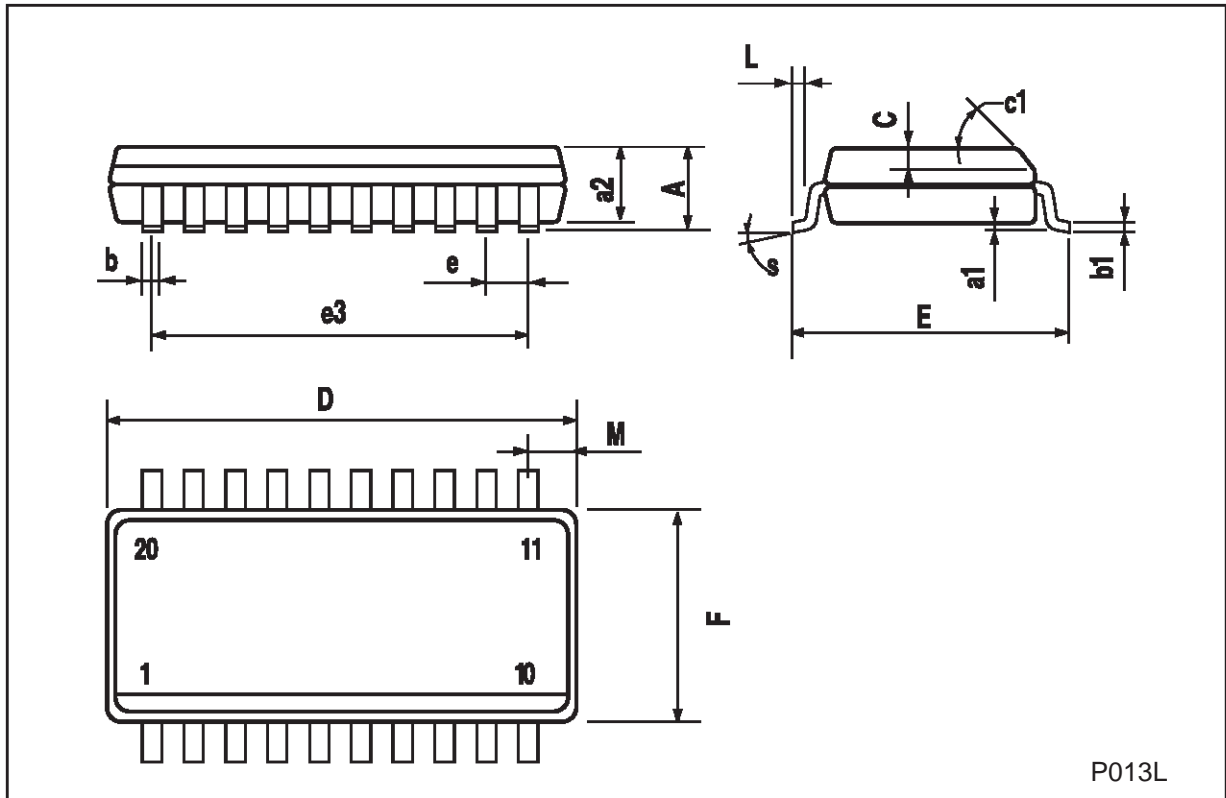
WAVEFORM 1: LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 3: PROPAGATION DELAY TIME** ($f=1\text{MHz}$; 50% duty cycle)

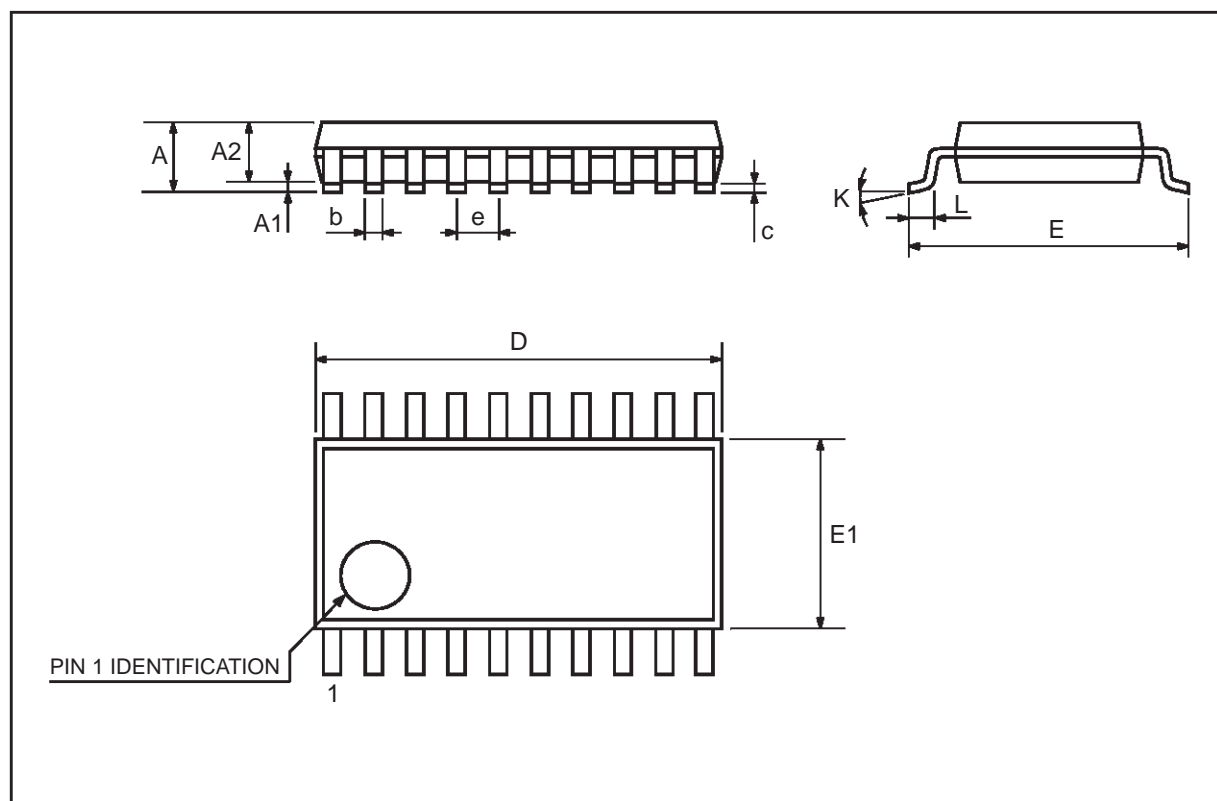
SO-20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1999 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

<http://www.st.com>