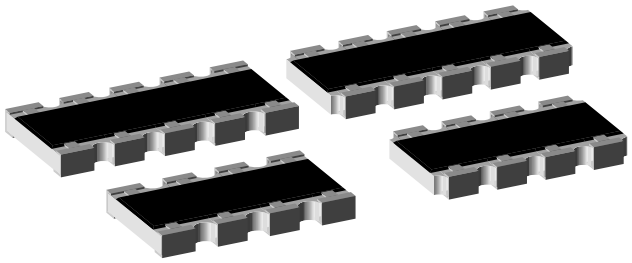
Thick Film Resistor/Capacitor Chip Array, Surface Mount



FEATURES

- Single component reduces board space and component counts
- X7R dielectric characteristic
- Wrap around termination
- Thick film R/C element
- Inner electrode protection
- Flow and reflow solderable
- Automatic placement capability, standard size
- 8 pin or 10 pin configurations
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

STANDARD ELECTRICAL SPECIFICATIONS

GLOBAL MODEL	SCHEMATIC	RESISTOR CHARACTERISTICS				CAPACITOR CHARACTERISTICS				
		POWER RATING $P_{70\,°C}$ W	TEMP. COEFF. ± ppm/°C	RESISTANCE TOLERANCE ± %	RESISTANCE RANGE Ω	DIELECTRIC	TEMPERATURE COEFFICIENT %	CAP. TOL. ± %	CAP. VOLTAGE V_{DC}	CAP. RANGE
CRCA12E CRCA12S	01	0.125	200	5	10 to 1M	X7R	± 15	20	50	10 pF to 270 pF
	02	0.125	200	5	10 to 1M	X7R	± 15	20	50	10 pF to 270 pF
	03	0.125	200	5	10 to 1M	X7R	± 15	20	50	10 pF to 270 pF

Notes

RESISTOR
- Operating temperature range: -55 °C to +125 °C
- Technology: Thick film

CAPACITOR
- Operating temperature range: X7R -55 °C to +125 °C
- Maximum dissipation factor: 2.5 %we
- Dielectric withstanding voltage: 125 V_{DC}, 5 s, 50 mA charge

- Ask about extended value ranges.
- Packaging: According to EIA 481.
- Power rating depends on the max. temperature at the solder point, the component placement density and the substrate material.

TECHNICAL SPECIFICATIONS

PARAMETER	UNIT	RESISTOR	X7R CAPACITOR
Rated dissipation at 70 °C (CECC 40401 I EIA 575)	W	0.125	-
Capacitor voltage rating	V	-	50
Dielectric withstanding voltage (5 s, 50 mA charge)	V_{DC}	-	125
Category temperature range	°C	-55 / +125	-55 / +125
Insulation resistance	Ω	$> 10^{10}$	

GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: CRCA12E081472220R (preferred part numbering format)

C	R	C	A	1	2	E	0	8	1	4	7	2	2	2	0	R	

MODEL	PIN COUNT	SCHEMATIC	RESISTANCE VALUE	CAPACITANCE VALUE	PACKAGING	SPECIAL
CRCA12E **CRCA12S**	**08** = 8 pin **10** = 10 pin	**1** = 01 **2** = 02 **3** = 03 **0** = Special	2 digit significant figures, followed by a multiplier **100** = 10 Ω **683** = 68 kΩ **105** = 1 MΩ (Tolerance = ± 5 %)	2 digit significant figures, followed by multiplier **100** = 10 pF **560** = 56 pF **271** = 270 pF (Tolerance = ± 20 %)	**E** = Lead (Pb)-free, T/R (2000 pcs) **R** = Tin/Lead, T/R (2000 pcs)	(Dash number) (Up to 1 digit) Blank = Standard

Historical Part Number Example: CRCA12E0801472J220MRB8 (will continue to be accepted)

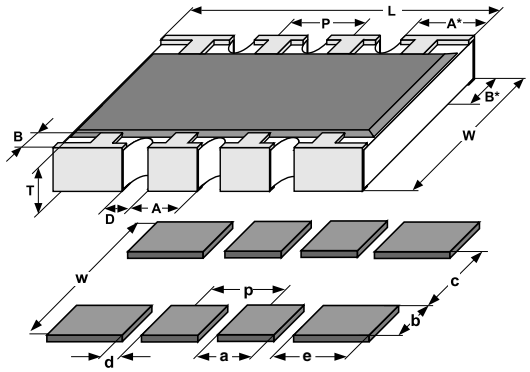
CRCA12E	08	01	472	J	220	M	RB8
MODEL	PIN COUNT	SCHEMATIC	RESISTANCE VALUE	TOLERANCE	CAPACITANCE VALUE	TOLERANCE	PACKAGING

Note
- For additional information on packaging, refer to the Surface Mount Network Packaging document (www.vishay.com/doc?31540).

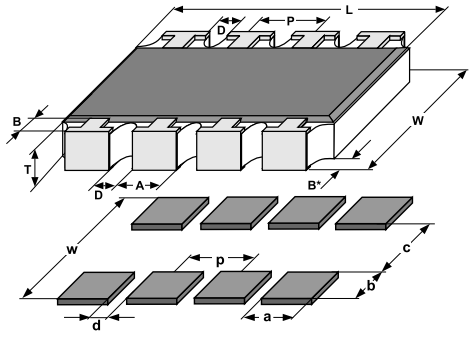
For technical questions, contact: ff2aresistors@vishay.com

DIMENSIONS

8-Terminal device S-Version



E-Version



GLOBAL MODEL	PIN NO#	SIZE		DIMENSIONS in millimeters								
		INCH	METRIC	L	W	T	B	B*	A	A*	D_{NOM}	P_{NOM}
CRCA12E	8	2012	5032	5.1 ± 0.15	3.05 ± 0.15	0.61 ± 0.10	0.51 ± 0.25	0.38 ± 0.2	0.79 ± 0.15	-	0.25	1.27
CRCA12S	8	2012	5032	5.1 ± 0.15	3.05 ± 0.15	0.61 ± 0.10	0.51 ± 0.25	0.38 ± 0.2	0.79 ± 0.15	0.89 ± 0.15	0.25	1.27
CRCA12E	10	2512	6432	6.4 ± 0.15	3.05 ± 0.15	0.61 ± 0.10	0.51 ± 0.25	0.38 ± 0.2	0.79 ± 0.15	-	0.25	1.27
CRCA12S	10	2512	6432	6.4 ± 0.15	3.05 ± 0.15	0.61 ± 0.10	0.51 ± 0.25	0.38 ± 0.2	0.79 ± 0.15	0.89 ± 0.15	0.25	1.27

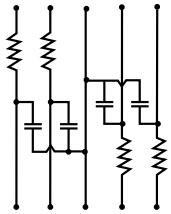
SOLDER PAD DIMENSIONS in millimeters							
	c	w	d	p	a	b	e
WAVE SOLDERING	2.2	4.3	0.57	1.27	0.71	1.05	1.09
REFLOW SOLDERING	2.2	3.9	0.57	1.27	0.71	0.86	1.09

Note

- The images shown are for an 8 pin part. For a 10 pin part, use the same pitch and add another pair of “a” dimension pads to the inner solder pads.

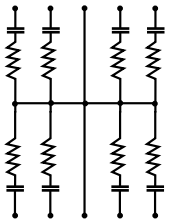
SCHEMATICS

01 Circuit
CRCA12E and S



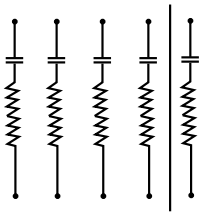
10 Pin only

02 Circuit
CRCA12E and S

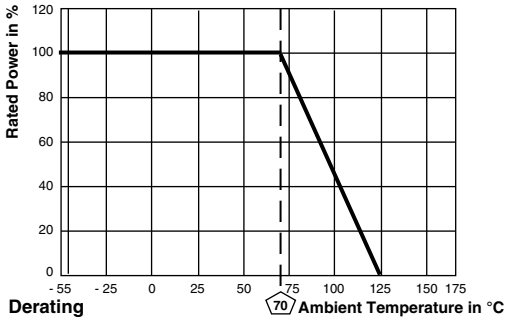


10 Pin only

03 Circuit
CRCA12E and S



8 Pin 10 Pin



PERFORMANCE

TEST	CONDITIONS OF TEST	TEST RESULTS (TYPICAL TEST LOTS)	
		R	C
Endurance test at 70 °C MIL-STD-202 method 108	1000 h at 70 °C, 1.5 h “ON”, 0.5 h “OFF”	± (5 % + 2 Ω)	± 20 %
Dielectric withstanding voltage MIL-STD-202 method 301	125 V_{DC}, 5 s, 50 mA charge	No physical damage	
Thermal shock MIL-STD-202 method 107	100 cycles, -55 °C to +125 °C	± (5 % + 2 Ω)	± 20 %
Moisture MIL-STD-202 method 106	Omit steps 7A and B	± (5 % + 2 Ω)	± 20 %
Resistance to soldering heat EIA 575	10 s at 260 °C solder bath temperature	± (5 % + 2 Ω)	± 20 %
High temperature exposure EIA 575	125 °C for 100 h	± (5 % + 2 Ω)	± 20 %
Low temperature operation EIA 575	1 h at -55 °C then 45 min at 50 V	± (5 % + 2 Ω)	± 20 %
Solderability and leaching EIA 575 3.12	Condition C	95 % coverage	

APPLICABLE SPECIFICATIONS

- IPC standards
- EIA 575

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