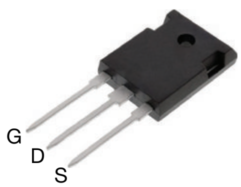
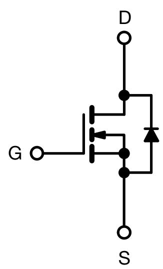
Automotive E Series Power MOSFET with Fast Body Diode

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ typ. at 25 °C (Ω)	V_{GS} = 10 V	0.045
Q_g typ. (nC)	229	
Q_{gs} (nC)	53	
Q_{gd} (nC)	91	
Configuration	Single	

TO-247AD





N-Channel MOSFET

FEATURES

AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE

- Fast body diode MOSFET using Automotive Grade E series technology
- Reduced t_{rr}, Q_{rr}, and I_{RRM}
- Low figure-of-merit (FOM) R_{on} x Q_g
- Low input capacitance (C_{iss})
- Low switching losses due to reduced Q_{rr}
- 175 °C operating temperature
- AEC-Q101 qualified
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Automotive onboard charger
- Automotive DC/DC converter

ORDERING INFORMATION	
Package	TO-247AD
Lead (Pb)-Free and Halogen-Free	SQW61N65EF-GE3

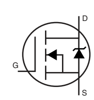
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	650	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 175 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	62	A
		T_C = 100 °C		44	
Pulsed Drain Current [a]			I_{DM}	187	
Linear Derating Factor				4.2	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	1323	mJ
Maximum Power Dissipation			P_D	625	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +175	°C
Drain-Source Voltage Slope			dV/dt	70	V/ns
Reverse Diode dV/dt [d]				50	
Soldering Recommendations (Peak temperature) [c]	For 10 s			260	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature
b. V_{DD} = 140 V, starting T_J = 25 °C, L = 73.5 mH, R_g = 25 Ω, I_{AS} = 6 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, di/dt = 470 A/μs, starting T_J = 25 °C

THERMAL RESISTANCE RATINGS			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	0.24	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 30 mA	-	0.77	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 520 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 520 V, V_{GS} = 0 V, T_J = 125 °C	-	-	500	μA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 32 A	-	0.045	0.052	Ω
Forward Transconductance	g_{fs}	V_{DS} = 30 V, I_D = 32 A	-	28	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	7379	-	pF
Output Capacitance	C_{oss}		-	310	-	
Reverse Transfer Capacitance	C_{rss}		-	4	-	
Effective Output Capacitance, Energy Related [a]	$C_{o(er)}$	V_{DS} = 0 V to 520 V, V_{GS} = 0 V	-	213	-	
Effective Output Capacitance, Time Related [b]	$C_{o(tr)}$		-	841	-	
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 32 A, V_{DS} = 520 V	-	229	344	nC
Gate-Source Charge	Q_{gs}		-	53	-	
Gate-Drain Charge	Q_{gd}		-	91	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 520 V, I_D = 32 A, V_{GS} = 10 V, R_g = 9.1 Ω	-	65	98	ns
Rise Time	t_r		-	107	161	
Turn-Off Delay Time	$t_{d(off)}$		-	252	378	
Fall Time	t_f		-	102	153	
Gate Input Resistance	R_g	f = 1 MHz, open drain	0.5	1	2	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	62	A
Pulsed Diode Forward Current	I_{SM}		-	-	187	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 32 A, V_{GS} = 0 V	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 30.5 A, di/dt = 100 A/μs, V_R = 400 V	-	204	408	ns
Reverse Recovery Charge	Q_{rr}		-	1.9	3.8	μC
Reverse Recovery Current	I_{RRM}		-	18	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

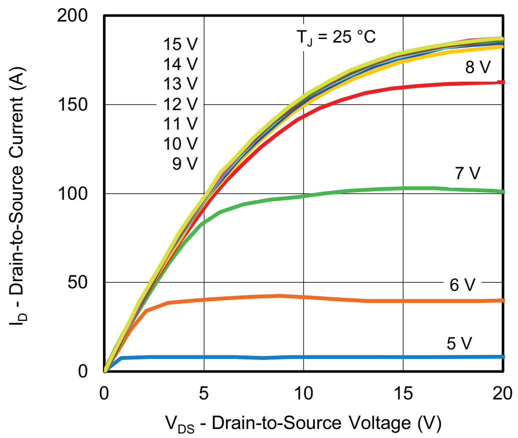


Fig. 1 - Typical Output Characteristics

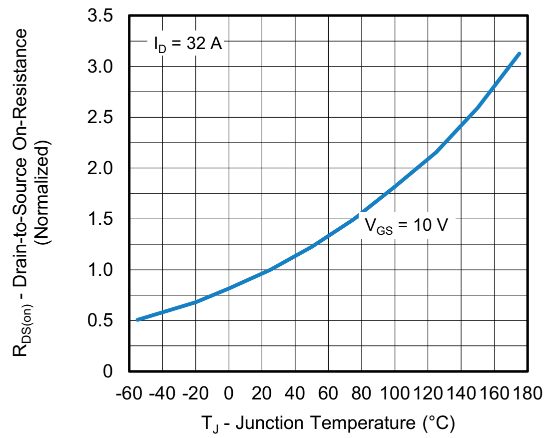


Fig. 4 - Normalized On-Resistance vs. Temperature

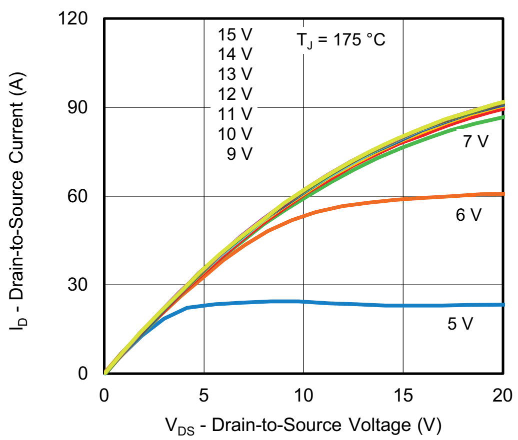


Fig. 2 - Typical Output Characteristics

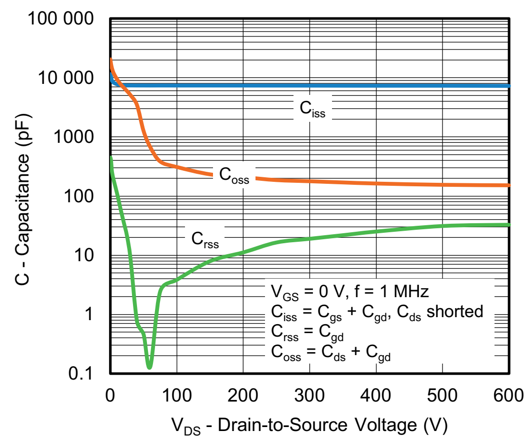


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

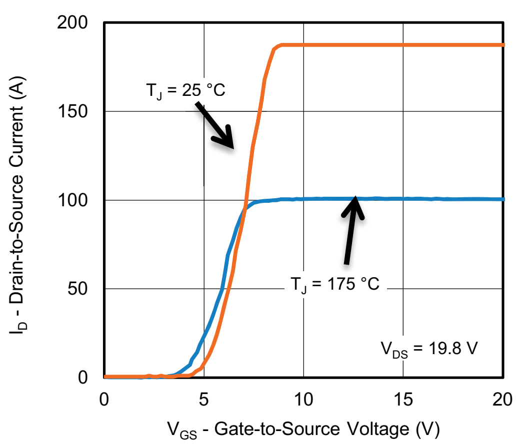


Fig. 3 - Typical Transfer Characteristics

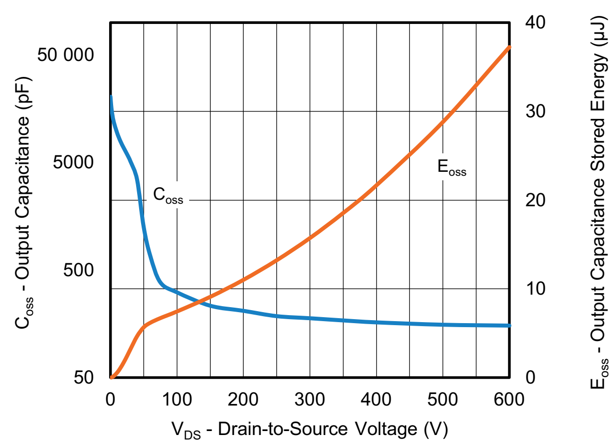


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

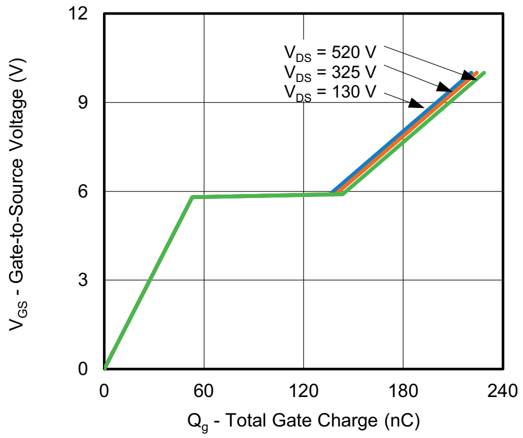


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

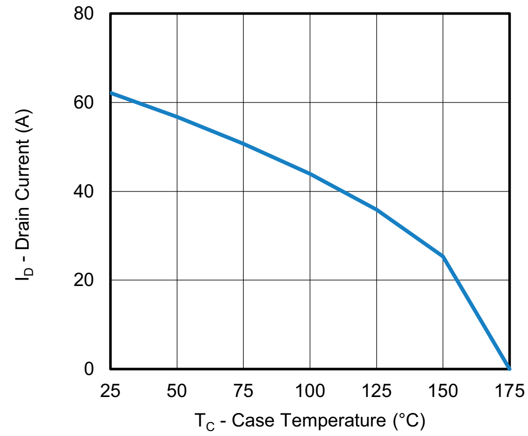


Fig. 10 - Maximum Drain Current vs. Case Temperature

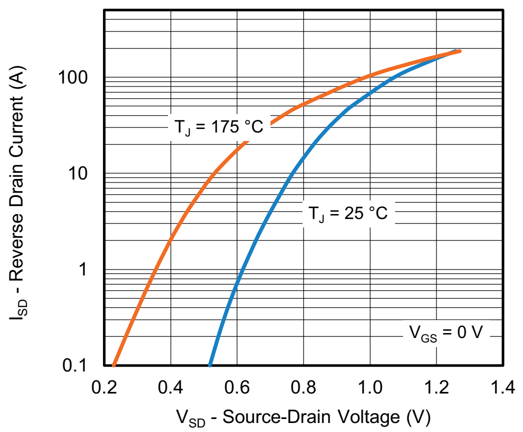


Fig. 8 - Typical Source-Drain Diode Forward Voltage

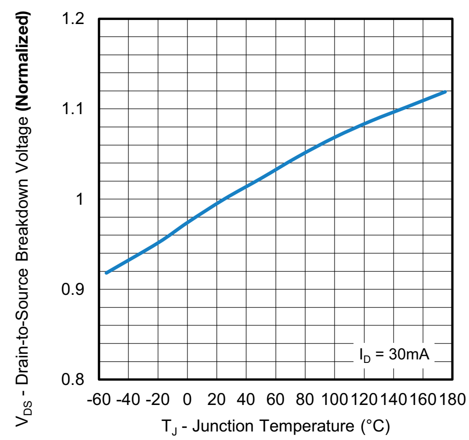


Fig. 11 - Temperature vs. Drain-to-Source Voltage

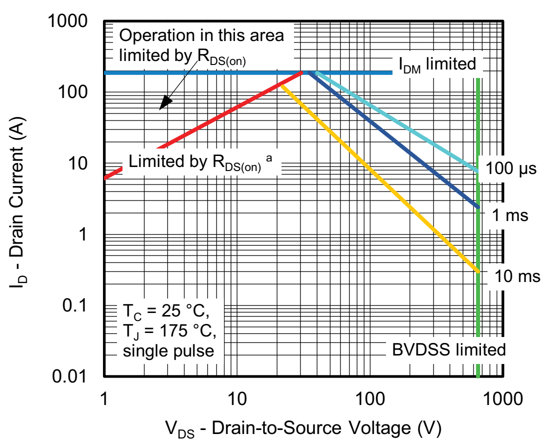


Fig. 9 - Maximum Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

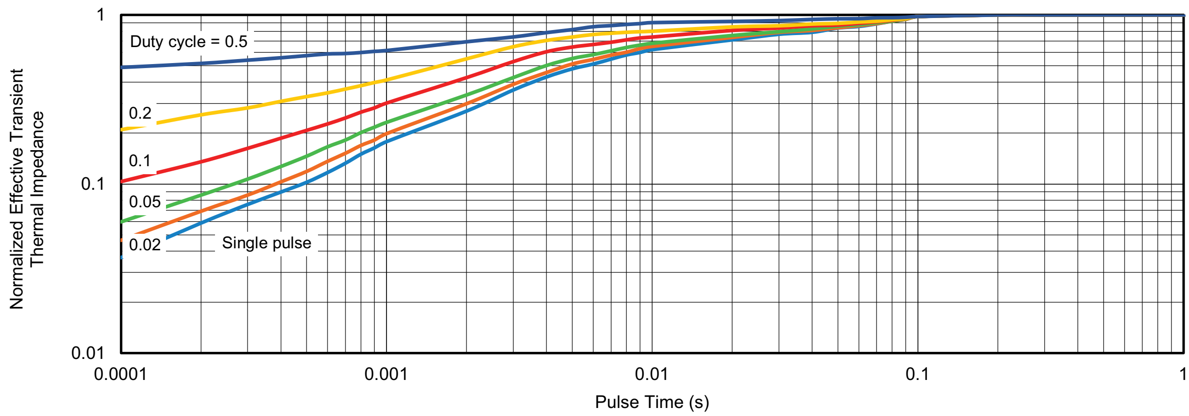


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

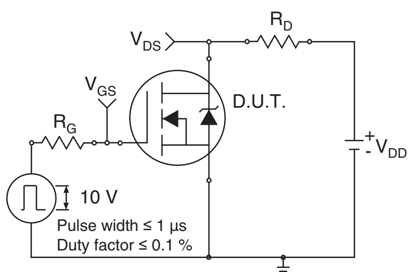


Fig. 13 - Switching Time Test Circuit

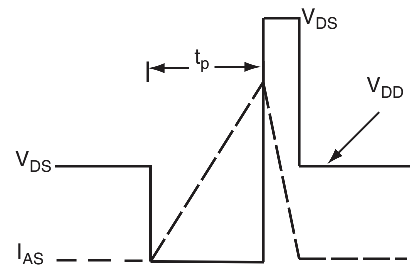


Fig. 16 - Unclamped Inductive Waveforms

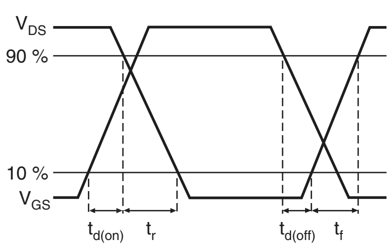


Fig. 14 - Switching Time Waveforms

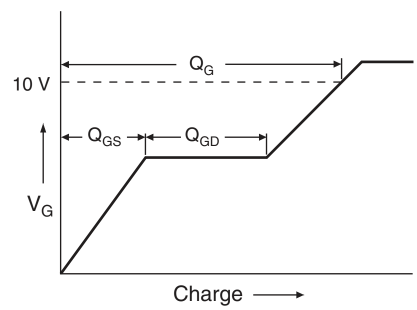


Fig. 17 - Basic Gate Charge Waveform

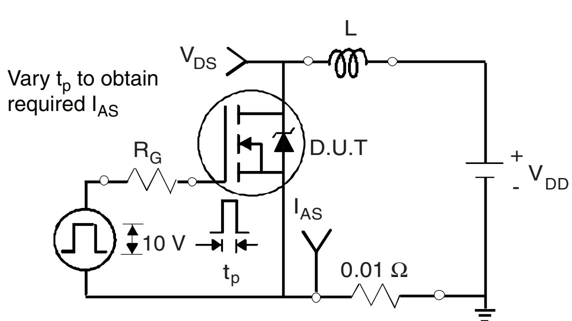


Fig. 15 - Unclamped Inductive Test Circuit

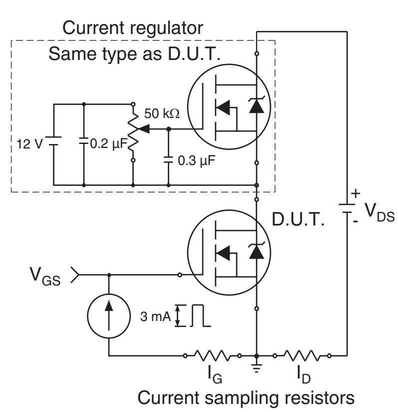
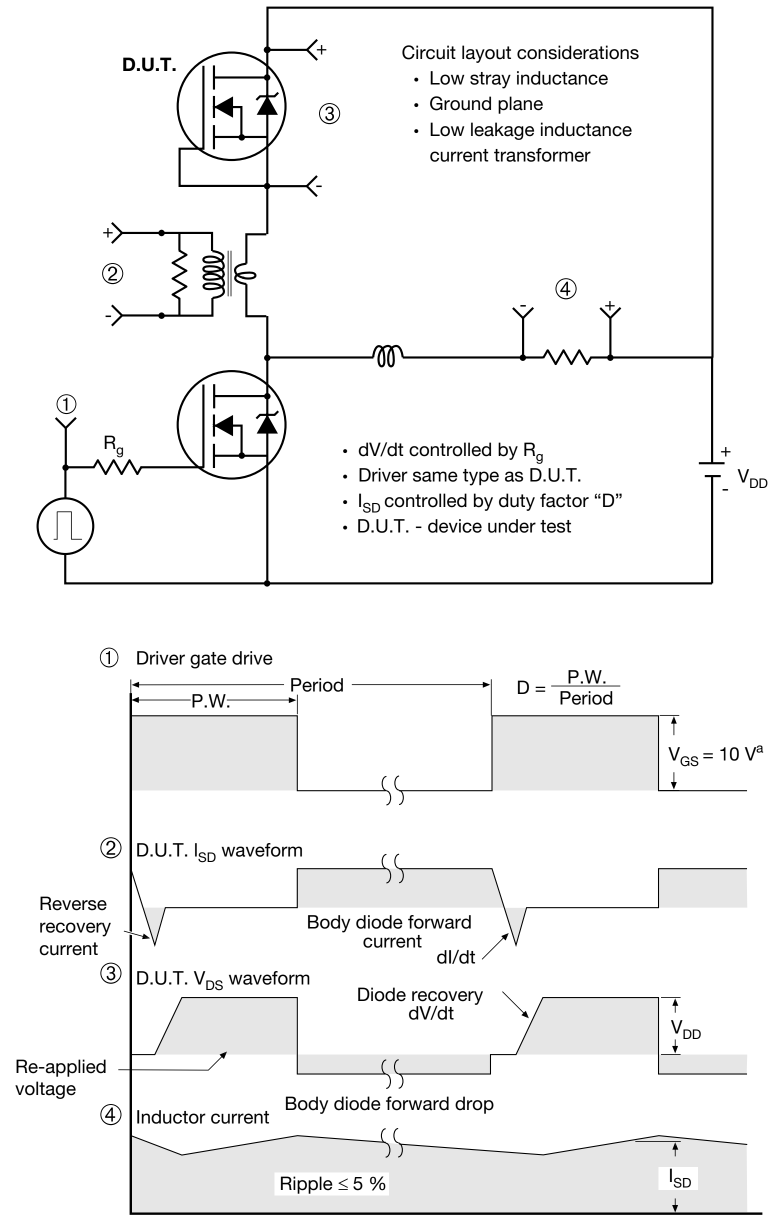


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. V_{GS} = 5 V for logic level devices

Fig. 19 - For N-Channel

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