Powered-off Isolation, 0.86 Ω, 1.65 V to 5.5 V, SPDT Analog Switch (2:1 Multiplexer)

DESCRIPTION

The DG4157E is a high performance single-pole, double-throw (SPDT) analog switch designed for 1.65 V to 5.5 V operation with a single power rail.

Fabricated with high density CMOS technology, the device achieves low on resistance of 0.86 Ω at a 4.5 V power supply, low power consumption, and fast switching speeds.

The DG4157E can handle both analog and digital signals and permits signals with amplitudes of up to V+ to be transmitted in either direction. Its control logic inputs can go over V+ up to 5.5 V. The control logic input high threshold is guaranteed as low as 1.8 V over the power supply range up to 5.5 V. It features break before make switching performance. Its -3 dB bandwidth is typically 152 MHz.

A powered-off protection circuit is built into the switch to prevent an abnormal current flow from COM pin to V+ during the power-down condition. Each output pin can withstand greater than 7 kV (human body model).

Operation temperature is specified from -40 °C to +85 °C. The DG4157E is available in the ultra compact µDFN-6L and SC-70-6 packages.

FEATURES

Pb-free Available

RoHS COMPLIANT

HALOGEN FREE

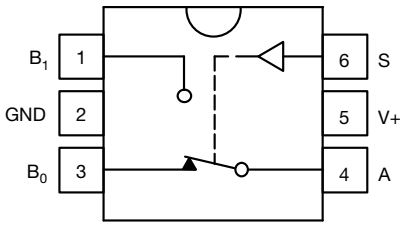
- Low switch on-resistance (0.86 Ω)
- 1.65 V to 5.5 V single supply operation
- Isolation in powered-off mode
- Guaranteed 1.8 V logic high
- Control logic inputs can go over V+
- Low charge injection (5 pC)
- Low total harmonic distortion
- Break before make switching
- Latch-up performance exceeds 300 mA per JESD 78
- ESD tested
  - 7000 V human body model (JS-001)
  - 1000 V charge device model (JS-002)
- Ultra compact µDFN-6L 1 mm x 1 mm x 0.35 mm package
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

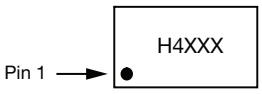
- Smartphones and tablets
- Consumer and computing
- Portable instrumentation
- Medical equipment

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

SC-70-6L

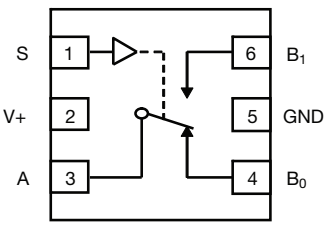


Top view

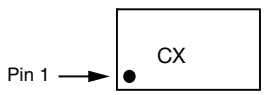


Device marking: H4XXX
XXX = date / lot traceability code

µDFN-6L



Top view



Device marking: CX
X = date / lot traceability code

TRUTH TABLE	
LOGIC INPUT (S)	FUNCTION
0	B_0 connected to A
1	B_1 connected to A

ORDERING INFORMATION		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	SC-70-6L	DG4157EDL-T1-GE3
	µDFN-6L	DG4157EDN-T1-GE4

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		**LIMIT**	**UNIT**
V+, A, B_0, B_1, S reference to GND		-0.3 to 6	V
Continuous current (any terminal)		± 200	mA
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 400	
Thermal resistance [a]		407	°C/W
ESD / HBM	JS-001	7000	V
ESD / CDM	JS-002	1000	
Latch up	JESD78	300	mA
Operating temperature		-40 to +85	°C
Max. operating junction temperature		150	
Operating junction temperature		125	
Storage temperature		-65 to +150	

Note

a. Measured on an 1" x 1" inch FR4 board, using 0.39" by 1", 2 oz. copper trace without air flow

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 3 V, V_S = 0 V or V+ [e]	**TEMP.[a]**	**LIMITS** -40 °C to +85 °C			**UNIT**
				MIN. [b]	**TYP. [c]**	**MAX. [b]**	
DC Characteristics							
On resistance	R_{ON}	V+ = 2.7 V, B_0 or B_1 = 1.5 V, I_O = 100 mA	Room	-	1.6	2	Ω
			Full	-	-	3	
		V+ = 4.5 V, B_0 or B_1 = 3.5 V, I_O = 100 mA	Room	-	0.86	1.2	
			Full	-	-	1.5	
On resistance flatness	$R_{FLATNESS}$	V+ = 2.7 V, B_0 or B_1 = 0.75 V, 1.5 V, I_O = 100 mA	Room	-	0.2	-	
		V+ = 4.5 V, B_0 or B_1 = 1 V, 3.5 V, I_O = 100 mA	Room	-	0.05	0.3	
			Full	-	-	0.4	
On resistance match	ΔR_{ON}	V+ = 2.7 V, B_0 or B_1 = 1.5 V, I_O = 100 mA	Room	-	0.003	-	
		V+ = 4.5 V, B_0 or B_1 = 3.5 V, I_O = 100 mA	Room	-	0.004	0.12	
			Full	-	-	0.15	
Switch off leakage current	I_{OFF}	V+ = 5.5 V, A = 1 V, 4.5 V B_0 or B_1 = 4.5 V, 1 V or floating	Room	-3	1.36	3	nA
			Full	-20	-	20	
Switch on leakage current	I_{ON}		Room	-4	1.4	4	
			Full	-40	-	40	
Power down leakage	$I_{A(DP)}$	V+ = 0 V, V_A = 4.5 V, V_S = GND	Full	-1	-	1	µA
Digital Control							
Input, high voltage	V_{INH}	V+ = 2.7 V to 5.5 V	Full	1.8	-	-	V
Input, low voltage	V_{INL}		Full	-	-	0.6	
Input current	I_{INH}, I_{INL}	V_S = 0 or V+	Full	-1	-	1	µA

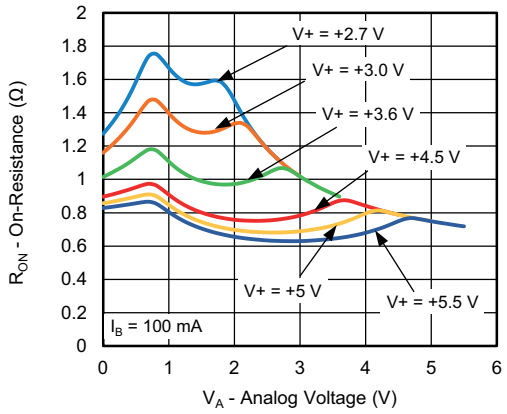
SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, V_S = 0 V or V+ [e]	TEMP.[a]	LIMITS -40 °C to +85 °C MIN. [b]	TYP. [c]	MAX. [b]	UNIT
AC Characteristics							
Turn-on time [d]	t_{ON}	V+ = 2.7 V, B_0 or B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room	-	27	42	ns
			Full	-	-	47	
		V+ = 4.5 V, B_0 or B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room	-	17	32	
			Full	-	-	35	
Turn-off time [d]	t_{OFF}	V+ = 2.7 V, B_0 or B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room	-	16	32	
			Full	-	-	35	
		V+ = 4.5 V, B_0 or B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room	-	11	28	
			Full	-	-	30	
Break-before-make time [d]	t_{BBM}	V+ = 2.7 V, B_0 = B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room	1	13	-	
		V+ = 4.5 V, B_0 = B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF		1	8	-	
Charge injection [d]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Room	-	-5	-	pC
Off isolation [d]	OIRR	R_L = 50 Ω, f = 1 MHz	Room	-	-64	-	dB
		R_L = 50 Ω, f = 10 MHz		-	-41	-	
Crosstalk [d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-64	-	
		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz		-	-41	-	
Bandwidth [d]	BW	R_L = 50 Ω	Room	-	152	-	MHz
Total harmonic distortion [d]	THD	R_L = 600 Ω, V_{SIGNAL} = 0.5 V, f = 20 Hz to 20 kHz	Room	-	0.0055	-	%
Capacitance							
BX port off capacitance [d]	$C_{B(OFF)}$	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	13	-	pF
A port on capacitance [d]	$C_{A(ON)}$			-	52	-	
Control pin capacitance [d]	C_{IN}			-	1	-	
Power Supply							
Quiescent supply current	I+	V+ = 5.5 V, V_S = 0 V, 5.5 V	Room	-	0.0004	0.8	µA
			Full	-	-	1	

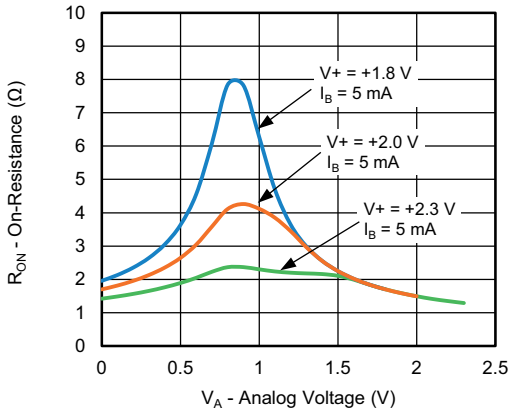
Notes

a. Room = 25 °C, full = as determined by the operating suffix
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
c. Typical values are for design aid only, not guaranteed nor subject to production testing
d. Guarantee by design, nor subjected to production test
e. V_S = input voltage to perform proper function

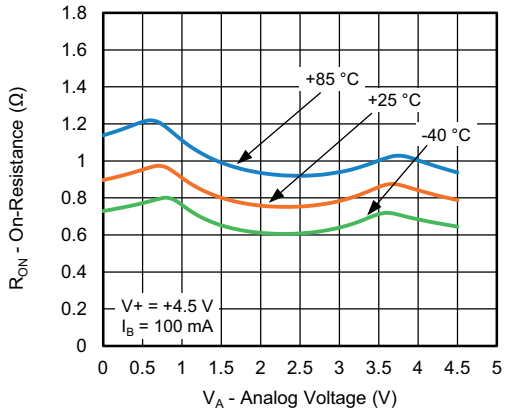
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



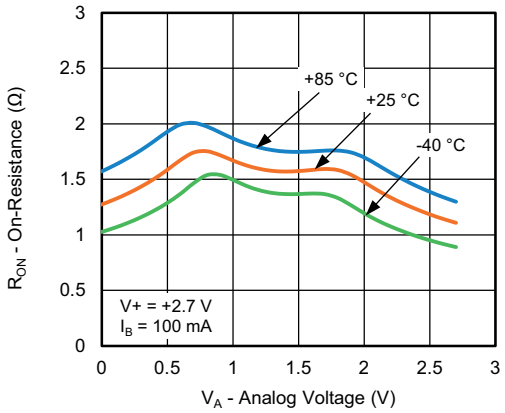
R_{ON} vs. V_A and Supply Voltage



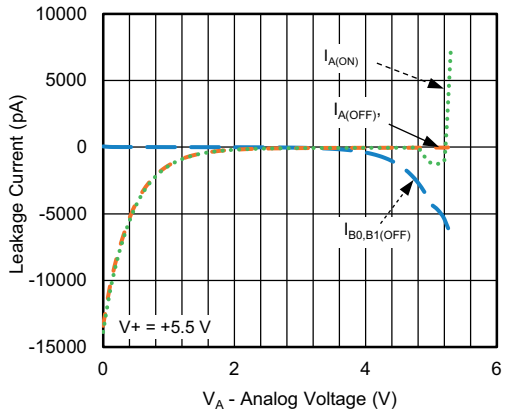
R_{ON} vs. V_A and Supply Voltage



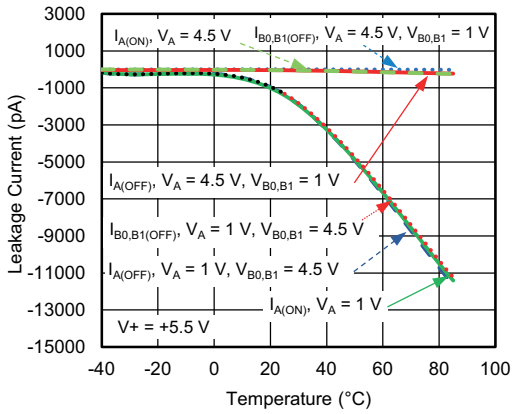
R_{ON} vs. V_A and Temperature



R_{ON} vs. V_A and Temperature

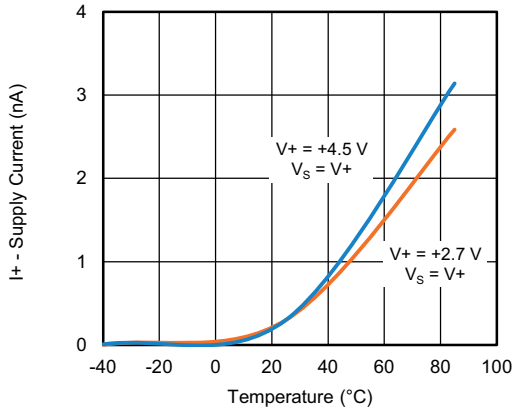


Leakage Current vs. Analog Voltage

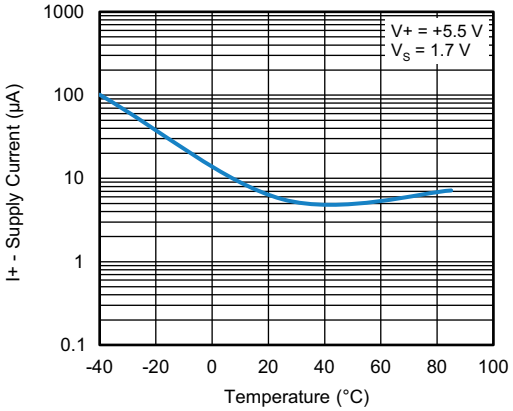


Leakage Current vs. Temperature

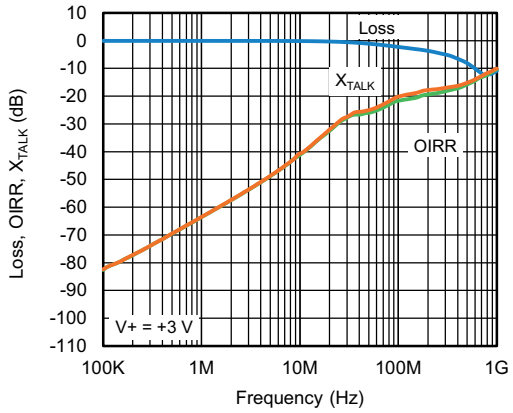
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



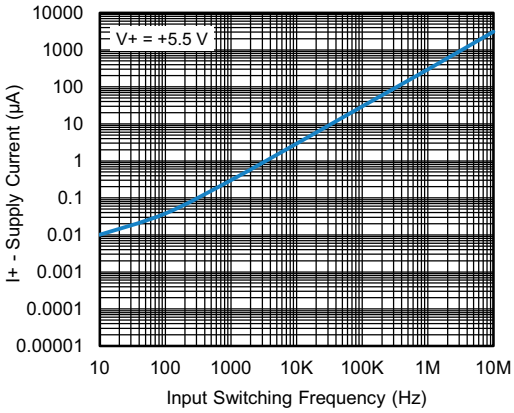
Supply Current vs. Temperature



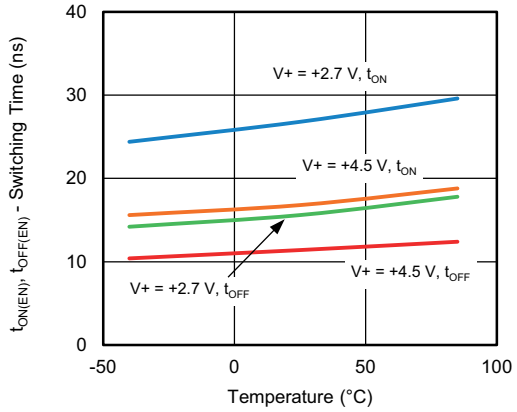
Supply Current vs. Temperature



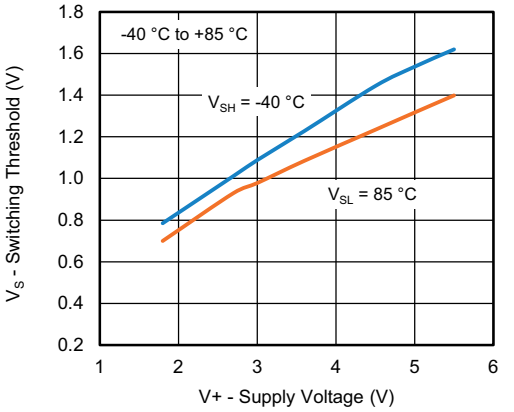
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



Supply Current vs. Switching Frequency

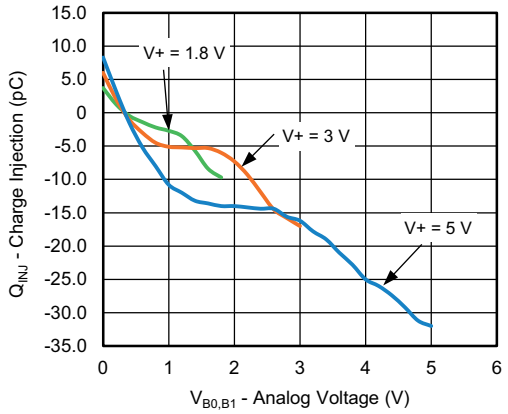


Switching Time vs. Temperature

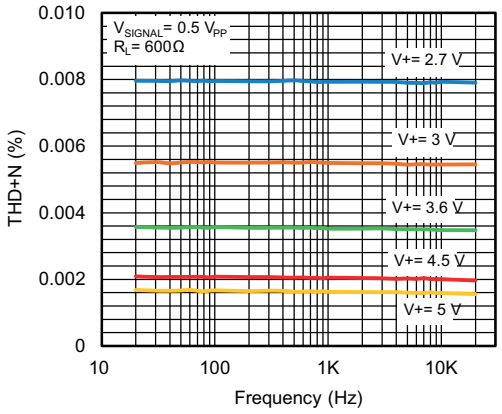


Switching Threshold vs. Supply Voltage

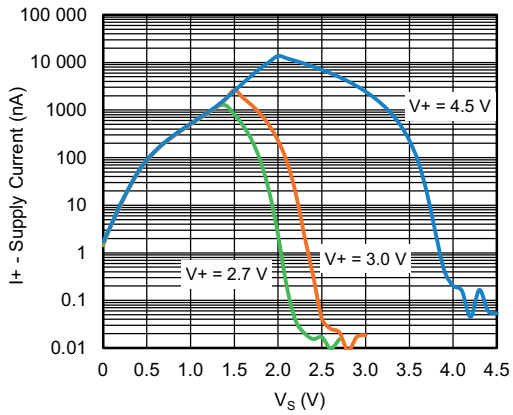
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



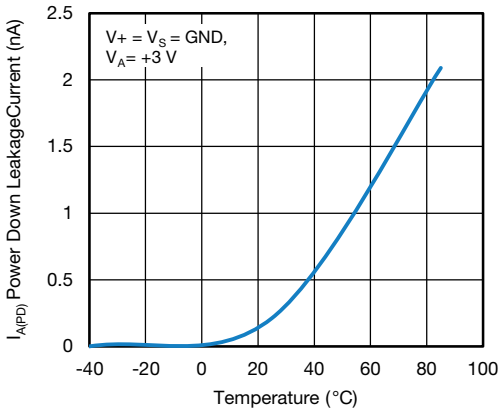
Charge Injection vs. Source Voltage



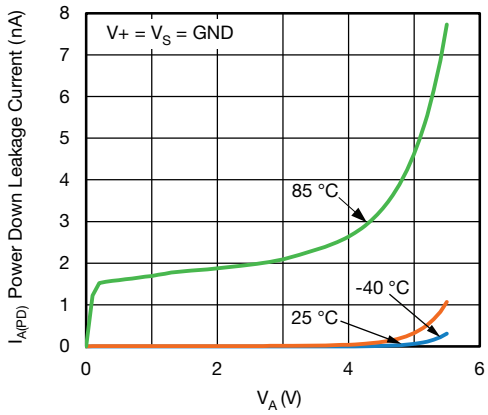
THD+N vs. Frequency



Supply Current vs. Logic Voltage



Power Down Leakage Current vs. Temperature



Power Down Leakage Current vs. V_A

TEST CIRCUITS

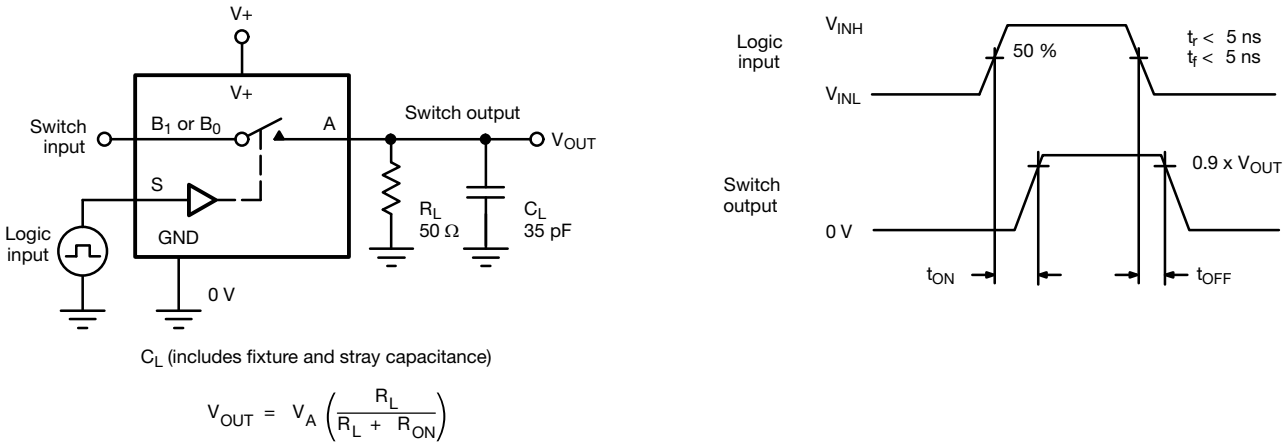


Fig. 1 - Switching Time

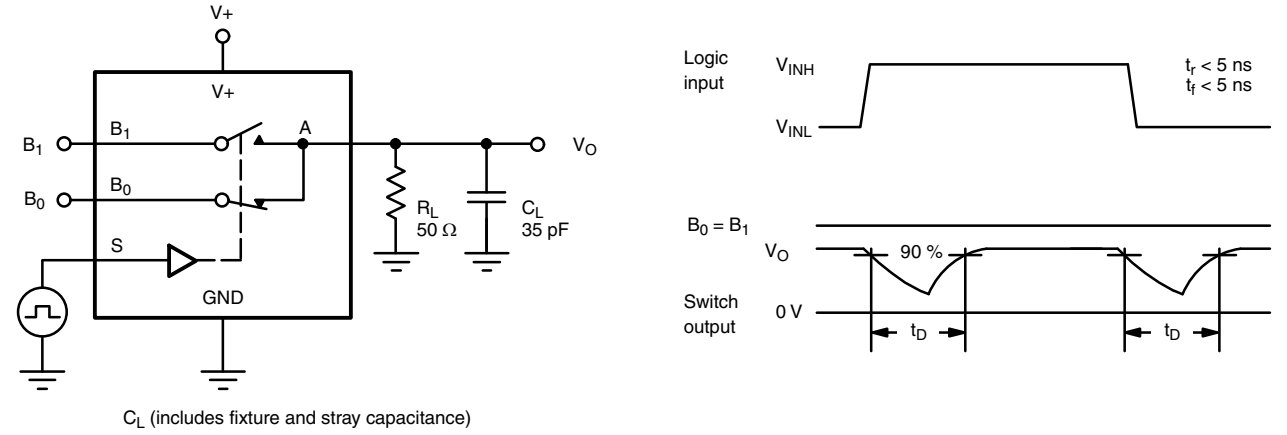


Fig. 2 - Break-Before-Make Interval

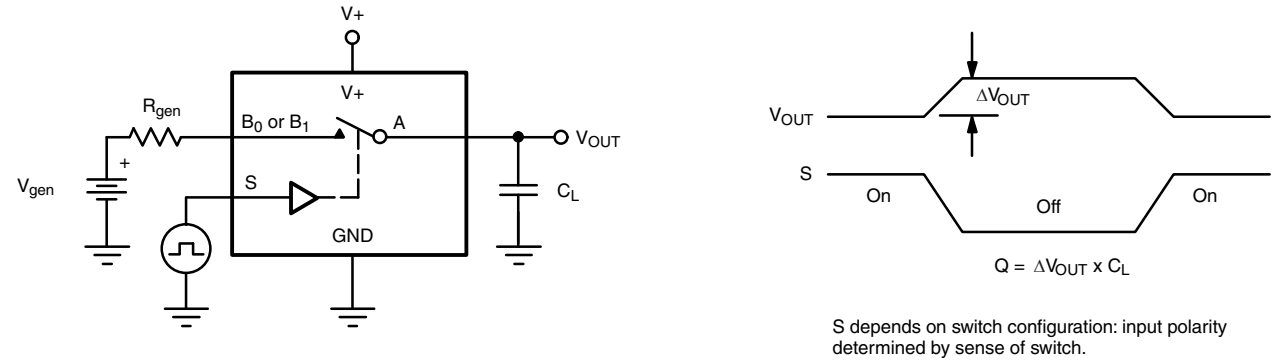


Fig. 3 - Charge Injection

TEST CIRCUITS

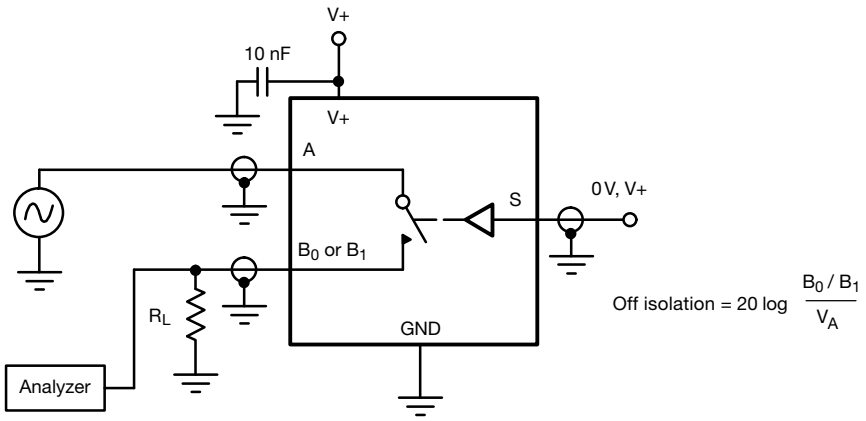


Fig. 4 - Off-Isolation

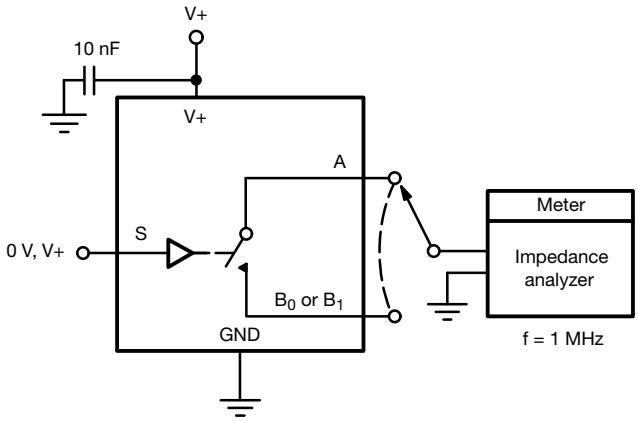


Fig. 5 - Channel Off/On Capacitance

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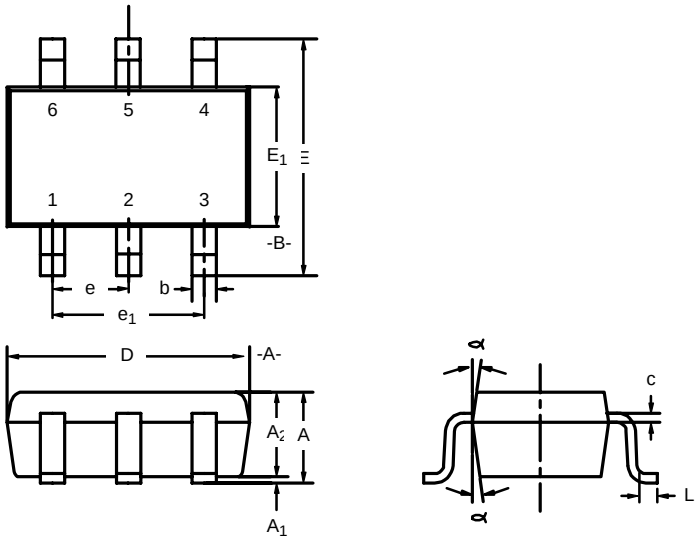
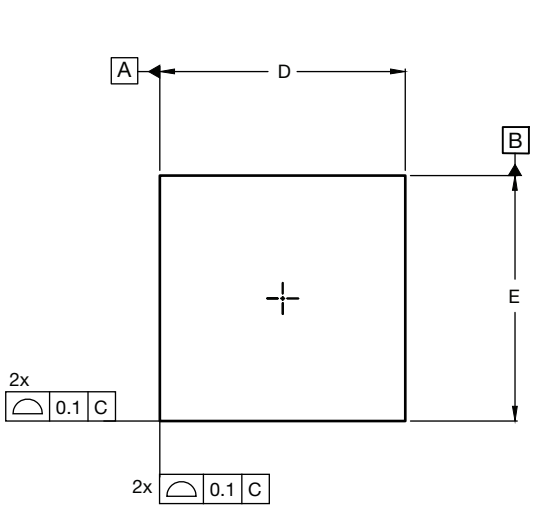
SC-70: 6-LEADS



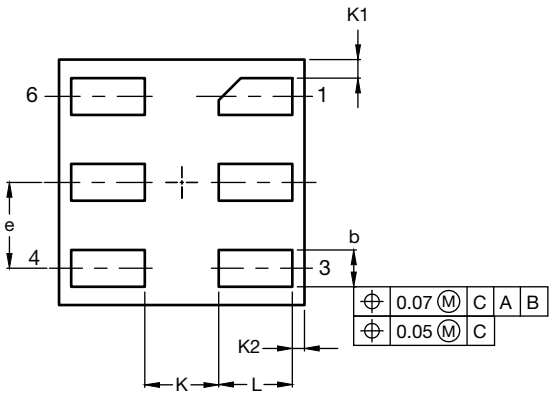
Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	–	1.10	0.035	–	0.043
A_1	–	–	0.10	–	–	0.004
A_2	0.80	–	1.00	0.031	–	0.039
b	0.15	–	0.30	0.006	–	0.012
c	0.10	–	0.25	0.004	–	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E_1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e_1	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

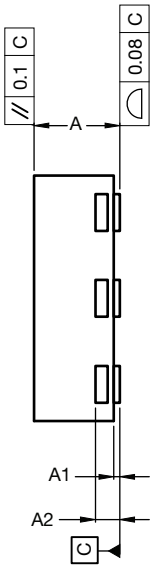
µDFN-6L 1 mm x 1 mm Case Outline



Top view



Bottom view



Side view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.32	0.35	0.38	0.013	0.014	0.015
A1	0.00	-	0.05	0.000	-	0.002
A2		0.10 Ref.			0.004 Ref.	
b	0.12	0.15	0.18	0.005	0.006	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.95	1.00	1.05	0.037	0.039	0.041
e		0.35 BSC			0.014 BSC	
K		0.30 Ref.			0.012 Ref.	
K1		0.075 Ref.			0.003 Ref.	
K2		0.05 Ref.			0.002 Ref.	
L	0.27	0.30	0.33	0.011	0.012	0.013

Notes

(1) Use millimeters as the primary measurement.
(2) Dimensioning and tolerances conform to ASME Y14.5M-1994.
(3) N is the number of terminals.
Nd and Ne is the number of terminals in each D and E site respectively.
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
(6) Package warpage max. 0.05 mm.

ECN: T16-0553-Rev. A, 26-Sep-16
DWG: 6053

Disclaimer

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