

Vishay Siliconix

16 Ω , Low Parasitic Capacitance and Leakage, +12 V / +5 V / +3 V / ± 5 V Quad SPST Switches

DESCRIPTION

The DG411LE, DG412LE, and DG413LE are monolithic quad single-pole-single-throw analog switches. The DG411LE and DG412LE differ only in that they respond to opposite logic levels. The DG413LE has two normally open and two normally closed switches. It can be given various configurations, including four SPST, two SPDT, and one DPDT.

The DG411LE, DG412LE, and DG413LE offer low on resistance of 16 Ω , low parasitic capacitance of 15 pF switch on capacitance, and low charge injection over the signal swing range.

The DG411LE, DG412LE, and DG413LE operate on single and dual supplies. Single supply voltage ranges from 3 V to 16 V while dual supply operation is recommended with \pm 3 V to \pm 8 V. Each switch conducts equally well in both direction when on, and blocks input voltages up to the supply levels when off.

The DG411LE, DG412LE, and DG413LE are available in 16 lead TSSOP, SOIC, and PDIP packages.

FEATURES

 3 V to 16 V single supply or ± 3 V to ± 8 V dual supply



• On-resistance $R_{DS(on)}$: 16 Ω

• Low parasitic capacitance:

C_{D(ON)}: 15 pF C_{S(OFF)}: 5 pF

 Less than 8 pC charge injection over the full signal swing range

 Fast switching t_{ON}: 16 ns t_{OFF}: 9 ns

• TTL, CMOS compatible

 Material categorization: for definitions of compliance please see <u>www.vishav.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

BENEFITS

- Wide operation voltage range
- Low signal errors and distortion
- · Fast switching time
- Minimized switching glitch

APPLICATIONS

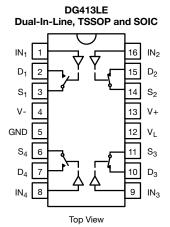
- · Automatic test equipment
- · Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- · Audio and video signal routing
- Relay replacement
- Battery powered systems
- Computer peripherals
- · Audio and video signal routing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line, TSSOP and SOIC IN₁ IN₂ D_2 D٩ Sı S_2 V-V٠ V_L **GND** S_3 S_4 D_4 D_3 IN_4

Top View

DG411LE, DG412LE



Document Number: 78091



DG411LE, DG412LE, DG413LE

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TRUTH TABLE								
LOGIC	DG411LE	DG412LE						
0	ON	OFF						
1	OFF	ON						

Logic "0" \leq 0.8 V Logic "1" \geq 2.4 V

TRUTH TABLE							
LOGIC	SW ₁ , SW ₄	SW ₂ , SW ₃					
0	OFF	ON					
1	ON	OFF					

 $\begin{array}{l} Logic~"0" \leq 0.8~V \\ Logic~"1" \geq 2.4~V \end{array}$

ORDERING INFORMATION								
TEMP. RANGE	CONFIGURATION	PACKAGE	PART NUMBER	MIN. ORDER / PACK. QUANTITY				
		16-pin TSSOP	DG411LEDQ-GE3	Tube 360 units				
		10-рін 1330Р	DG411LEDQ-T1-GE3	Tape and reel, 3000 units				
	DG411LE	10 -i- 0010	DG411LEDY-GE3	Tube 500 units				
		16-pin SOIC	DG411LEDY-T1-GE3	Tape and reel, 2500 units				
		16-pin PDIP	DG411LEDJ-GE3	Tube 500 units				
		16-pin TSSOP -	DG412LEDQ-GE3	Tube 360 units				
40.00			DG412LEDQ-T1-GE3	Tape and reel, 3000 units				
-40 °C to +85 °C Lead-free	DG412LE		DG412LEDY-GE3	Tube 500 units				
Load 1100			DG412LEDY-T1-GE3	Tape and reel, 2500 units				
		16-pin PDIP	DG412LEDJ-GE3	Tube 500 units				
		16 pin TSSOD	DG413LEDQ-GE3	Tube 360 units				
		16-pin TSSOP	DG413LEDQ-T1-GE3	Tape and reel, 3000 units				
	DG413LE	16-pin SOIC	DG413LEDY-GE3	Tube 500 units				
		10-ріп 3010	DG413LEDY-T1-GE3	Tape and reel, 2500 units				
		16-pin PDIP	DG413LEDJ-GE3	Tube 500 units				

ABSOLUTE MAXIMUM RATINGS							
PARAMETER		LIMIT	UNIT				
V+ to V-		-0.3 to +18					
GND to V-		18	7				
V _L		(GND -0.3) to (V+) +0.3	V				
I _N a, V _S , V _D		-0.3 to (V+) +0.3 or 30 mA, whichever occurs first					
Continuous Current (Any terminal)		30	A				
Peak Current, S or D (Pulsed 1 ms, 10 % du	ity cycle)	100	mA				
Storage Temperature	(DQ, DY suffix)	-65 to +125	°C				
Storage remperature	(AK suffix)	-65 to +150	7				
	16-pin TSSOP ^c	450					
Power Dissipation (Packages) b	16-pin SOIC ^d	650	mW				
	16-pin CerDIP ^e	900	7				
ESD Human Body Model (HBM); per ANSI /	ESDA / JEDEC® JS-001	2500	V				
Latch Up Current, per JESD78D		400	mA				

Notes

- a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
- b. All leads welded or soldered to PC board
- c. Derate 7 mW/°C above 75 °C
- d. Derate 7.6 mW/°C above 75 °C
- e. Derate 12 mW/°C above 75 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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SPECIFICATIONS ^a (Single Supply 12 V)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED	TEMP. b	TYP. °	LIM	IFFIX IITS 0 +125 °C	LIM	IFFIX IITS o +85 °C	UNIT
		$V_{+} = 12 \text{ V}, V_{-} = 0 \text{ V}$ $V_{L} = 5 \text{ V}, V_{IN} = 2.4 \text{ V}, 0.8 \text{ V}^{f}$			MIN. d	MAX. d	MIN. d	MAX.d	
Analog Switch	•			•					
Analog Signal Range ^e	V _{ANALOG}		Full	-	0	12	0	12	٧
Drain-Source On-Resistance	R _{DS(on)}	V+ = 10.8 V, V- = 0 V $I_S = 10 \text{ mA}, V_D = 2/9 \text{ V}$	Room Full	16	-	26 40	-	26 35	Ω
On resistance		ig = 10 mz, v _D = 2/3 v			-		-		
	I _{S(off)}		Room	-	-1	1	-1	1	
Switch Off Leakage Current		$V_D = 1/11 \text{ V}, V_S = 11/1 \text{ V}$	Full	-	-15	15	-10	10	
-	I _{D(off)}		Room	-	-1	1	-1	1	nA
	B(OII)		Full	-	-15	15	-10	10	
Channel On Leakage	I _{D(on)}	$V_S = V_D = 11/1 V$	Room	-	-1	1	-1	1	
Current	10(011)		Full	-	-15	15	-10	10	
Digital Control	_			1	T	T	ı		
Input Current, VIN Low	I _{IL}	V _{IN} under test = 0.8 V	Full	0.01	-1.5	1.5	-1	1	μA
Input Current, VIN High	I _{IH}	V _{IN} under test = 2.4 V	Full		-1.5	1.5	-1	1	μ/ι
Dynamic Characteristics									
Turn-On Time	+		Room	16	-	50	-	50	- ns
rum-on nine	t _{ON}	R_L = 300 Ω, C_L = 35 pF, V_S = 5 V, see figure 2	Full	-	-	70	-	60	
T O# Time -			Room	9	-	30	-	30	
Turn-Off Time	t _{OFF}		Full	-	-	48	-	40	
Break-Before-Make Time Delay	t _D	DG413L only, $V_S = 5 V$, $R_L = 300 \Omega$, $CL = 35 pF$	Room	5	-	-	-	-	
Charge Injection e	Q	$V_g = 0 \text{ V}, R_g = 0 \Omega, C_L = 10 \text{ nF}$	Room	6.6	-	-	-	-	рС
Off-Isolation e	OIRR		Room	68.4	-	-	-	-	
Channel-to-Channel Crosstalk ^e	X _{TALK}	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$	Room	114	-	-	-	-	dB
Source Off Capacitance e	C _{S(off)}		Room	5	-	-	-	-	
Drain Off Capacitance e	C _{D(off)}	f = 1 MHz	Room	6	-	-	-	-	рF
Channel-On Capacitance e	C _{D(on)}		Room	15	-	-	-	-	
Power Supplies	2(0.1)						1		
• •			Room	0.02	-	1	_	1	
Positive Supply Current	l+		Full	-	-	7.5	-	5	
			Room	-0.002	-1	-	-1	-	
Negative Supply Current	l-		Full	-	-7.5	-	-5	-	
Logic Supply Current	l.	$V_{IN} = 0 \text{ V or 5 V}$	Room	0.002	-	1	-	1	μA
Logic Supply Current	IL		Full	-	-	7.5	-	5	
Ground Current	la		Room	-0.002	-1	-	-1	-	
Ground Current	I _{GND}		Full	-	-7.5	-	-5	-	

- a. Refer to PROCESS OPTION FLOWCHART
- b. Room = 25 °C, full = as determined by the operating temperature suffix
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
- e. Guaranteed by design, not subject to production test
- f. V_{IN} = input voltage to perform proper function
- g. Leakage parameters are guaranteed by worst case test conditions and not subject to test



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SPECIFICATIONS a (Dual Supply ± 5 V)									
PARAMETER	SYMBOL			TYP. °	LIM	IFFIX IITS +125 °C	LIN	IFFIX IITS o +85 °C	UNIT
		V+ = 5 V, V- = -5 V $V_L = 5 V, V_{IN} = 2.4 V, 0.8 V^f$			MIN. d	MAX. d	MIN. d	MAX. d	
Analog Switch					I.				
Analog Signal Range ^e	V _{ANALOG}		Full	-	-5	5	-5	5	V
Drain-Source	R _{DS(on)}	V+ = 5 V, V- = -5 V,	Room	18	-	30	-	30	Ω
On-Resistance	20(0.1)	$I_S = 10 \text{ mA}, V_D = \pm 3.5 \text{ V}$	Full	-	-	42	-	37	
	I _{S(off)}		Room	-	-1	1	-1	1	
Switch Off	0(011)	V+ = 5.5, V- = -5.5 V,	Full	-	-15	15	-10	10	
Leakage Current ^g	I _{D(off)}	$V_D = \pm 4.5 \text{ V}, V_S = \pm 4.5 \text{ V}$	Room	-	-1	1	-1	1	nA
	·D(OII)		Full	-	-15	15	-10	10	
Channel On	l	V+ = 5.5 V, V- = -5.5 V,	Room	-	-1	1	-1	1	
Leakage Current ^g	I _{D(on)}	$V_S = V_D = \pm 4.5 \text{ V}$	Full	-	-15	15	-10	10	
Digital Control									
Input Current, V _{IN} Low ^e	I _{IL}	V _{IN} under test = 0.8 V	Full	0.05	-1.5	1.5	-1	1	
Input Current, V _{IN} High ^e	I _{IH}	V _{IN} under test = 2.4 V	Full	0.05	-1.5	1.5	-1	1	μA
Dynamic Characteristics									
T 0 T 0		$R_L = 300 \Omega$, $C_L = 35 pF$, $V_S = \pm 3.5 V$, see figure 2	Room	17	-	50	-	50	
Turn-On Time ^e	t _{ON}		Full	-	-	70	-	60	
			Room	12	-	35	-	35	
Turn-Off Time ^e	t _{OFF}		Full	-	-	50	-	40	ns
Break-Before-Make Time Delay ^e	t _D	DG413L only, $V_S = 3.5 \text{ V}$, $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$	Room	5	-	-	-	-	
Charge Injection ^e	Q	$V_g = 0 \text{ V}, R_g = 0 \Omega, C_L = 10 \text{ nF}$	Room	5.8	-	-	-	-	рС
Off Isolation e	OIRR	3	Room	68	-	-	-	-	
Channel-to-Channel Crosstalk ^e	X _{TALK}	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$	Room	113	-	-	-	-	dB
Source Off Capacitance e	C _{S(off)}		Room	5	-	-	-	-	
Drain Off Capacitance e	C _{D(off)}	f = 1 MHz	Room	6	-	-	-	-	рF
Channel On Capacitance e	C _{D(on)}		Room	14	-	-	-	-	
Power Supplies	. , ,								
o . o			Room	0.03	-	1	-	1	
Positive Supply Current e	I+		Full	-	-	7.5	-	5	
			Room	-0.002	-1	-	-1	-	
Negative Supply Current ^e	I-	.,	Full	-	-7.5	-	-5	-	
Lania Ormania Ormania	,	$V_{IN} = 0 \text{ V or 5 V}$	Room	0.002	-	1	-	1	μA
Logic Supply Current e	IL		Full	-	-	7.5	-	5	
			Room	-0.002	-1	-	-1	-	
Ground Current e	I _{GND}		Full	-	-7.5	-	-5	-	

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SPECIFICATIONS ^a (Single Supply 5 V)													
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED	TEMP.b 1	TEMP.b	TEMP.b	TEMP.b	TEMP.b	TYP. °	LIN	IFFIX IITS +125°C	LIM	IFFIX IITS o +85 °C	UNIT
		V+ = 5 V, V- = 0 V $V_L = 5 V, V_{IN} = 2.4 V, 0.8 V^f$			MIN. d	MAX. d	MIN. d	MAX. d					
Analog Switch													
Analog Signal Range ^e	V _{ANALOG}		Full	-	-	5	ı	5	>				
Drain-Source	B-a/	V+ = 4.5 V,	Room	36	-	50	ı	50	Ω				
On-Resistance e	R _{DS(on)}	$I_S = 5 \text{ mA}, V_D = 1 \text{ V}, 3.5 \text{ V}$	Full	-	-	88	-	75	22				
Dynamic Characteristics	Dynamic Characteristics												
Turn-On Time ^e	t _{ON}		Room	27	-	50	-	50					
Turn on time	ON	$R_L = 300 \Omega$, $C_L = 35 pF$,	Hot	-	-	90	-	60					
Turn-Off Time ^e	t _{OFF}	$V_S = 3.5 \text{ V}$, see figure 2	Room	15	-	30	-	30	ns				
Tuni on Timo	OFF	OFF	Hot	-	-	55	-	40					
Break-Before-Make Time Delay ^e	t _D	DG413L only, V_S = 3.5 V, R_L = 300 Ω , C_L = 35 pF	Room	11	-	-	-	-					
Charge Injection ^e	Q	$V_g = 0 \text{ V}, R_g = 0 \Omega, C_L = 10 \text{ nF}$	Room	3.3	-	-	-	-	рC				
Power Supplies													
Positive Supply Current e	l+		Room	0.02	-	1	ı	1					
Tositive Supply Current	IΤ		Hot	-	-	7.5	-	5					
Negative Supply Current e	I-		Room	-0.002	-1	-	-1	-					
Negative Supply Current	I-	$V_{IN} = 0 \text{ V or 5 V}$	Hot	-	-7.5	-	-5	-	μΑ				
Logic Supply Current ^e		VIN — U V OI U V	Room	0.002	-	1	ı	1	μΛ				
Logic Supply Current	lι		Hot	-	-	7.5	ı	5					
Ground Current e	I _{GND}		Room	-0.002	-1	-	-1	-					
Ground Gurrent	GND		Hot	-	-7.5	-	-5	-					

- a. Refer to PROCESS OPTION FLOWCHART
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- g. Leakage parameters are guaranteed by worst case test conditions and not subject to test

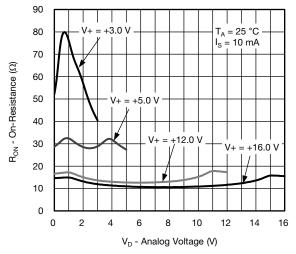


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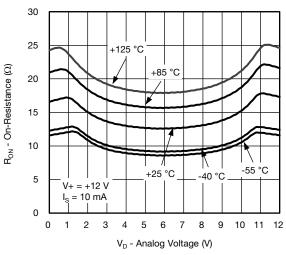
SPECIFICATIONS a (Single Supply 3 V)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED	TEMP. b TYP.		ASUFFIX LIMITS -55 °C to +125 °C		LIM	IFFIX IITS D +85 °C	UNIT
		V+ = 3 V, V- = 0 V $V_L = 3 V, V_{IN} = 0.4 V, 2.0 V^f$			MIN. d	MAX. d	MIN. d	MAX. d	
Analog Switch	•								
Analog Signal Range ^e	V _{ANALOG}		Full	1	0	3	0	3	V
Drain-Source On-Resistance	R _{DS(on)}	V+ = 2.7 V, V- = 0 V, $I_S = 5 \text{ mA}, V_D = 0.5, 2.2 \text{ V}$	Room Full	106	-	130 150	-	130 140	Ω
			Room	-	-1	1	-1	1	
Switch Off	I _{S(off)}	V+ = 3.3, V- = 0 V,	Full	-	-15	15	-10	10	
Leakage Current ^g		$V_D = 1, 2 \text{ V}, V_S = 2, 1 \text{ V}$	Room	-	-1	1	-1	1	A
	I _{D(off)}		Full	-	-15	15	-10	10	nA
Channel On		V+ = 3.3 V, V- = 0 V,	Room	-	-1	1	-1	1	
Leakage Current ^g	I _{D(on)}	$V_S = V_D = 1, 2 V$	Full	-	-15	15	-10	10	
Digital Control									
Input Current, V _{IN} Low	I _{IL}	V _{IN} under test = 0.4 V	Full	0.005	-1.5	1.5	-1	1	μA
Input Current, V _{IN} High	I _{IH}	V _{IN} under test = 2.4 V	Full	0.005	-1.5	1.5	-1	1	μΛ
Dynamic Characteristics									
Turn-On Time	t _{ON}		Room	57	-	85	-	85	
Turri on Time	UN	$R_L = 300 \Omega, C_L = 35 pF,$	Full	-	-	150	-	110	
Turn-Off Time	t _{OFF}	$V_S = 1.5 V$, see figure 2	Room	25	-	60	-	60	ns
Tuni on Time	OFF		Full	-	-	100	-	85	
Break-Before-Make Time Delay	t _D	DG413L only, $V_S = 1.5 \text{ V}$, $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$	Room	24	-	-	-	-	
Charge Injection ^e	Q	$V_g = 0 \text{ V}, R_g = 0 \Omega, C_L = 10 \text{ nF}$	Room	2	-	-	-	ı	рC
Off Isolation e	OIRR		Room	68	-	-	-	1	
Channel-to-Channel Crosstalk ^e	X _{TALK}	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$	Room	107	-	-	-	-	dB
Source Off Capacitance e	C _{S(off)}		Room	6	-	-	-	-	
Drain Off Capacitance e	C _{D(off)}	f = 1 MHz	Room	7	-	-	-	-	pF
Channel On Capacitance e	C _{D(on)}		Room	15	-	-	-	-	

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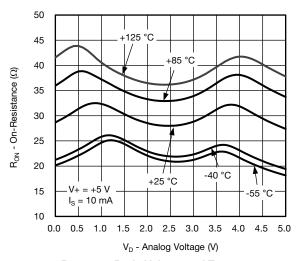
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



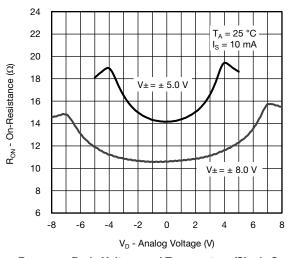
R_{DS(on)} vs. Drain Voltage (Single Supply)



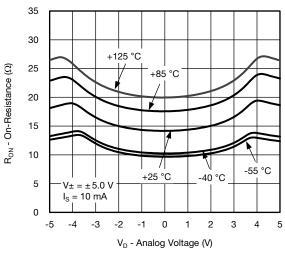
R_{DS(on)} vs. Drain Voltage and Temperature



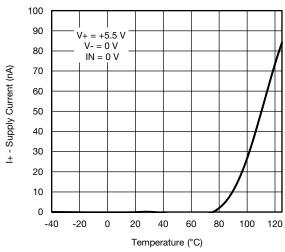
 $R_{DS(on)}$ vs. Drain Voltage and Temperature



R_{DS(on)} vs. Drain Voltage and Temperature (Single Supply)

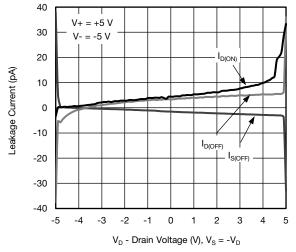


Supply Current vs. Temperature

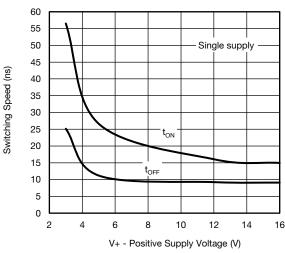


Switching Time vs. Single Supply

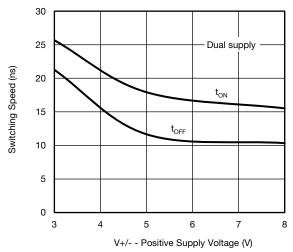
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



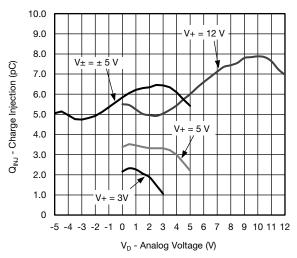
Leakage Current vs. Drain Voltage



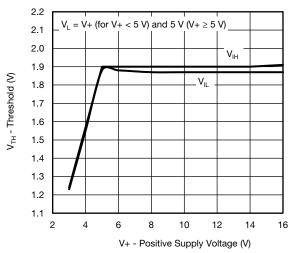
Switching Time vs. Single Supply Voltage



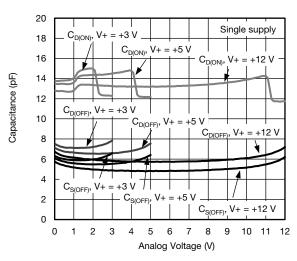
Switching Time vs. Dual Supply Voltage



Charge Injection vs. Drain Voltage



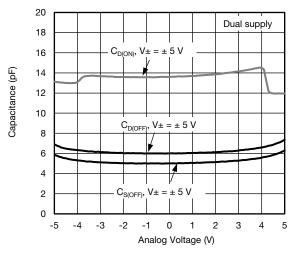
Threshold vs. Single Supply Current

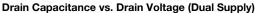


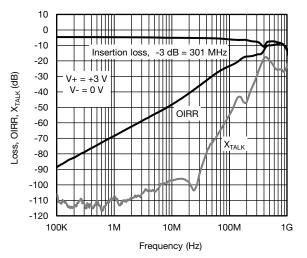
Drain Capacitance vs. Drain Voltage (Single Supply)

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

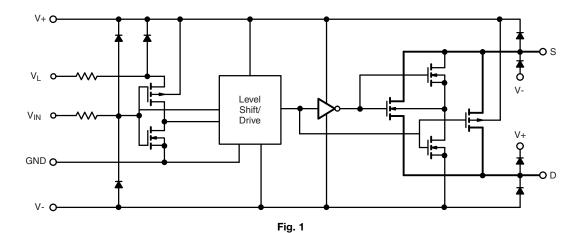




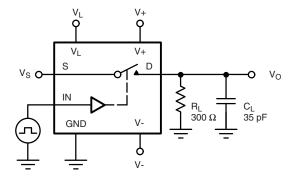


Insertion Loss, Off Isolation and Crosstalk vs. Frequency

SCHEMATIC DIAGRAM (Typical Channel)

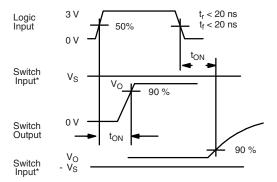


TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_0 = V_S$$
 $R_L + r_{DS(on)}$



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Fig. 2 - Switching Time

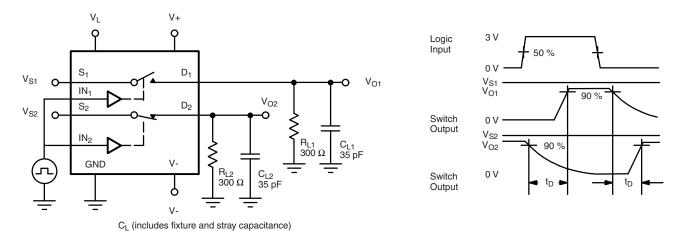
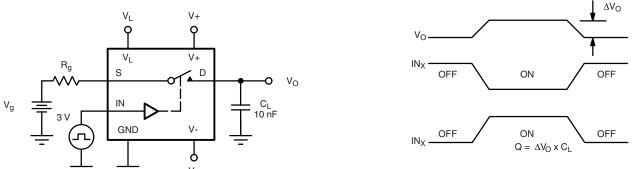


Fig. 3 - Break-Before-Make (DG413LE)



 $\ensuremath{\mathsf{IN}_X}$ dependent on switch configuration Input polarity determined by sense of switch.

Fig. 4 - Charge Injection

TEST CIRCUITS

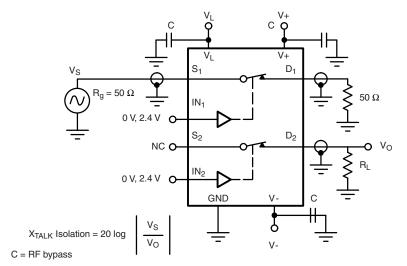


Fig. 5 - Crosstalk

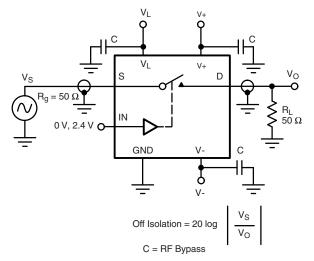


Fig. 6 - Off-Isolation

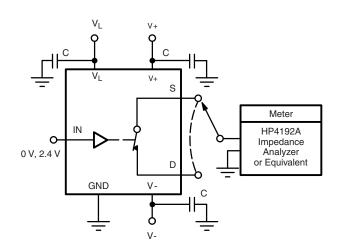
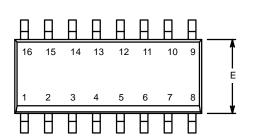


Fig. 7 - Source / Drain Capacitances

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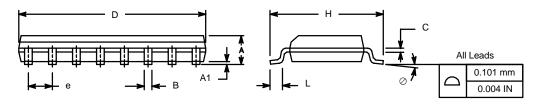
SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012



	MILLIM	MILLIMETERS		HES			
Dim	Min	Max	Min	Max			
Α	1.35	1.75	0.053	0.069			
A ₁	0.10	0.20	0.004	0.008			
В	0.38	0.51	0.015	0.020			
С	0.18	0.23	0.007	0.009			
D	9.80	10.00	0.385	0.393			
E	3.80	4.00	0.149	0.157			
е	1.27	BSC	0.050	BSC			
Н	5.80	6.20	0.228	0.244			
L	0.50	0.93	0.020	0.037			
0	0°	8°	0°	8°			
FCN: S-03946—Rev. F. 09-Jul-01							

ECN: S-03946—Rev. F, 09-Jul-01

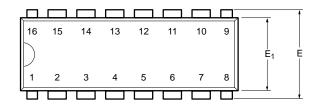
DWG: 5300

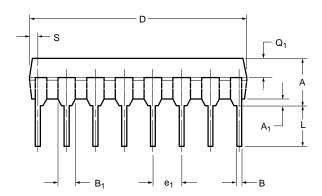


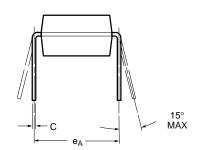
Document Number: 71194 www.vishay.com 02-Jul-01 sww.vishay.com



PDIP: 16-LEAD





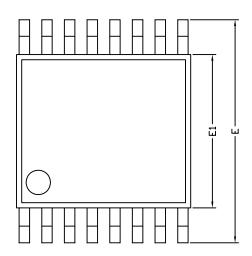


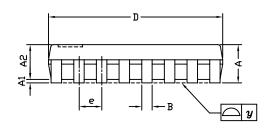
	MILLIM	IETERS	INCHES			
Dim	Min	Max	Min	Max		
Α	3.81	5.08	0.150	0.200		
A ₁	0.38	1.27	0.015	0.050		
В	0.38	0.51	0.015	0.020		
B ₁	0.89	1.65	0.035	0.065		
С	0.20	0.30	0.008	0.012		
D	18.93	21.33	0.745	0.840		
Е	7.62	8.26	0.300	0.325		
E ₁	5.59	7.11	0.220	0.280		
e ₁	2.29	2.79	0.090	0.110		
e _A	7.37	7.87	0.290	0.310		
L	2.79	3.81	0.110	0.150		
Q_1	1.27	2.03	0.050	0.080		
S	0.38	1.52	.015	0.060		
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482						

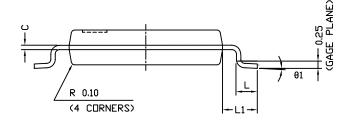
Document Number: 71261 www.vishay.com 06-Jul-01 sum.vishay.com



TSSOP: 16-LEAD







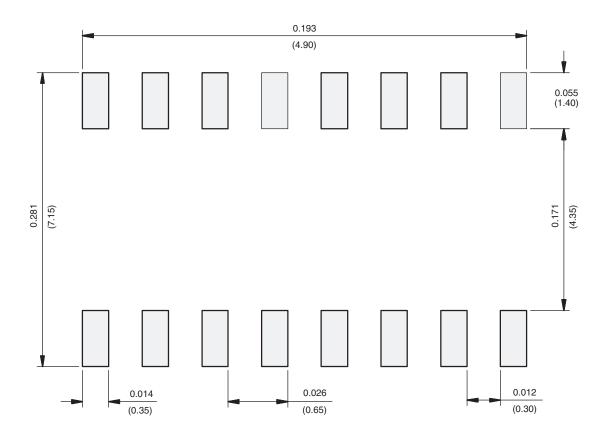
	DIMENSIONS IN MILLIMETERS						
Symbols	Min	Nom	Max				
Α	-	1.10	1.20				
A1	0.05	0.10	0.15				
A2	=	1.00	1.05				
В	0.22	0.28	0.38				
С	=	0.127	-				
D	4.90	5.00	5.10				
E	6.10	6.40	6.70				
E1	4.30	4.40	4.50				
е	-	0.65	-				
L	0.50	0.60	0.70				
L1	0.90	1.00	1.10				
у	=	-	0.10				
θ1	0°	3°	6°				
ECN: S-61920-Rev. D. 23-0	Oct-06						

DWG: 5624

Document Number: 74417 www.vishay.com 23-Oct-06



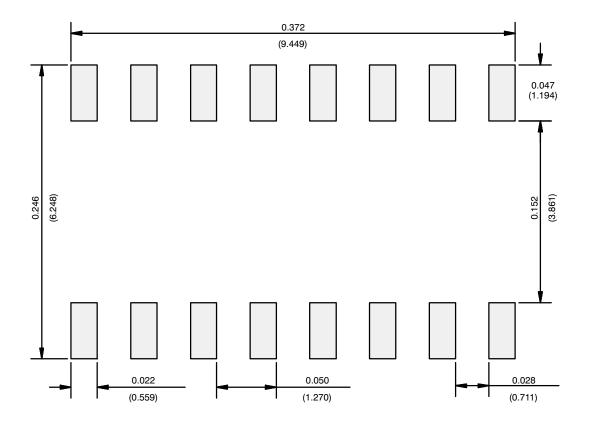
RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads Dimensions in inches (mm)



RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

APPLICATION NOTE

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Vishay

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