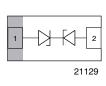
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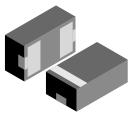
GREEN



Vishay Semiconductors

Bidirectional Symmetrical (BiSy) Single Line ESD Protection Diode in LLP1006-2M





20855

MARKING (example only)



Bar = pin 1 marking X = date code

Y = type code (see table below)

LINKS TO ADDITIONAL RESOURCES





FEATURES

- Ultra compact LLP1006-2M package
- Low package height < 0.4 mm
- 1-line ESD protection
- Working range ± 5.5 V
- Low leakage current < 0.1 μA
- Low load capacitance C_D = 10 pF
- ESD immunity acc. IEC 61000-4-2 ± 30 kV contact discharge
 - ± 30 kV air discharge
- Soldering can be checked by standard vision inspection, no X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

ORDERING INFORMATION					
DEVICE NAME ORDERING CODE		TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY		
VCUT05B1-DD1	VCUT05B1-DD1-G-08	8000	8000		

PACKAGE DATA							
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS	
VCUT05B1-DD1	LLP1006-2M	Р	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C	

ABSOLUTE MAXIMUM RATINGS VCUT05B1-DD1						
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT		
Peak pulse current	Acc. IEC 61000-4-5, 8/20 µs/single shot	I _{PPM}	3	А		
Peak pulse power	Pin 1 to pin 2 acc. IEC 61000-4-5; t _p = 8/20 μs; single shot	P _{PP}	38	W		
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V _{ESD}	± 30	kV		
	Air discharge acc. IEC 61000-4-2; 10 pulses	V _{ESD}	± 30	KV		
Operating temperature	Junction temperature	TJ	-55 to +145	°C		
Storage temperature		T _{stg}	-55 to +150	°C		

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.

Rev. 2.0, 19-Nov-2021 **1** Document Number: 81149 For technical questions, contact: <u>ESDprotection@vishay.com</u>

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CUT THE SPIKES WITH VCUT05B1-DD1

The VCUT05B1-DD1 is a Bidirectional and Symmetrical (BiSy) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VCUT05B1-DD1 offers a high isolation (low leakage current, low capacitance) within the specified working range. Due to the short leads and small package size of the tiny LLP1006-2M package the line inductance is very low, so that fast transients like and ESD strike can be clamped with minimal over- or undershoots.

ELECTRICAL CHARACTERISTICS VCUT05B1-DD1 (T _{amb} = 25 °C, unless otherwise specified)							
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Protection paths	Number of lines which can be protected	N _{channel}	-	-	1	lines	
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	5.5	V	
Reverse voltage	At I = 0.1 μA	V_R	5.5	=.	-	V	
Reverse current	At V = 5.5 V	I _R	-	-	0.1	μΑ	
Reverse breakdown voltage	At I = 1 mA	V_{BR}	6	7.5	8.5	V	
Reverse clamping voltage	At I _{PP} = 1 A	V _C	-	8.3	10.5	V	
	At I _{PP} = I _{PPM} = 3 A	V _C	-	10.3	12.5	V	
Capacitance	At V = 0 V; f = 1 MHz	C _D	-	10	13	pF	
	At V = 2.5 V; f = 1 MHz	C _D	-	8	-	pF	

TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

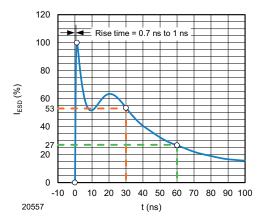


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω /150 pF)

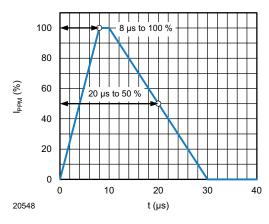


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

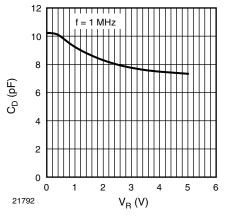


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

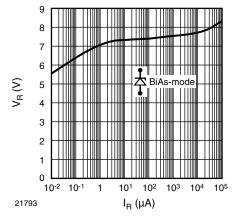


Fig. 4 - Typical Reverse Voltage $V_{\mbox{\scriptsize R}}$ vs. Reverse Current $I_{\mbox{\scriptsize R}}$

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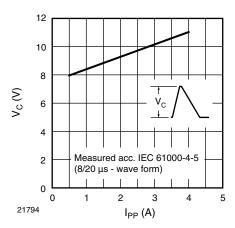


Fig. 5 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

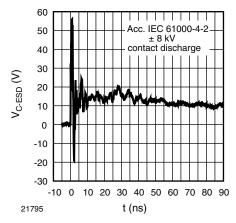


Fig. 6 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

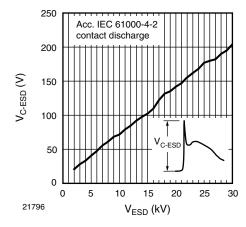
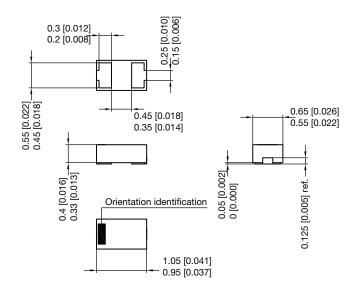


Fig. 7 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

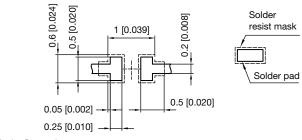
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PACKAGE DIMENSIONS in millimeters (inches): LLP1006-2M



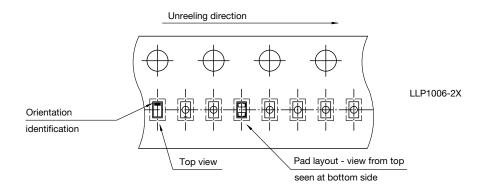
Foot print recommendation:



Pad Design Patented: (@US 9.018.537 B2)

Document no.: S8-V-3906.04-005 (4) Rev. 7 - Date: 11.May 2016

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Rev. 2.0, 19-Nov-2021 4 Document Number: 81149

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