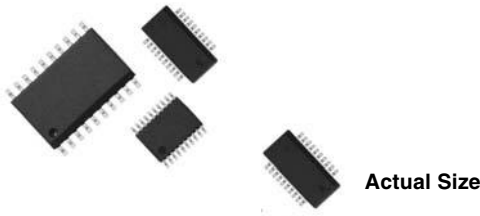




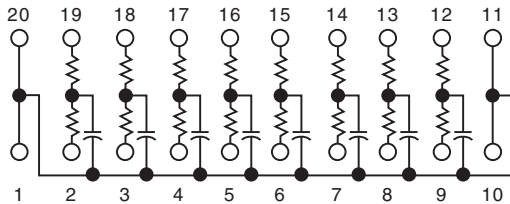
## 25 mil or 50 mil Pitch, T-Filter Thin Film Surface Mount Resistor/Capacitor Network



Small outline, surface mount, EMI/RFI reduction

Vishay Thin Film's T-filter network is an integrated thin film network on a single die. Noise suppression is at a maximum with the use of thin film technology. The T-filter network, schematic AA is designed to suppress EMI/RFI noise with such applications as I/O ports of personal computers and peripherals, workstations and local area networks. With a rugged molded case to protect the circuit from the environment and an integrated thin film network this product is your choice when reduced size, improved accuracy and surface mount capability are your goals. Available packages SOIC, SSOP and TSSOP.

### SCHEMATIC AA



### FEATURES

- Resistors and capacitors on a single chip
- Saves board space
- Reduces total assembly costs
- Uniform performance characteristics
- UL 94 V-0 flame resistant
- Rugged, molded case construction
- VTSRC - JEDEC M0-153AC
- VSSRC - JEDEC M0-137AD
- VSORC - JEDEC MS-013AC
- Compliant to RoHS Directive 2002/95/EC



### TYPICAL PERFORMANCE

	TCR	TOLERANCE
<b>RESISTOR</b>	200	10 %
	TCC	TOLERANCE
<b>CAPACITOR</b>	200	20 %

### STANDARD VALUES

MODELS			R (Ω)	C (pF)
VSORC	VSSRC	VTSRC		
	X		10	100
	X		25	200
X			100	390

STANDARD ELECTRICAL SPECIFICATIONS		
TEST	SPECIFICATIONS	CONDITIONS
Material	Tantalum nitride on silicon	-
Pin/Lead Number	20	-
Resistance Range	10 Ω to 750 Ω	-
TCR: Absolute	± 200 ppm/°C	0 °C to + 70 °C
TCR: Tracking	± 10 ppm/°C	-
Tolerance: Absolute	± 10 % standard (R), ± 20 % standard (C)	At 1 MHz and V <sub>RMS</sub> over + 10 °C to + 70 °C
Power Rating: Resistor	100 mW	-
Power Rating: Package	(T)SSOP: 1 W, SOIC: 1.2 W	See derating curve
Stability: Ratio	± 2 %	1000 h
Operating Temperature Range	0 °C to + 70 °C	-
Storage Temperature Range	- 55 °C to + 125 °C	-
Capacitance Range	TSSOP: 10 pF to 150 pF, SOIC/SSOP: 10 pF to 250 pF	-
ESD Protection	> 2 kV	MIL-STD-883, method 3015
Breakdown Voltage	35 V to 50 V	-

**DIMENSIONS** in inches and millimeters

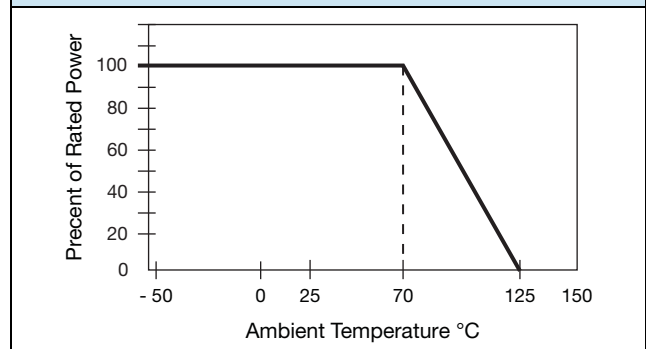

DIMENSION	JEDEC M0-153AC, VTSRC20-AA		JEDEC M0-137AD, VSSRC20-AA		JEDEC MS-013AC, VSORC20-AA	
	INCHES	MILLIMETERS	INCHES	MILLIMETERS	INCHES	MILLIMETERS
A	0.256 ± 0.003	6.5 ± 0.08	0.344 max.	8.74 max.	0.500 ± 0.010	12.7 ± 0.25
B (ref.)	0.025	0.65	0.025	0.64	0.050	1.27
C (ref.)	0.0087	0.22	0.010	0.25	0.016	0.41
D	0.004	0.10	0.006	0.15	0.008	0.20
E (typ.)	0.024	0.61	0.025	0.64	0.030	0.76
F	0.173 ± 0.003	4.39 ± 0.08	0.154 ± 0.003	3.9	0.293 ± 0.003	7.44
G	0.015 x 45°	0.38	0.015 x 45°	0.38	0.025 x 45°	0.64
H	0.252 ± 0.005	6.4 ± 0.13	0.236 ± 0.008	6.0 ± 0.20	0.406 ± 0.005	10.31
J (ref.)	0.005	0.13	0.010	0.25	0.010	0.25
W	0.043 ± 0.005	1.09 ± 0.13	0.064 ± 0.005	1.6	0.100 ± 0.005	2.59

**IMPRINTING**

VSORC, VSSRC, VTSRC	20	AA	XXX	/	XXX
MODEL	PIN COUNT	SCHEMATIC	RESISTANCE Code: e.g. 100 = 10 W	/	CAPACITANCE Code: e.g. 101 = 100 pF
		XXXX Date code			Optional marking

**MECHANICAL SPECIFICATIONS**

Resistive Element	Tantalum nitride
Substrate Material	Silicon
Body	Molded epoxy
Terminals	Copper alloy
Plating	100 % matte Sn
Lead Coplanarity	0.0005"
Marking Resistance to Solvents	Permanency testing per MIL-STD-202, method 215

**DERATING CURVE**

**PACKING INFORMATION**

MODEL	LEADS	TAPE AND REEL	TUBES
JEDEC M0-153AC, VTSRC (TSSOP)	20	2500	74
JEDEC M0-137AD, VSSRC (SSOP)	20	2500	55
JEDEC MS-013AC, VSORC (SOIC)	20	1000	38



GLOBAL PART NUMBER INFORMATION																
New Global Part Numbering: VTSRC20AA330470TF																
V	T	S	R	C	2	0	A	A	3	3	0	4	7	0	T	F
GLOBAL MODEL				NUMBER OF LEADS/ SCHEMATICS				RESISTANCE AND TOLERANCE/ CAPACITANCE AND TOLERANCE				PACKAGING				
VTSRC VSSRC VSORC				20AA				xxxxyy First 2 digits are significant figures. Last digit specifies number of zeros to follow.  K = 10 % resistance tol. fixed M = 20 % capacitor tol. fixed				UF = TUBED  TAPE AND REEL TF = Full reels				
Historical Part Number example: VTSRC20AA330K470MT/R (for reference purposes only)																
VTSRC		20		AA		330K		470M		T/R						
MODEL		NUMBER OF LEADS		SCHEMATIC		RESISTANCE		TOLERANCE		PACKAGING						



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