

COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET
Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(ON)}$ Max	I_D Max $T_A = +25^\circ\text{C}$
Q1 N-Channel	30V	460m Ω @ $V_{GS} = 4.5\text{V}$	1.1A
		560m Ω @ $V_{GS} = 2.5\text{V}$	0.9A
Q2 P-Channel	-30V	1000m Ω @ $V_{GS} = -4.5\text{V}$	-0.7A
		1500m Ω @ $V_{GS} = -2.5\text{V}$	-0.5A

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

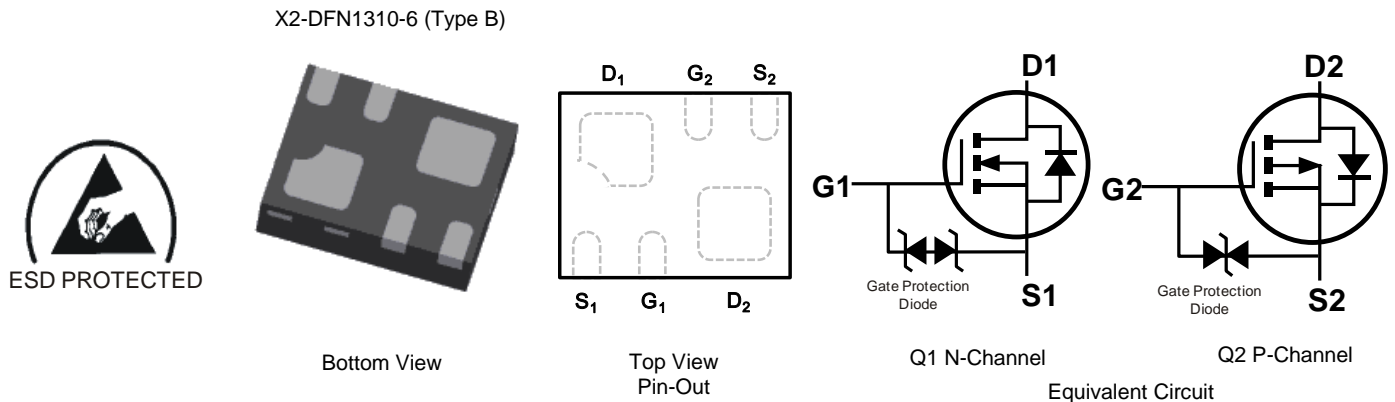
- Motor Control
- Power Management Functions
- Backlighting

Features and Benefits

- Footprint of just 1.3 mm²
- Ultra Low Profile Package – 0.35mm Profile
- Low Gate Threshold Voltage
- Fast Switching Speed
- Ultra-Small Surface Mount Package
- **ESD Protected Gate**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

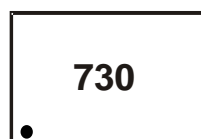
Mechanical Data

- Case: X2-DFN1310-6 (Type B)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 $\text{\textcircled{4}}$
- Weight: 0.002 grams (Approximate)


Ordering Information (Note 4)

Part Number	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DMC3730UFL3-7	7	8	3,000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information


730 = Product Type Marking Code

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1	Q2	Unit
Drain-Source Voltage			V _{DSS}	30	-30	V
Gate-Source Voltage			V _{GSS}	±8	±8	V
Continuous Drain Current (Note 5) V _{GS} = 4.5V	Steady State	T _A = +25°C	I _D	1.1	-0.7	A
		T _A = +70°C		0.8	-0.6	

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T _A = +25°C	P _D	0.39	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	R _{θJA}	330	°C/W
Total Power Dissipation (Note 6)	T _A = +25°C	P _D	0.81	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R _{θJA}	156	°C/W
Thermal Resistance, Junction to Case (Note 6)		R _{θJC}	51	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (N-Channel Q1) (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	1	μA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±10	μA	V _{GS} = ±8V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	0.45	0.72	0.95	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	291	460	mΩ	V _{GS} = 4.5V, I _D = 200mA
			335	560		V _{GS} = 2.5V, I _D = 100mA
			398	730		V _{GS} = 1.8V, I _D = 75mA
Diode Forward Voltage	V _{SD}	—	0.7	1.2	V	V _{GS} = 0V, I _S = 300mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{ISS}	—	65.9	—	pF	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{OSS}	—	5.8	—	pF	
Reverse Transfer Capacitance	C _{RSS}	—	4.3	—	pF	
Gate Resistance	R _G	—	64	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _G	—	0.9	—	nC	V _{DS} = 15V, V _{GS} = 4.5V, I _D = 1A
Gate-Source Charge	Q _{GS}	—	0.1	—	nC	
Gate-Drain Charge	Q _{GD}	—	0.1	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	3.6	—	ns	V _{GS} = 4.5V, V _{DS} = 10V, R _G = 6Ω, I _D = 1A
Turn-On Rise Time	t _R	—	6.4	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	19.4	—	ns	
Turn-Off Fall Time	t _F	—	6.9	—	ns	

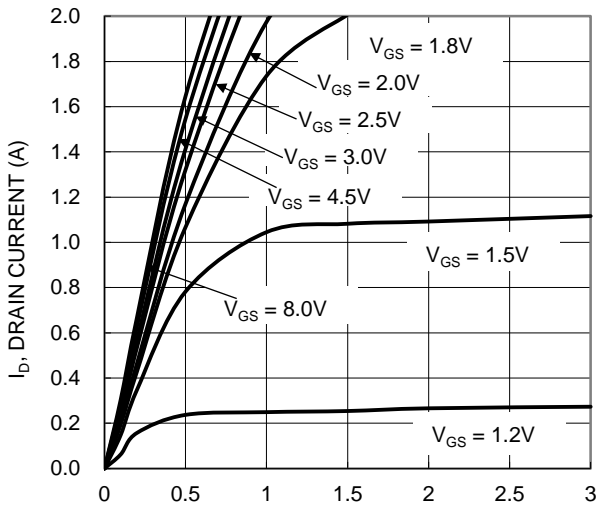
- Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

Electrical Characteristics (P-Channel Q2) (@T_A = +25°C, unless otherwise specified.)

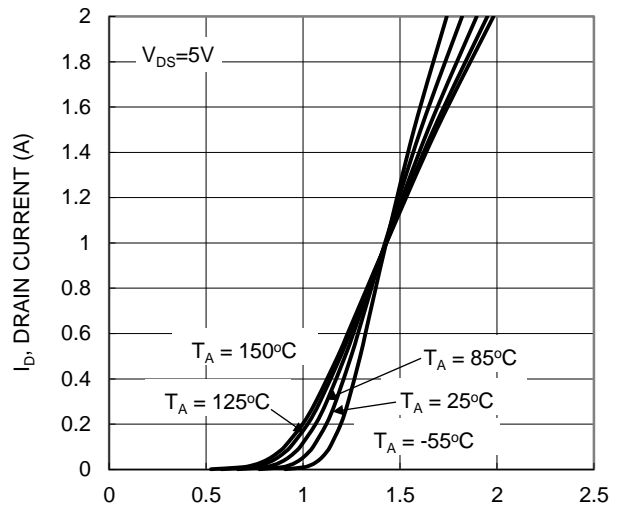
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-30	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	-1	μA	V _{DS} = -30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±10	μA	V _{GS} = ±8V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	-0.5	-0.78	-1.1	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	644	1,000	mΩ	V _{GS} = -4.5V, I _D = -400mA
			769	1,500		V _{GS} = -2.5V, I _D = -200mA
			949	2,000		V _{GS} = -1.8V, I _D = -100mA
Diode Forward Voltage	V _{SD}	—	-0.8	-1.2	V	V _{GS} = 0V, I _S = -300mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{ISS}	—	83	—	pF	V _{DS} = -30V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{OSS}	—	6.2	—	pF	
Reverse Transfer Capacitance	C _{RSS}	—	4.1	—	pF	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Gate Resistance	R _G	—	177	—	Ω	
Total Gate Charge	Q _G	—	0.9	—	nC	V _{DS} = -15V, V _{GS} = -4.5V, I _D = -1A
Gate-Source Charge	Q _{GS}	—	0.1	—	nC	
Gate-Drain Charge	Q _{GD}	—	0.2	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	6.0	—	ns	V _{GS} = -4.5V, V _{DS} = -10V, R _G = 6Ω, I _D = -1A
Turn-On Rise Time	t _R	—	11.7	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	28.9	—	ns	
Turn-Off Fall Time	t _F	—	15.5	—	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

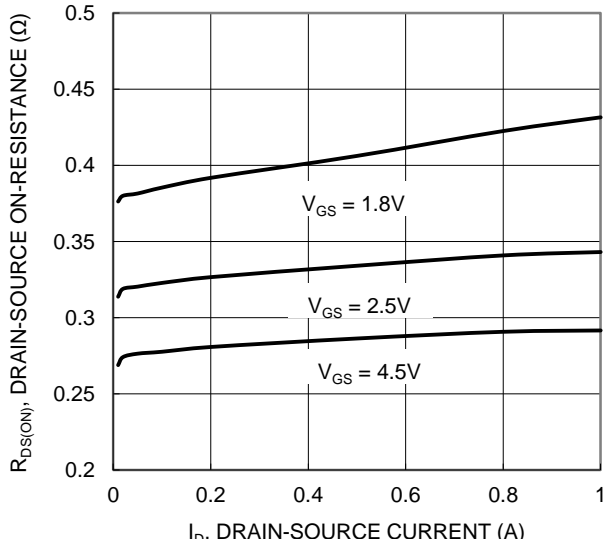
Typical Characteristics (N-Channel)



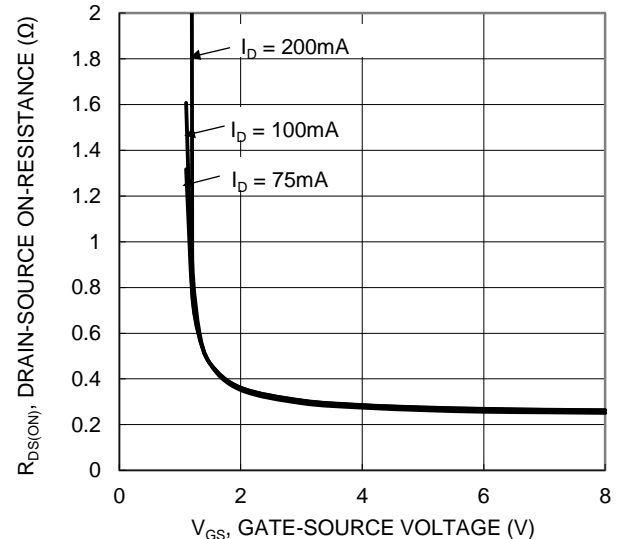
V_{DS} , DRAIN-SOURCE VOLTAGE (V)
Figure 1. Typical Output Characteristic



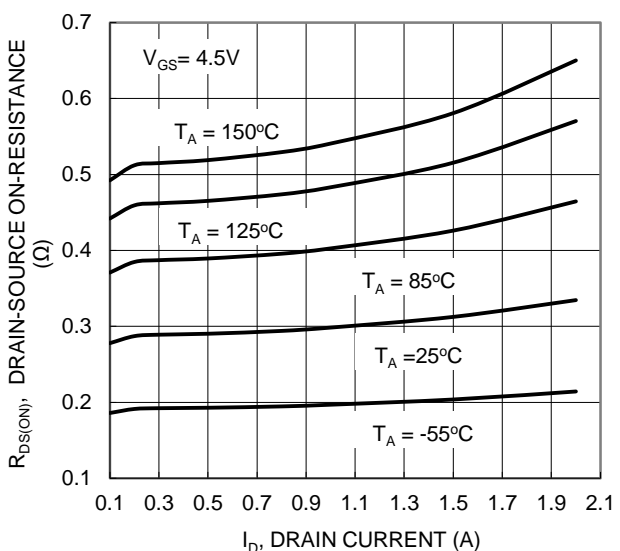
V_{GS} , GATE-SOURCE VOLTAGE (V)
Figure 2. Typical Transfer Characteristic



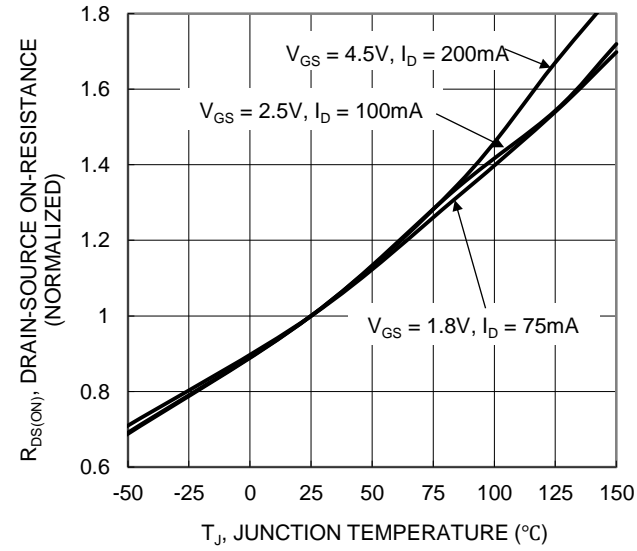
I_D , DRAIN-SOURCE CURRENT (A)
Figure 3. Typical On-Resistance vs Drain Current and Gate Voltage



V_{GS} , GATE-SOURCE VOLTAGE (V)
Figure 4. Typical Transfer Characteristic



I_D , DRAIN CURRENT (A)
Figure 5. Typical On-Resistance vs Drain Current and Junction Temperature



T_J , JUNCTION TEMPERATURE ($^{\circ}C$)
Figure 6. On-Resistance Variation with Junction Temperature

Typical Characteristics (N-Channel) (Continued)

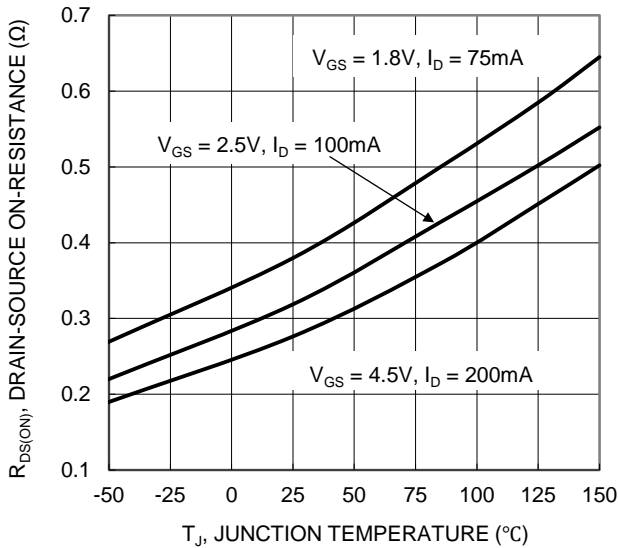


Figure 7. On-Resistance Variation with Junction Temperature

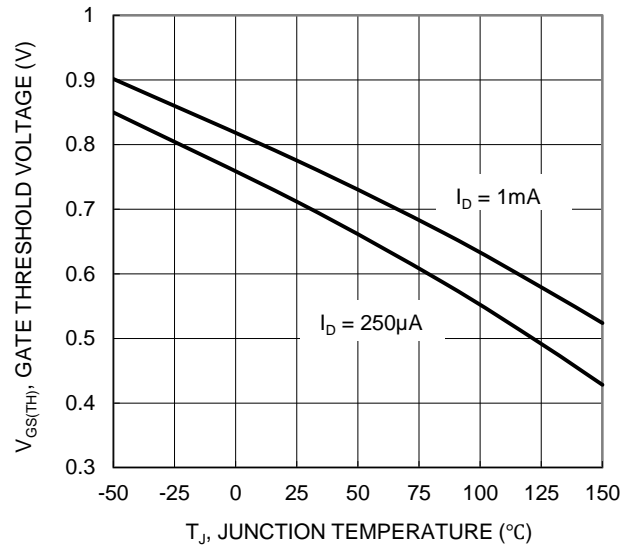


Figure 8. Gate Threshold Variation vs Junction Temperature

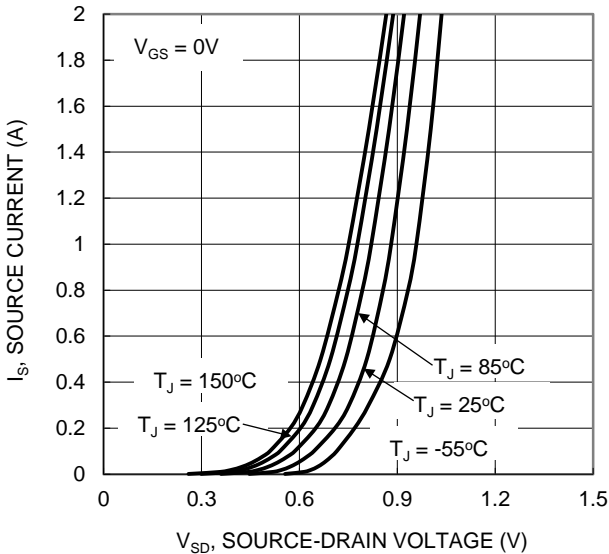


Figure 9. Diode Forward Voltage vs. Current

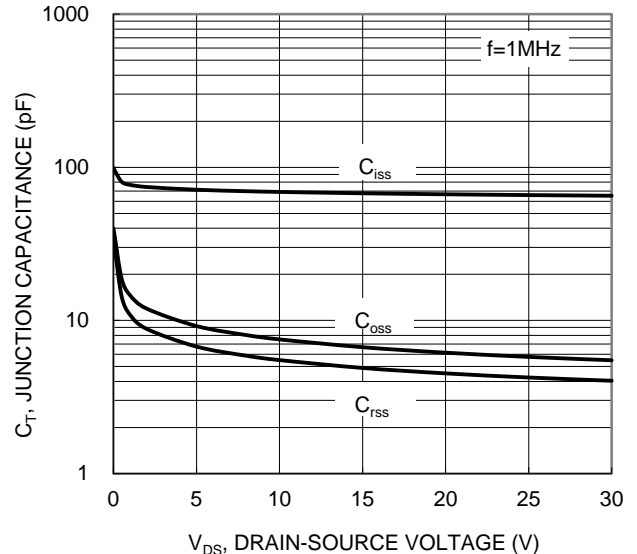


Figure 10. Typical Junction Capacitance

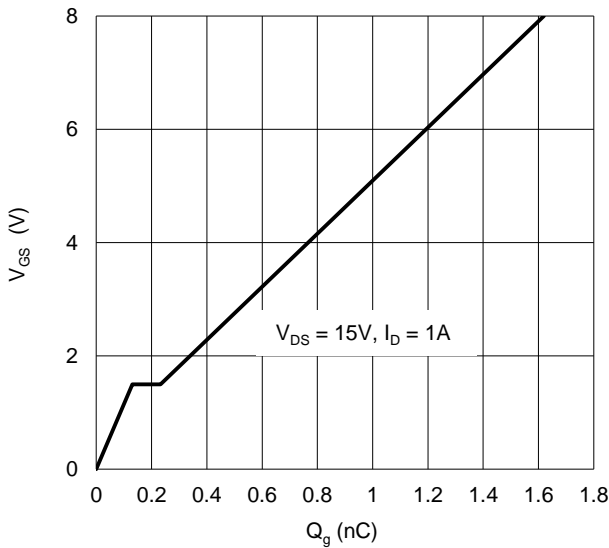


Figure 11. Gate Charge

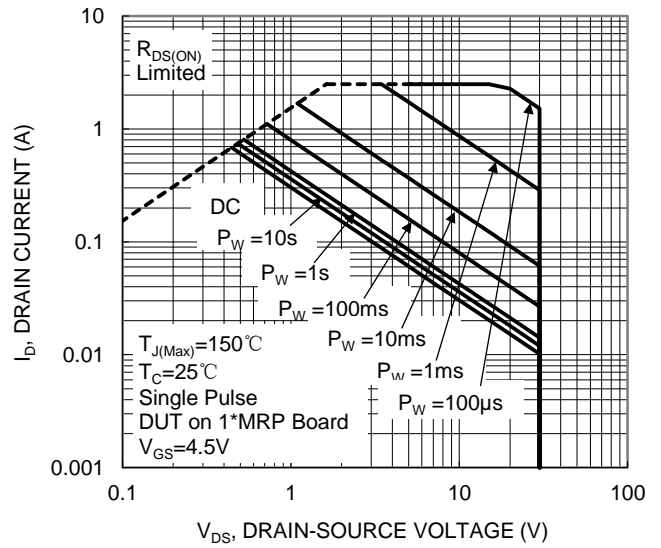


Figure 12. SOA, Safe Operation Area

Typical Characteristics (P-Channel)

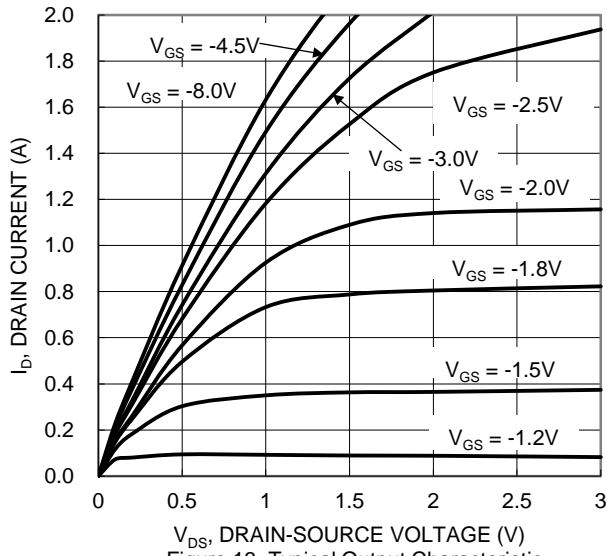


Figure 13. Typical Output Characteristic

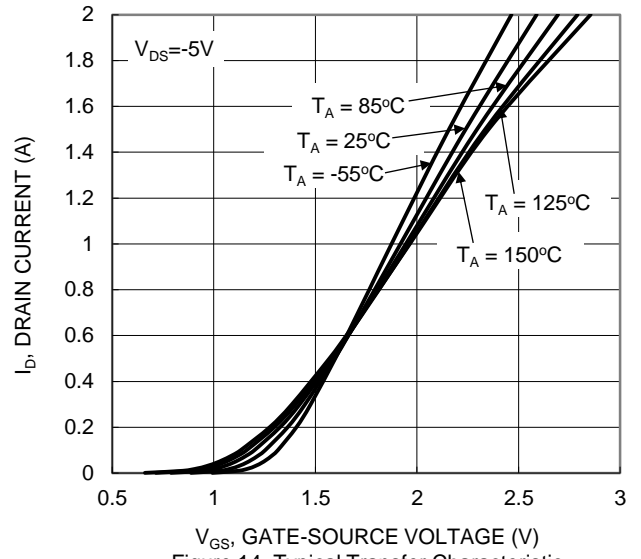


Figure 14. Typical Transfer Characteristic

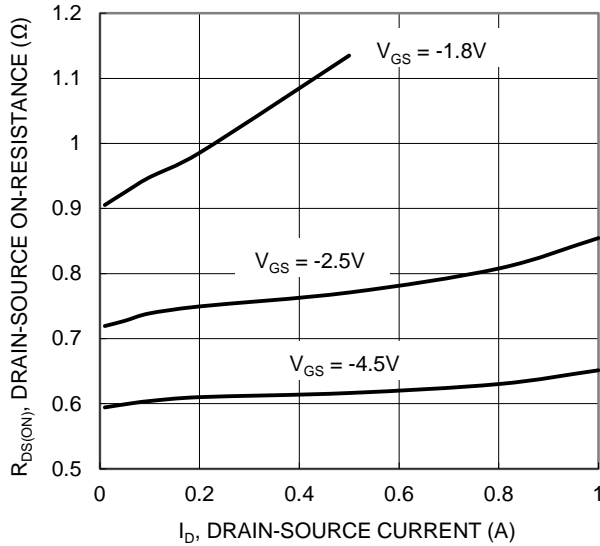


Figure 15. Typical On-Resistance vs Drain Current and Gate Voltage

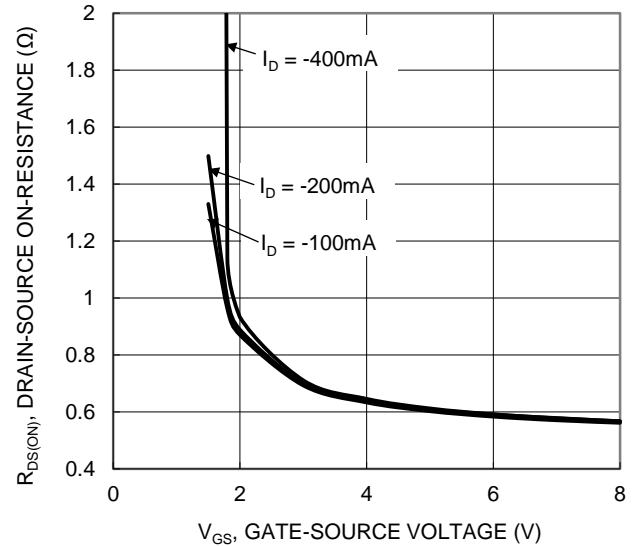


Figure 16. Typical Transfer Characteristic

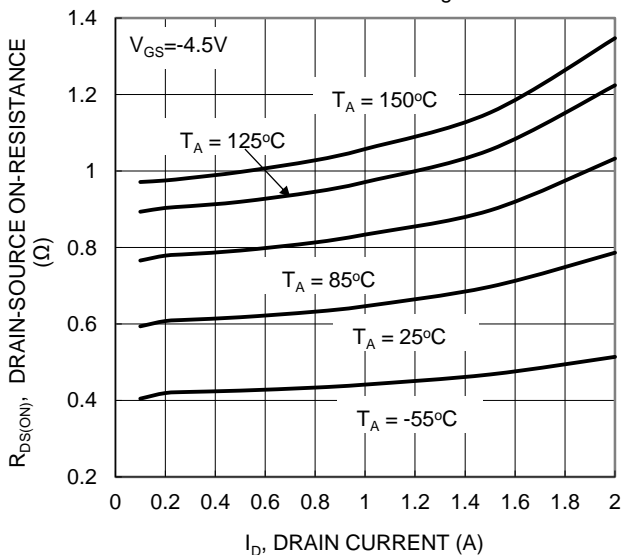


Figure 17. Typical On-Resistance vs Drain Current and Junction Temperature

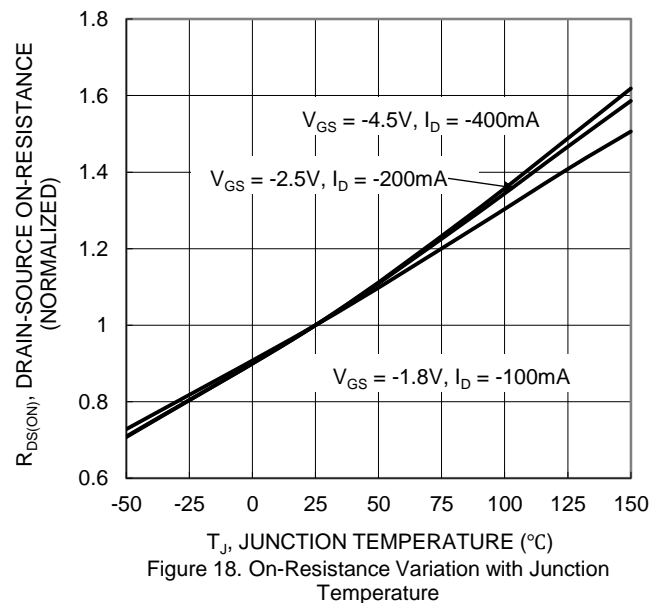


Figure 18. On-Resistance Variation with Junction Temperature

Typical Characteristics (P-Channel) (Continued)

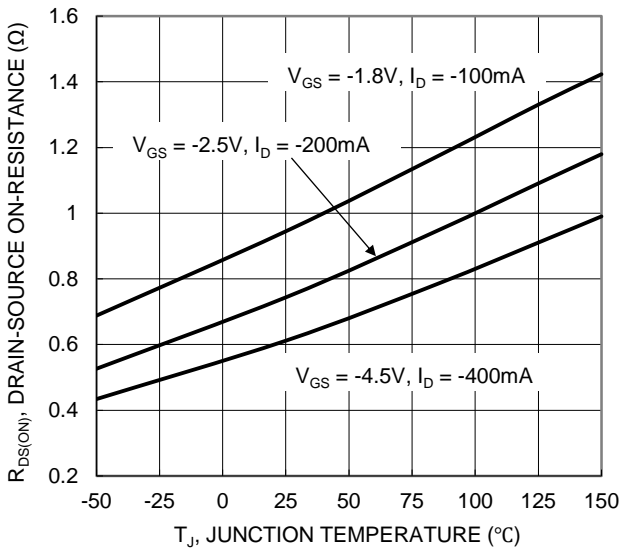


Figure 19. On-Resistance Variation with Junction Temperature

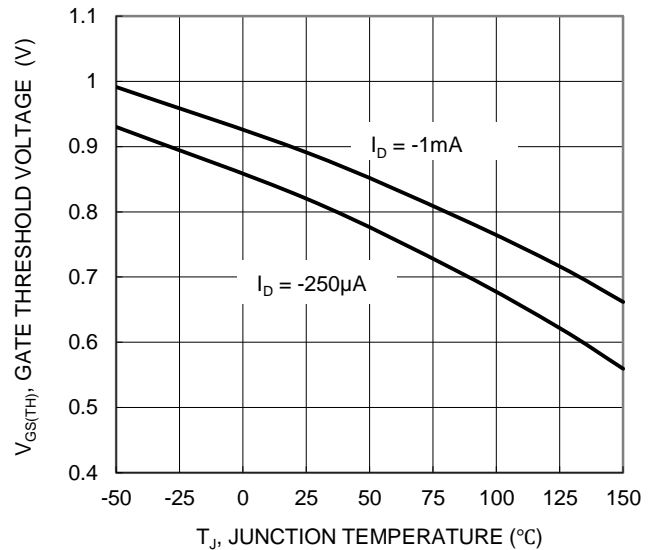


Figure 20. Gate Threshold Variation vs Junction Temperature

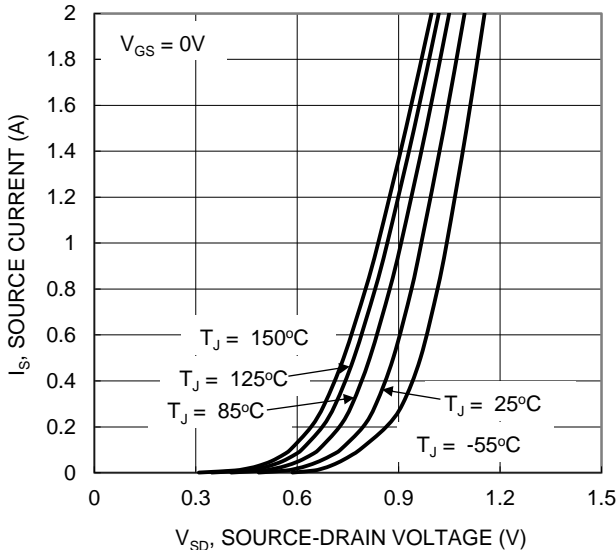


Figure 21. Diode Forward Voltage vs. Current

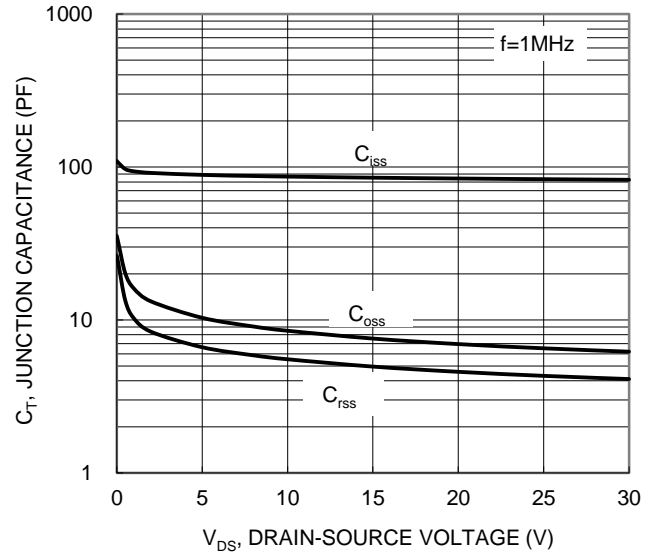


Figure 22. Typical Junction Capacitance

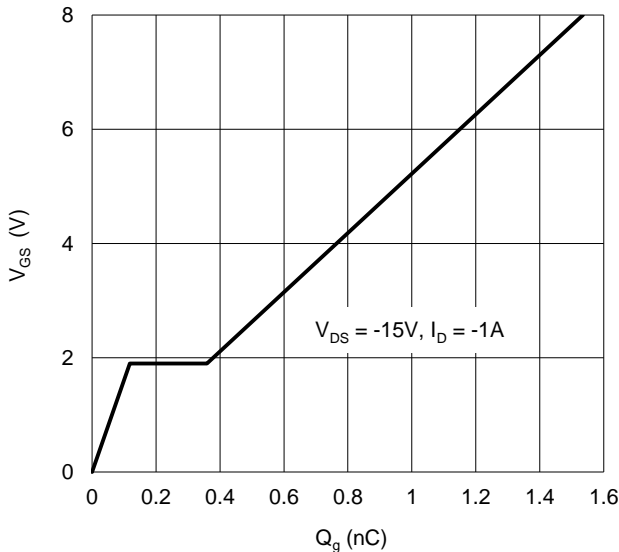


Figure 23. Gate Charge

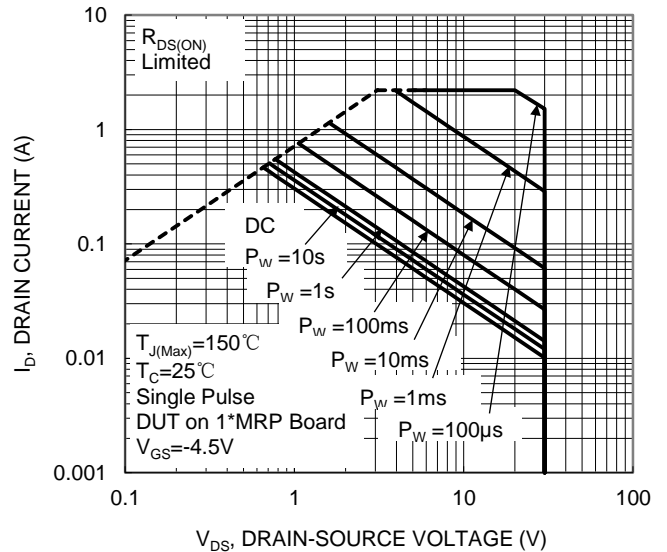


Figure 24. SOA, Safe Operation Area

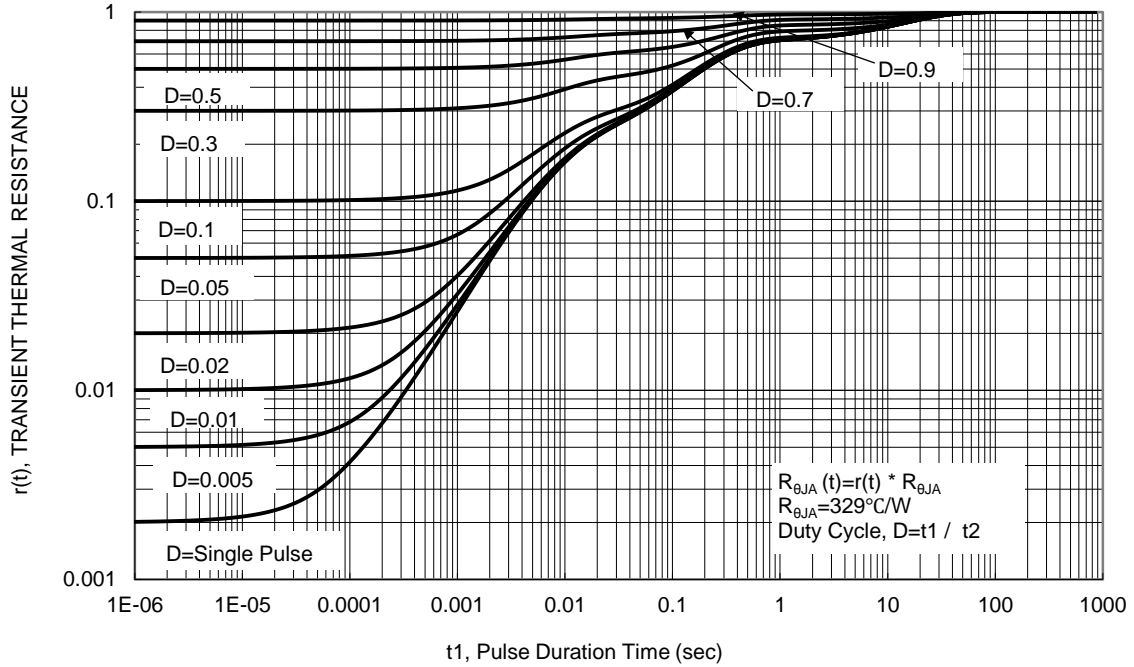
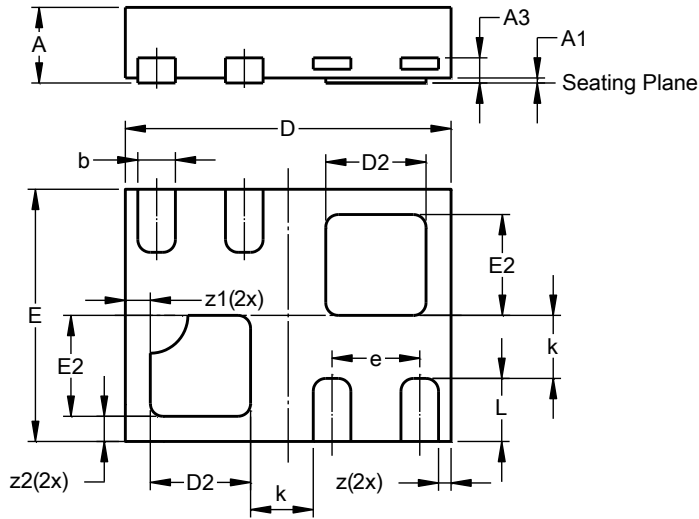


Figure 25. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1310-6 (Type B)

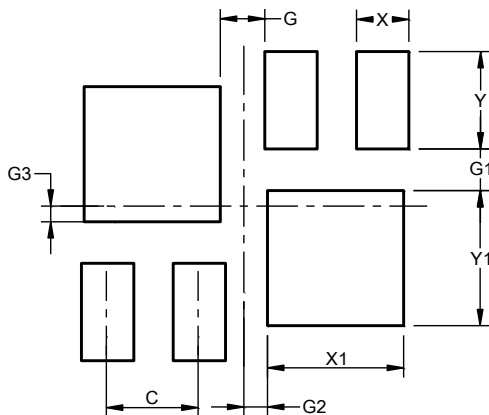


X2-DFN1310-6 (Type B)			
Dim	Min	Max	Typ
A	0.25	0.35	0.30
A1	0	0.05	0.02
A3	-	-	0.100
b	0.10	0.20	0.15
D	1.25	1.35	1.30
D2	0.30	0.50	0.40
E	0.95	1.05	1.00
E2	0.30	0.50	0.40
e	-	-	0.35
k	0.15	-	-
L	0.20	0.30	0.25
z	-	-	0.05
z1	-	-	0.10
z2	-	-	0.10
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1310-6 (Type B)



Dimensions	Value (in mm)
C	0.350
G	0.17
G1	0.16
G2	0.09
G3	0.06
X	0.20
X1	0.52
Y	0.375
Y1	0.52

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