



30V SYNCHRONOUS N-CHANNEL ENHANCEMENT MODE MOSFET PowerDI3333-8

Product Summary

Device	BV _{DSS}	R _{DS(ON)} Max
Q1	30V	$12m\Omega$ @ $V_{GS} = 5V$, $I_{D} = 15A$
Q2	30V	$6m\Omega @ V_{GS} = 5V, I_D = 15A$

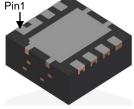
Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- DC-DC Converters
- Power Management Functions

PowerDI3333-8 (Type D)





Top View

Bottom View

Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Mechanical Data

- Case: PowerDI[®]3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin Annealed over Copper Leadframe.
 Solderable per MIL-STD-202, Method 208 ⁽³⁾
- Weight: 0.044 grams (Approximate)



Top View Pin Configuration

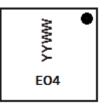
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN3012LEG-7	PowerDI3333-8 (Type D)	1000 / Tape & Reel
DMN3012LEG-13	PowerDI3333-8 (Type D)	3000 / Tape & Reel

Notes:

- 1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- See http://www.diodes.com/quality/lead_free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



E04 = Product Type Marking Code YYWW = Date Code Marking YY = Last Two Digits of Year (ex: 19 = 2019) WW = Week Code (01 to 53)



Maximum Ratings (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Q1	Q2	Unit	
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±10		V
	T _C = +25°C	1-	20		A
Continuous Drain Current @ V _{GS} = 5V	T _C = +70°C	I _D	16		
	T _A = +25°C	l _D	10		^
	T _A = +70°C		8		Α
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I _{DM}	70	100	А
Continuous Source-Drain Diode Current (Note 5)		Is	2.7	3.2	А
Avalanche Current (Note 6) L = 0.1mH		I _{AS}	34	50	А
Avalanche Energy (Note 6) L = 0.1mH		E _{AS}	58	125	mJ
ESD Capability(Note 9)		HBM	300		V
		CDM	1000		V

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Total Power Dissipation	$T_C = +25^{\circ}C$	ק	2.2	W	
Total Fower Dissipation	$T_C = +70^{\circ}C$	P_D	1.4		
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	ם	58		
Thermal Resistance, Junction to Ambient (Note 3)	t<10s	$R_{\theta JA}$	36	°C/W	
Thermal Resistance, Junction to Case (Note 5)	$R_{\theta JC}$	9.5			
Operating and Storage Temperature Range		$T_{J_i}T_{STG}$	-55 to +150	°C	

Electrical Characteristics Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current	I _{DSS}	_	_	1	μA	V _{DS} = 20V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 10V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						•
Gate Threshold Voltage	$V_{GS(TH)}$	1	_	2.1	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
Static Drain-Source On-Resistance	R _{DS(ON)}	_	10.5	12	mΩ	$V_{GS} = 5V, I_D = 15A$
Diode Forward Voltage	V _{SD}	_	_	1.0	V	V _{GS} = 0V, I _S = 15A
DYNAMIC CHARACTERISTICS (Note 8)						•
Input Capacitance	C _{iss}		650	850	pF	$V_{DS} = 15V, V_{GS} = 0V,$ f = 1.0MHz
Output Capacitance	Coss	_	314	410		
Reverse Transfer Capacitance	C_{rss}	_	12	16		
Gate Resistance	Rg	_	1.63	3.3	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	4.7	6.1		V _{DS} = 15V, I _D = 15A
Total Gate Charge at V _{TH}	Q _{g(TH)}	_	0.91	_	nC	
Gate-Source Charge	Qgs	_	1.6	_	IIC	
Gate-Drain Charge	Q_{gd}	_	0.9	_		
Turn-On Delay Time	t _{D(ON)}	_	5.1	7.7		$V_{DD} = 15V, V_{GS} = 4.5V,$ $I_{D} = 15A, R_{g} = 2\Omega$
Turn-On Rise Time	t _R	_	2.7	_		
Turn-Off Delay Time	t _{D(OFF)}	_	6.4	9.6	ns	
Turn-Off Fall Time	t _F	_	2.3	_		
Reverse Recovery Time	t _{RR}	_	24.5	_	ns	1 454 41/44 2004/
Reverse Recovery Charge	Q_{RR}	_	8.3	_	nC	$I_F = 15A$, di/dt = 300A/ μ s

5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
 Short duration pulse test used to minimize self-heating effect.
 Guaranteed by design. Not subject to product testing.
 Based on characterization data only. Not subject to production testing.

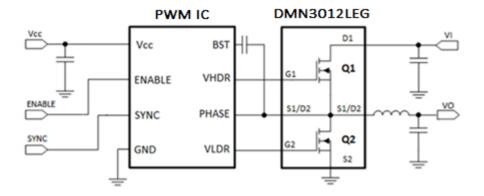


Electrical Characteristics Q2 (@T_A = +25°C, unless otherwise specified.)

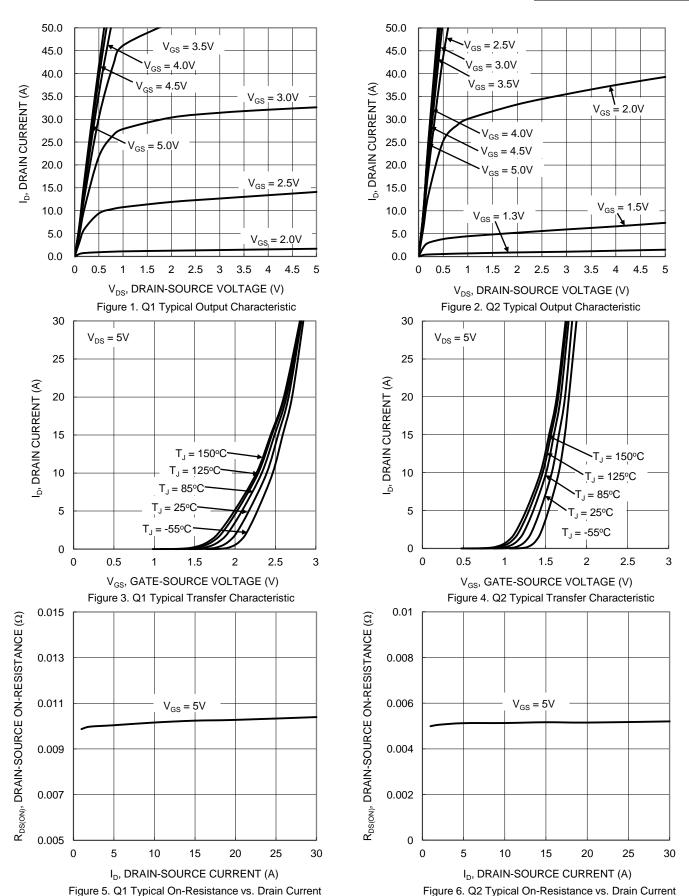
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	30	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	_	_	1.0	μA	$V_{DS} = 20V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 10V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	$V_{GS(TH)}$	0.75	_	1.15	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
Static Drain-Source On-Resistance	R _{DS(ON)}	_	5.2	6	mΩ	$V_{GS} = 5V, I_D = 15A$	
Diode Forward Voltage	V _{SD}	_	_	1.0	V	$V_{GS} = 0V, I_{S} = 15A$	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}	_	1137	1480	pF		
Output Capacitance	Coss	_	620	810	pF	$V_{DS} = 15V, V_{GS} = 0V,$ f = 1.0MHz	
Reverse Transfer Capacitance	C _{rss}	_	24	32	pF	71 = 1.0IVIDZ	
Gate Resistance	Rg	_	0.54	1.1	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (V _{GS} = 4.5V)	Q_{g}	_	9.7	12.6	nC		
Total Gate Charge at V _{TH}	Q _{g(TH)}	_	0.96	_	nC	\/ 4E\/ - 4E\	
Gate-Source Charge	Q _{gs}	_	1.7	_	nC	$V_{DS} = 15V, I_{D} = 15A$	
Gate-Drain Charge	Q_{gd}	_	1.2	_	nC	1	
Turn-On Delay Time	t _{D(ON)}	_	4.4	6.6	ns		
Turn-On Rise Time	t _R	_	3.5	_	ns	$V_{DD} = 15V, V_{GS} = 4.5V,$	
Turn-Off Delay Time	t _{D(OFF)}	_	12.4	18.6	ns	$I_D = 15A$, $R_g = 2\Omega$	
Turn-Off Fall Time	t _F	_	2.9	_	ns		
Reverse Recovery Time	t _{RR}		30.5		ns	I_ 15 \ di/dt 2000 /:-	
Reverse Recovery Charge	Q _{RR}	_	10.8	_	nC	$I_F = 15A$, di/dt = 300A/ μ s	

7. Short duration pulse test used to minimize self-heating effect. 8. Guaranteed by design. Not subject to product testing. Notes:

Typical Circuit







and Gate Voltage

and Gate Voltage



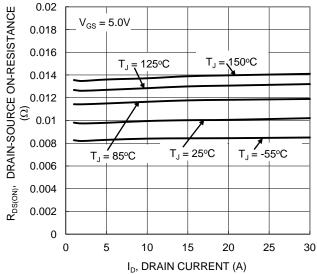


Figure 7. Q1 Typical On-Resistance vs. Drain Current and Temperature

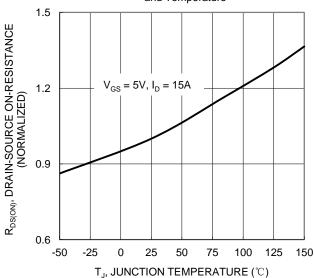
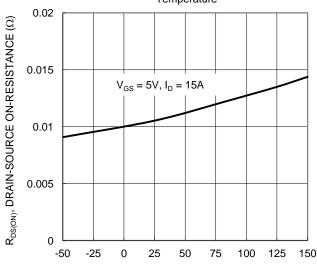


Figure 9. Q1 On-Resistance Variation with Temperature



T_J, JUNCTION TEMPERATURE (℃) Figure 11. Q1 On-Resistance Variation with Temperature

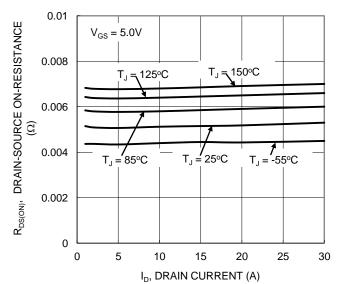


Figure 8. Q2 Typical On-Resistance vs. Drain Current and Temperature

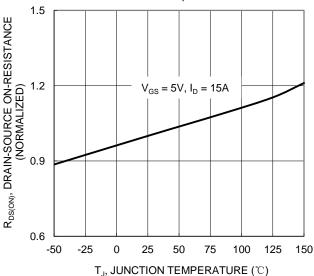
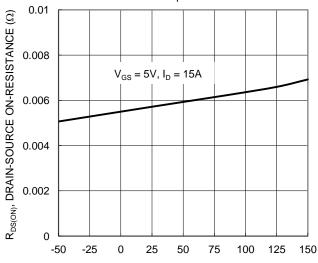


Figure 10. Q2 On-Resistance Variation with Temperature



 T_J , JUNCTION TEMPERATURE ($^{\circ}$ C) Figure 12. Q2 On-Resistance Variation with Temperature



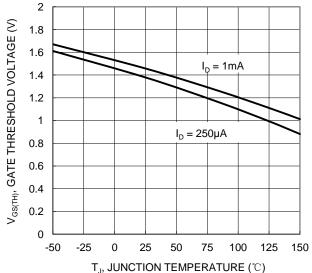
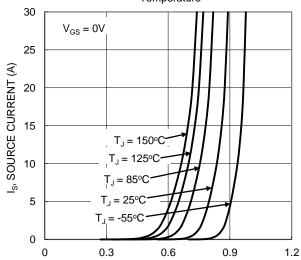


Figure 13. Q1 Gate Threshold Variation vs. Junciton Temperature



 $\rm V_{SD},$ SOURCE-DRAIN VOLTAGE (V) Figure 15. Q1 Diode Forward Voltage vs. Current

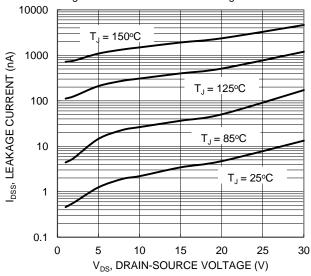


Figure 17. Q1 Typical Drain-Source Leakage Current vs. Voltage

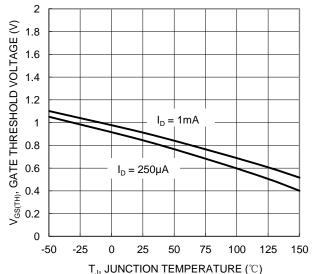
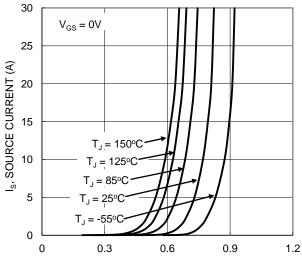
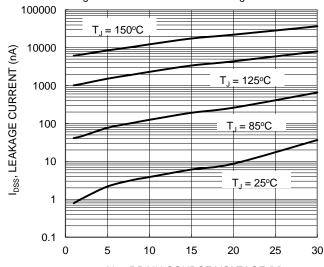


Figure 14. Q2 Gate Threshold Variation vs. Junciton Temperature

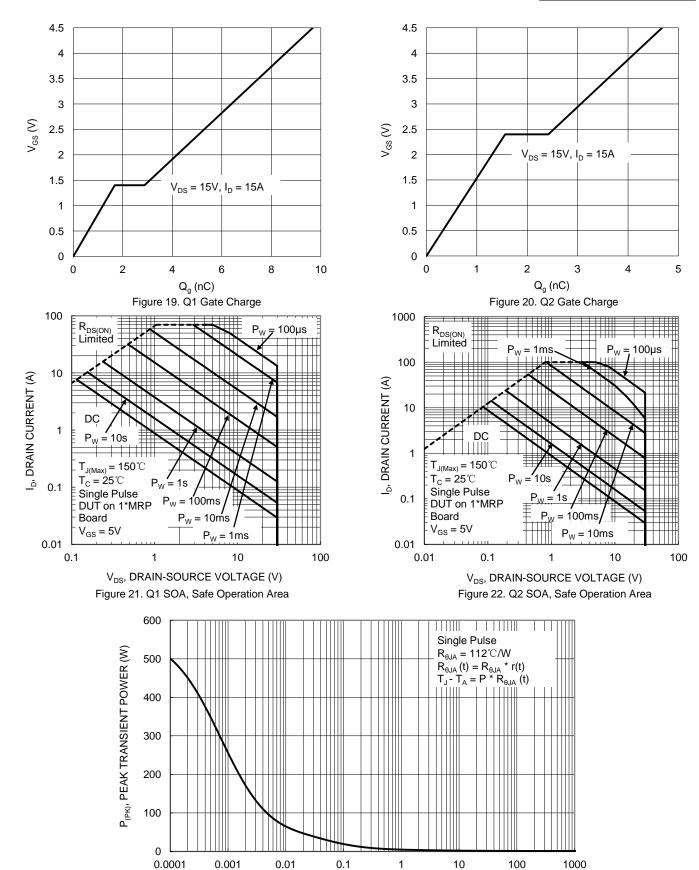


V_{SD}, SOURCE-DRAIN VOLTAGE (V) Figure 16. Q2 Diode Forward Voltage vs. Current



V_{DS}, DRAIN-SOURCE VOLTAGE (V) Figure 18. Q2 Typical Drain-Source Leakage Current vs. Voltage





t1, PULSE DURATION TIME (sec)
Figure 23. Single Pulse Maximum Power Dissipation



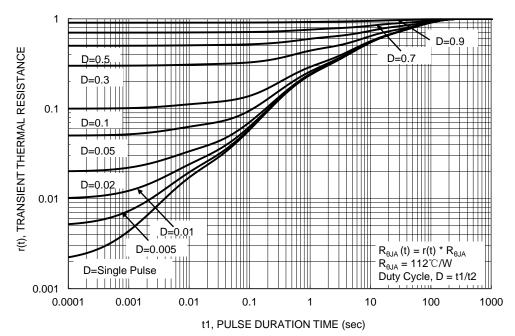


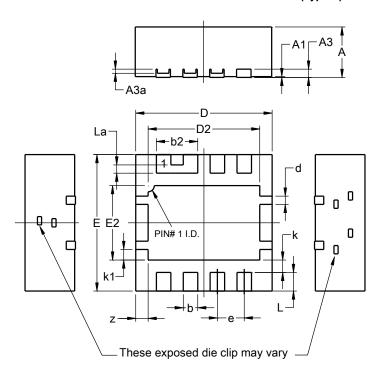
Figure 24. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8 (Type D)

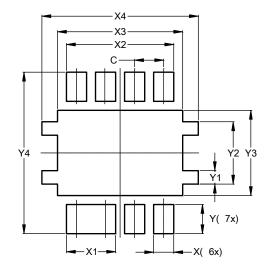


PowerDI3333-8 (Type D)					
Dim	Min	` ' ' '			
Α	1.17	1.23	1.20		
A1	0.00	0.05	0.02		
A3	0.15	0.25	0.20		
A3a	0.05	0.15	0.10		
b	0.30	0.40	0.35		
b2	0.95	1.05	1.00		
D	3.20	3.40	3.30		
D2	2.65	2.75	2.70		
Е	3.20	3.40	3.30		
E2	1.75	1.85	1.80		
d	0.15	0.25	0.20		
е			0.65		
k			0.30		
k1	0.21	0.31	0.26		
L	0.40	0.50	0.45		
La	0.15	0.25	0.20		
Z	0.25	0.35	0.30		
All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8 (Type D)



Dimensions	Value		
פווטופווסוטווס	(in mm)		
С	0.650		
Х	0.450		
X1	1.100		
X2	2.400		
Х3	2.800		
X4	3.500		
Y	0.650		
Y1	0.300		
Y2	1.390		
Y3	1.900		
Y4	3.600		



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