

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max $T_A = +25^\circ\text{C}$
30V	21m Ω @ $V_{GS} = 10\text{V}$	7.3A
	35m Ω @ $V_{GS} = 4.5\text{V}$	5.5A

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- **ESD Protected Gate**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

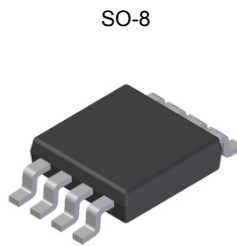
- Backlighting
- Power Management Functions
- DC-DC Converters

Mechanical Data

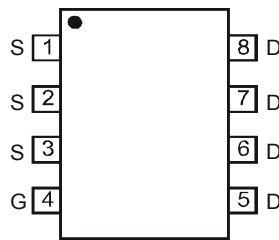
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.008 grams (approximate)



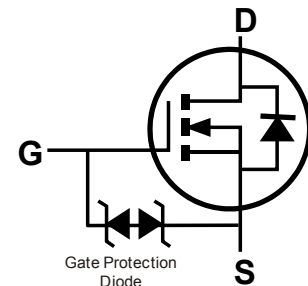
ESD PROTECTED



Top View



Top View
Pin Configuration



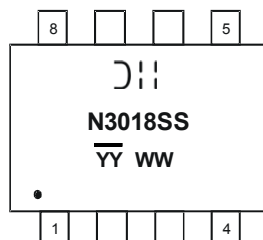
Equivalent Circuit

Ordering Information (Note 4)

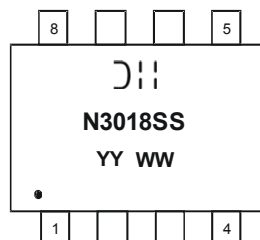
Part Number	Case	Packaging
DMN3018SSS-13	SO-8	2500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

⌋⌋ = Manufacturer's Marking
 N3018SS = Product Type Marking Code
 YYWW = Date Code Marking
 YY or \overline{YY} = Year (ex: 13 = 2013)
 WW = Week (01 - 53)
 YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)
 \overline{YY} = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	± 25	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	7.3 5.7	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	9.7 7.8	A
Continuous Drain Current (Note 6) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	5.5 4.3	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	7.6 5.8	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	60	A
Maximum Body Diode continuous Current			I_S	2.5	A

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	1.4	W
	$T_A = +70^\circ\text{C}$		0.9	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	90	$^\circ\text{C/W}$
	$t < 10\text{s}$		50	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	1.7	W
	$T_A = +70^\circ\text{C}$		1.1	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	75	$^\circ\text{C/W}$
	$t < 10\text{s}$		42	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	7.6	$^\circ\text{C/W}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	-	-	± 10	μA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	1	1.7	2.1	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	-	15	21	m Ω	$V_{GS} = 10\text{V}, I_D = 10\text{A}$
		-	20	35		$V_{GS} = 4.5\text{V}, I_D = 8.5\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	-	8.3	-	S	$V_{DS} = 5\text{V}, I_D = 6.9\text{A}$
Diode Forward Voltage	V_{SD}	0.5	-	1.2	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	697	-	pF	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	97	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	67	-	pF	
Gate resistance	R_g	-	1.47	-	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	-	6.0	-	nC	$V_{GS} = 10\text{V}, V_{DS} = 15\text{V},$ $I_D = 9\text{A}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	-	13.2	-	nC	
Gate-Source Charge	Q_{gs}	-	2.2	-	nC	
Gate-Drain Charge	Q_{gd}	-	1.8	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	4.3	-	ns	
Turn-On Rise Time	t_r	-	4.4	-	ns	$V_{DD} = 15\text{V}, V_{GS} = 10\text{V},$ $R_L = 15\Omega, I_D = 1\text{A}, R_G = 6\Omega$
Turn-Off Delay Time	$t_{D(off)}$	-	20.1	-	ns	
Turn-Off Fall Time	t_f	-	4.1	-	ns	
Reverse Recovery Time	T_{rr}	-	7.3	-	ns	$I_F = 9\text{A}, di/dt = 500\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}	-	7.9	-	nC	

- Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

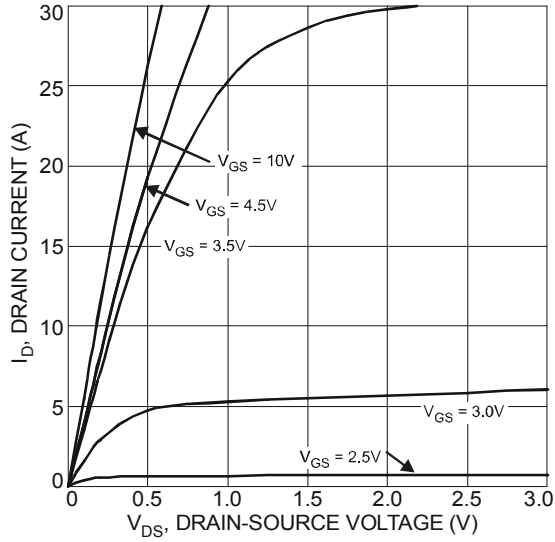


Fig. 1 Typical Output Characteristic

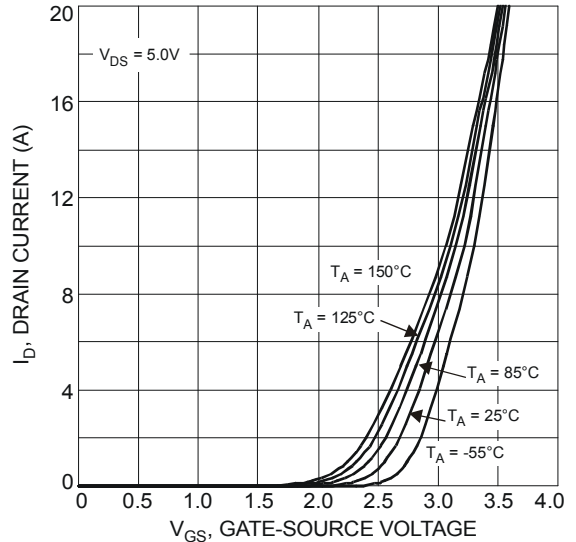


Fig. 2 Typical Transfer Characteristics

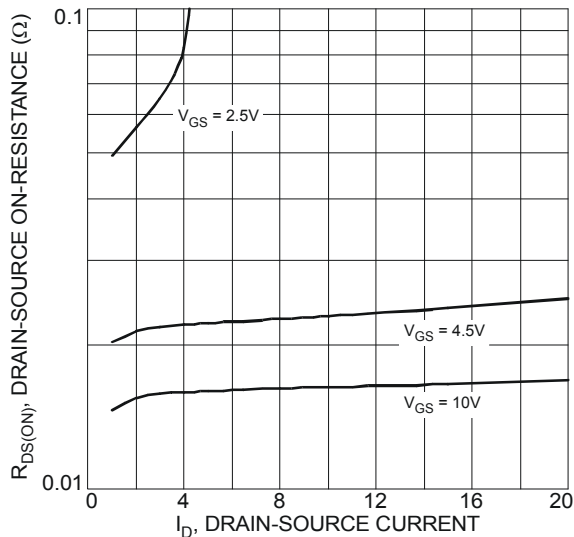


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

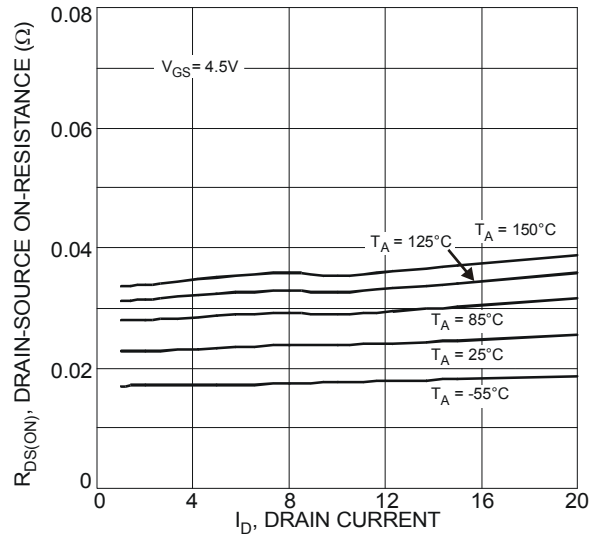


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

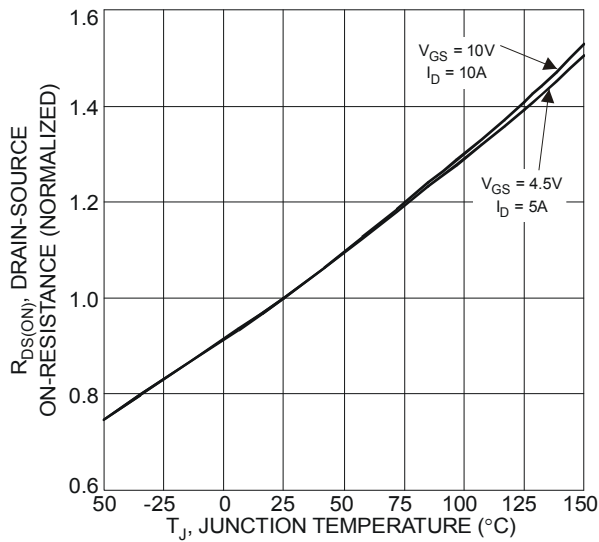


Fig. 5 On-Resistance Variation with Temperature

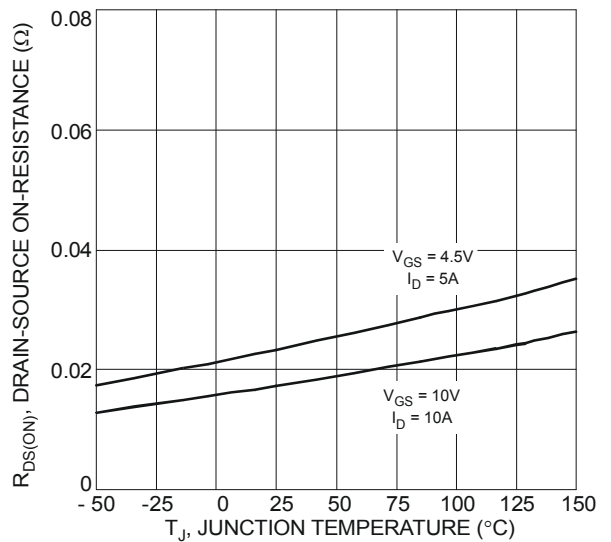


Fig. 6 On-Resistance Variation with Temperature

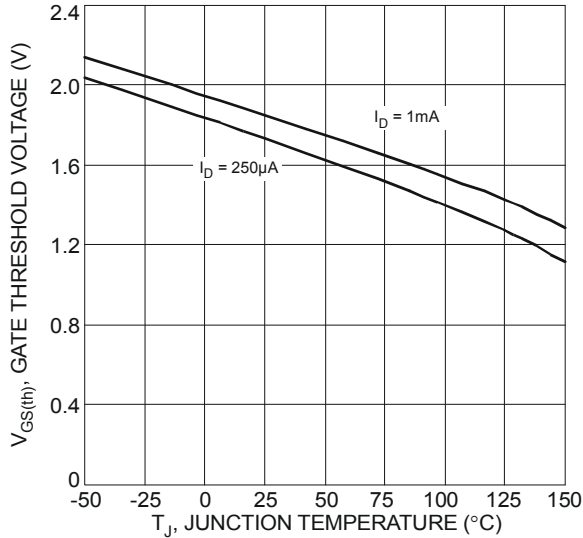


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

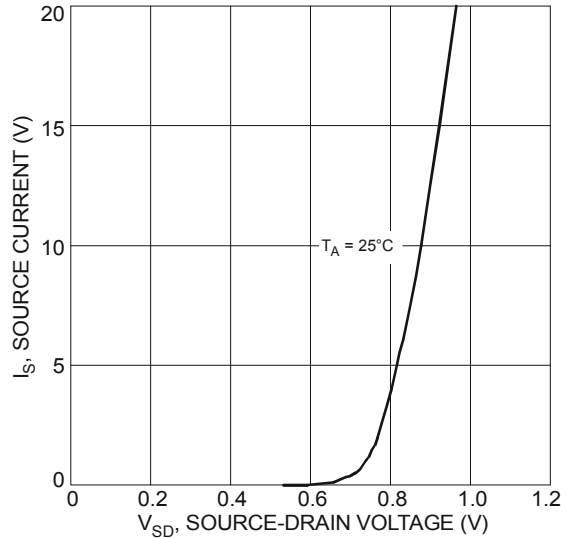


Fig.8 Diode Forward Voltage vs. Current

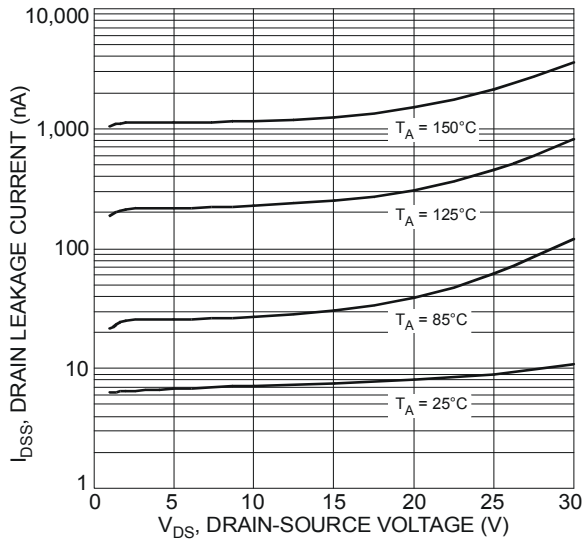


Fig. 9 Typical Drain-Source Leakage Current vs. Voltage

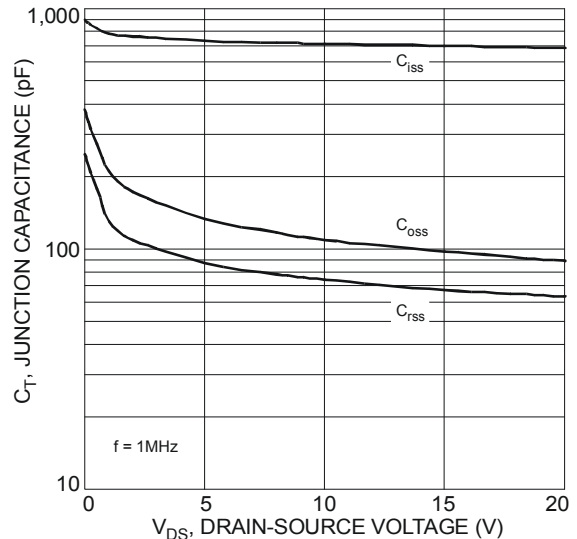


Fig. 10 Typical Junction Capacitance

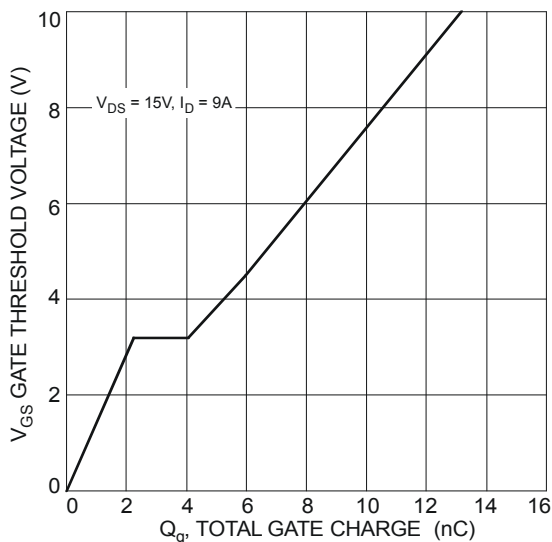
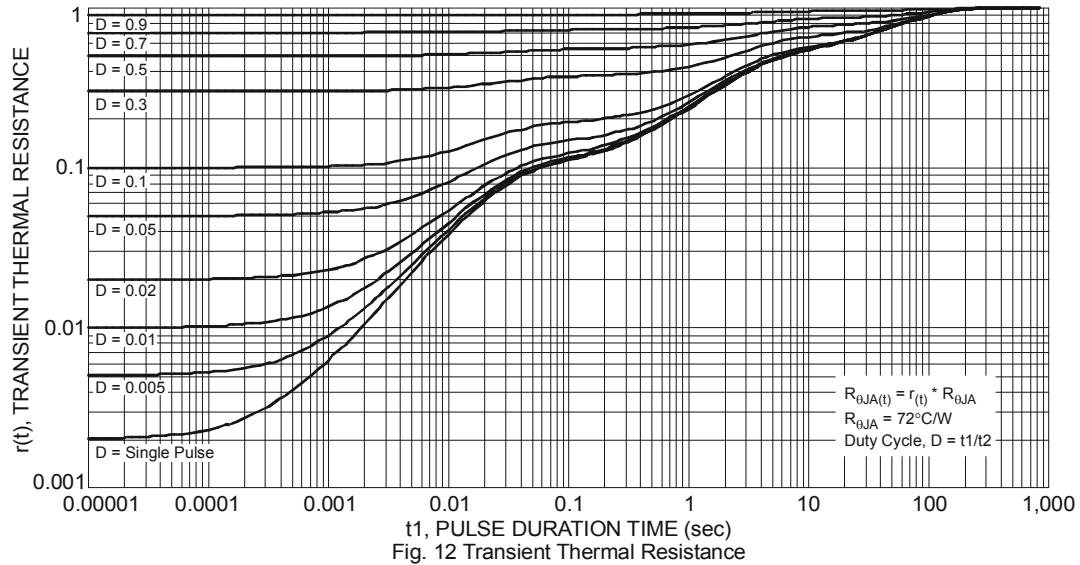
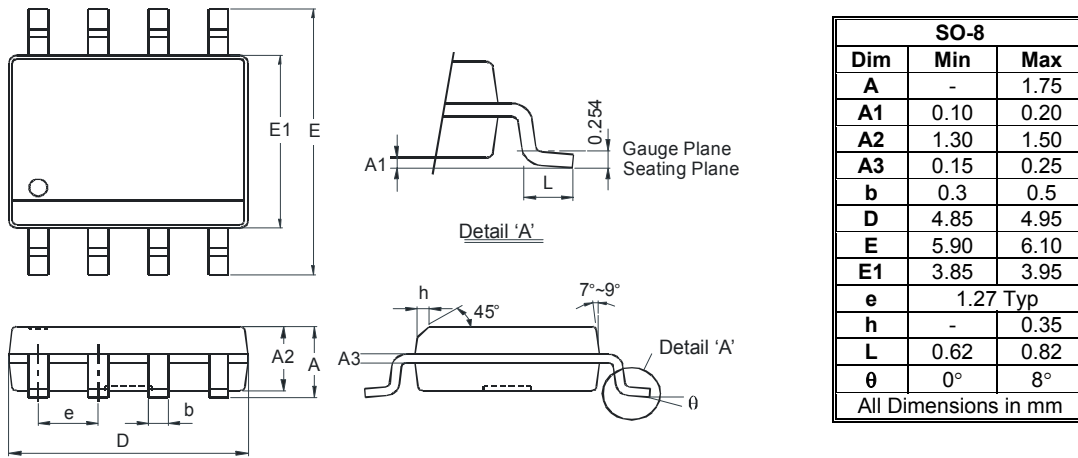


Fig. 11 Gate Charge



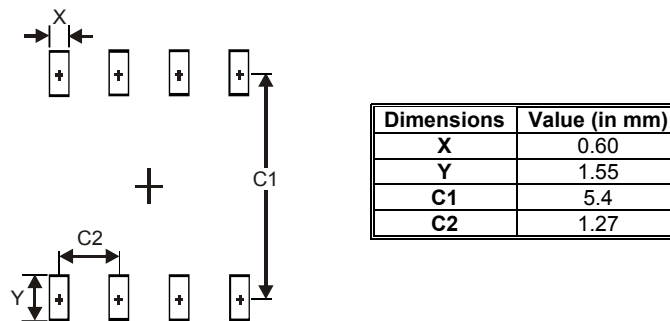
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version



Suggested Pad Layout

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