Product Summary

V_{DSS}	$R_{DS(ON)}$	Q_g	Q_{gd}	I_D
12V	18mΩ	3.2nC	0.3nC	4.8A

Typ. @ V_{GS} = 4.5V, T_A = +25°C

Description

This 2nd generation Lateral MOSFET (LD-MOS) is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high efficiency power transfer. It uses Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal $R_{DS(ON)}$ per footprint area.

Applications

- DC-DC converters
- Battery managements
- Load switches

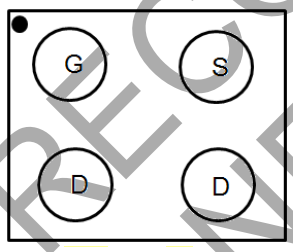
Features

- LD-MOS Technology with the Lowest Figure of Merit:
  $R_{DS(ON)}$ = 18mΩ to Minimize On-State Losses
  Q_g = 3.2nC for Ultra-Fast Switching
- $V_{GS(th)}$ = 0.8V typ. for a Low Turn-On Potential
- CSP with Footprint 1.0mm × 1.0mm
- Height = 0.62mm for Low Profile
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at https://www.diodes.com/products/automotive/automotive-products/.**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability. https://www.diodes.com/quality/product-definitions/**

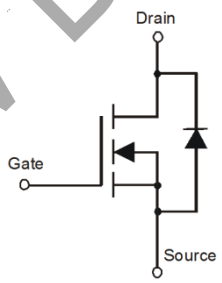
Mechanical Data

- Package: U-WLB1010-4
- Terminal Connections: See Diagram Below

U-WLB1010-4



Top View



Equivalent Circuit

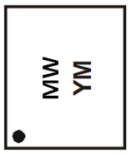
Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMN1032UCB4-7	U-WLB1010-4	3,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-WLB1010-4



MW = Product Type Marking Code
YM = Date Code Marking
Y or $\overline{Y}$ = Year (ex: J = 2022)
M or $\overline{M}$ = Month (ex: 2 = February)

Date Code Key

Year	2013	…	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	A	…	J	K	L	M	N	O	P	R	S	T

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	12	V
Gate-Source Voltage			V_{GSS}	±8	V
Continuous Drain Current (Note 5) V_{GS} = 4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	4.8 3.8	A
Continuous Drain Current (Note 5) V_{GS} = 2.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	4.5 3.6	A
Pulsed Drain Current (Note 6)			I_{DM}	15	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 7)	P_D	0.9	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 7)	$R_{\theta JA}$	138.81	°C/W
Thermal Resistance, Junction to Case @T_C = +25°C (Note 7)	$R_{\theta JC}$	31.77	°C/W
Power Dissipation (Note 5)	P_D	1.16	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 5)	$R_{\theta JA}$	107.59	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.
6. Repetitive rating, pulse width limited by junction temperature.
7. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	12	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1.0	μA	V_{DS} = 9.6V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	0.4	0.8	1.2	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	18	26	mΩ	V_{GS} = 4.5V, I_D =1A
		—	21	29		V_{GS} = 2.5V, I_D = 1A
		—	27	38		V_{GS} = 1.8V, I_D = 1A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	8.1	—	S	V_{DS} = 6V, I_D = 1A
Diode Forward Voltage	V_{SD}	—	0.7	1.0	V	V_{GS} = 0V, I_S = 1A
Reverse Recovery Charge	Q_{rr}	—	1.2	—	nC	V_{dd} = 5V, I_F = 1A, di/dt =100A/μs
Reverse Recovery Time	t_{rr}	—	10.5	—	ns	
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	325	450	pF	V_{DS} = 6V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	183	250		
Reverse Transfer Capacitance	C_{rss}	—	31	47		
Series Gate Resistance	R_G	—	3.1	—	Ω	f = 1MHz, V_{GS} = 0V, V_{DS} = 0V
Total Gate Charge	Q_g	—	3.2	4.5	nC	V_{GS} = 4.5V, V_{DS} = 6V, I_D =1A
Gate-Source Charge	Q_{gs}	—	0.4	—		
Gate-Drain Charge	Q_{gd}	—	0.3	—		
Gate Charge at Vth	$Q_{g(th)}$	—	0.2	—		
Turn-On Delay Time	$t_{D(on)}$	—	3.3	10	ns	V_{DS} = 6V, V_{GS} = 4.5V, R_G = 20Ω, I_D = 1A
Turn-On Rise Time	t_r	—	5.6	—		
Turn-Off Delay Time	$t_{D(off)}$	—	24	36		
Turn-Off Fall Time	t_f	—	9	—		

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

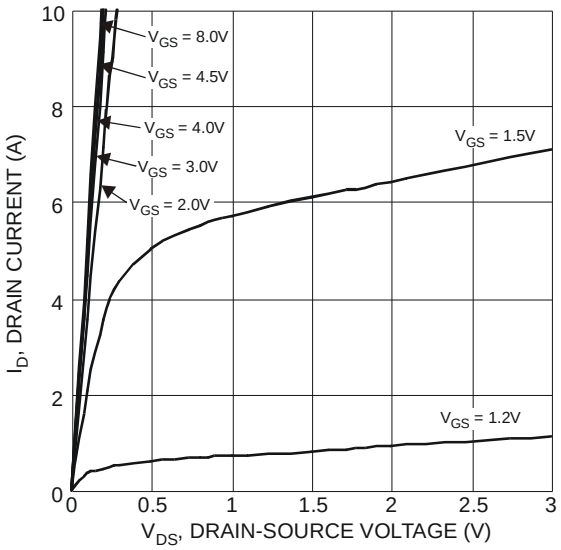


Figure 1 Typical Output Characteristics

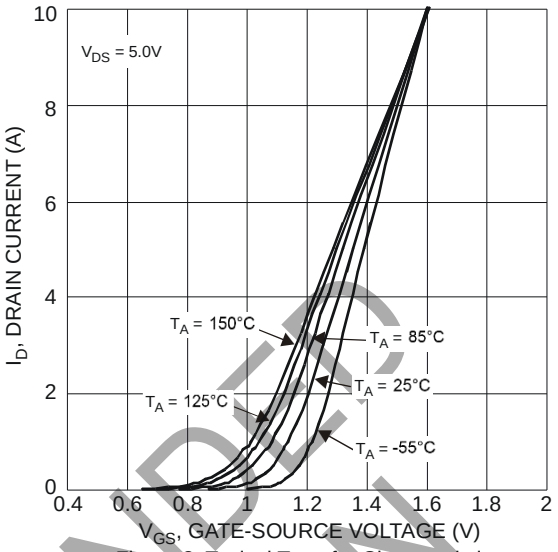


Figure 2 Typical Transfer Characteristics

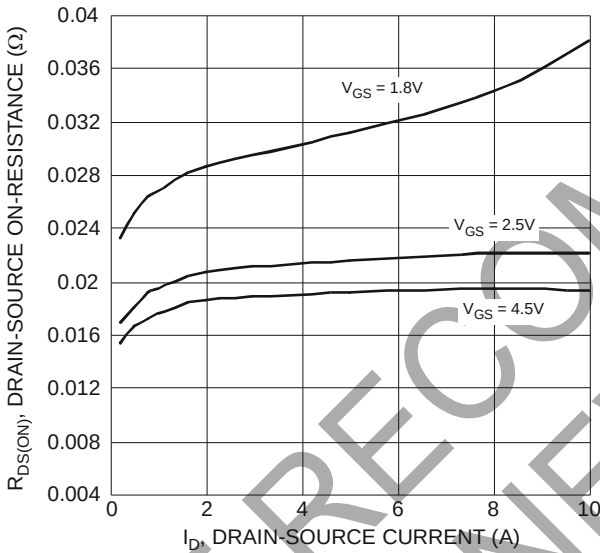


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

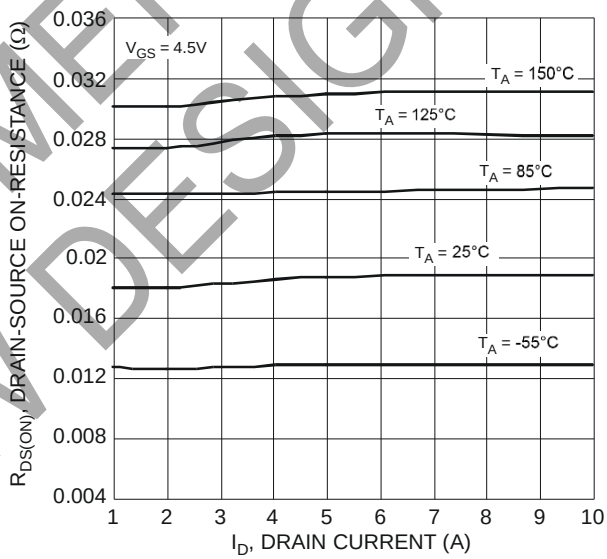


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

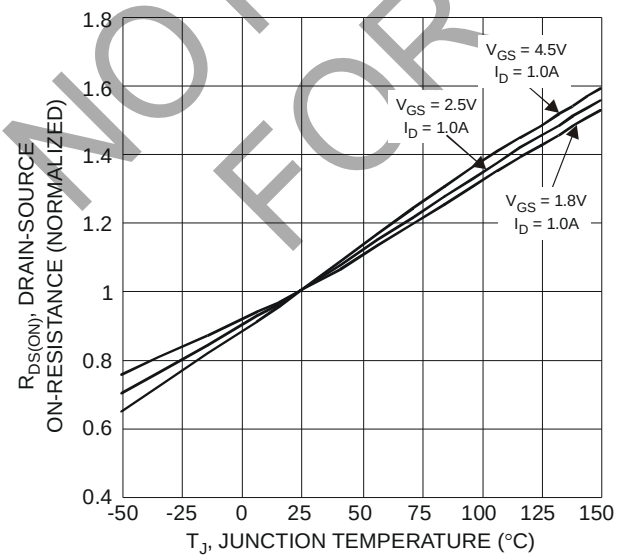


Figure 5 On-Resistance Variation with Temperature

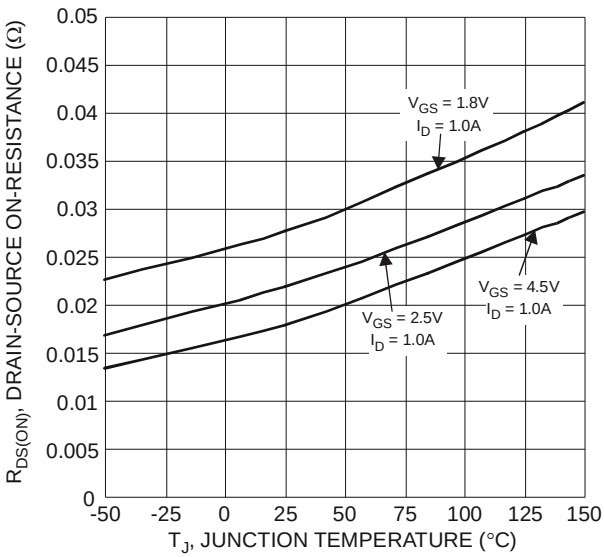


Figure 6 On-Resistance Variation with Temperature

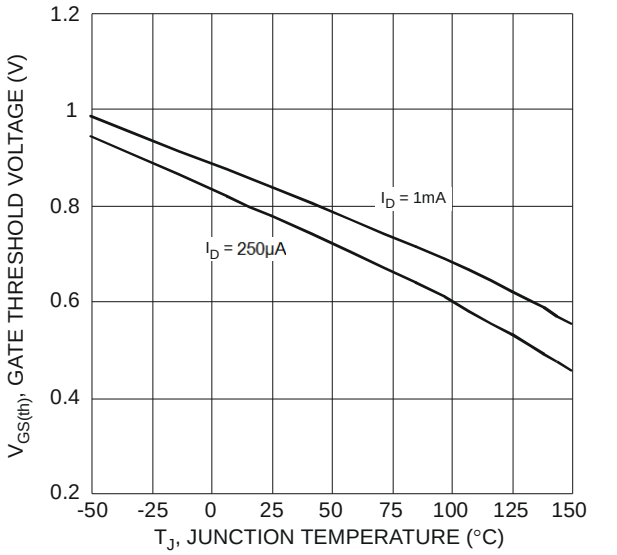


Figure 7 Gate Threshold Variation vs. Junction Temperature

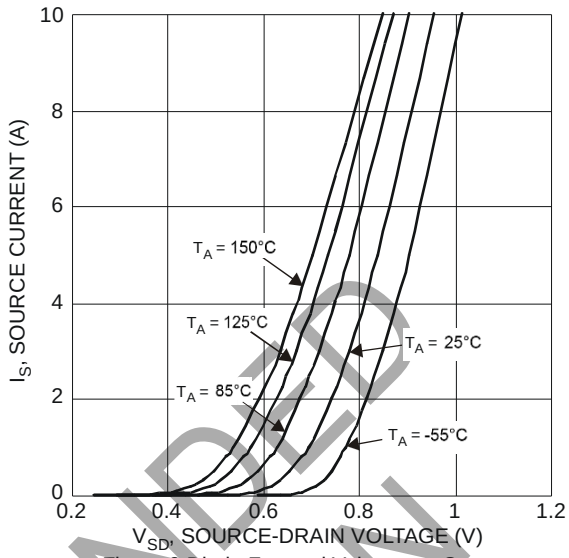


Figure 8 Diode Forward Voltage vs. Current

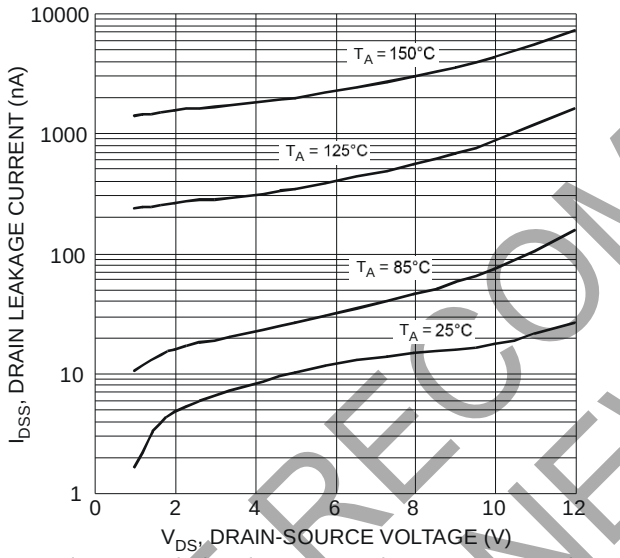


Figure 9 Typical Drain-Source Leakage Current vs. Voltage

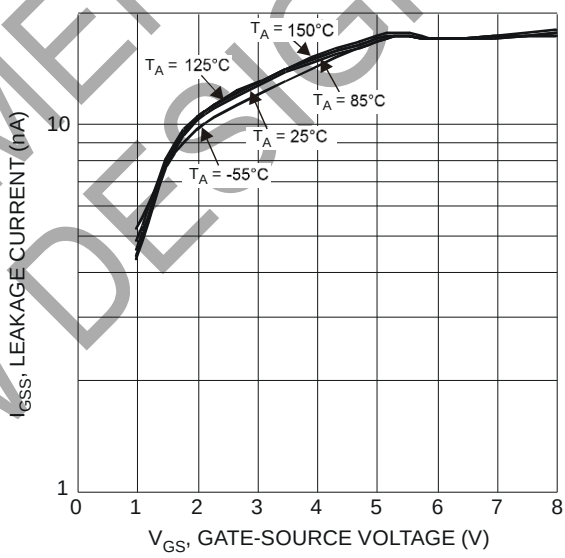


Figure 10 Gate-Source Leakage Current vs. Voltage

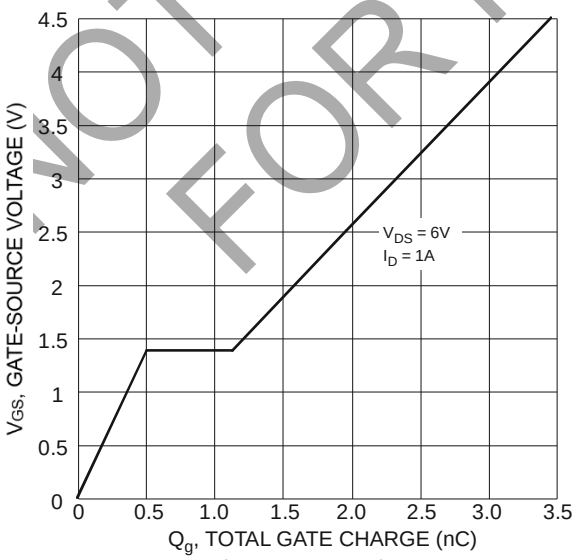


Figure 11 Gate Charge

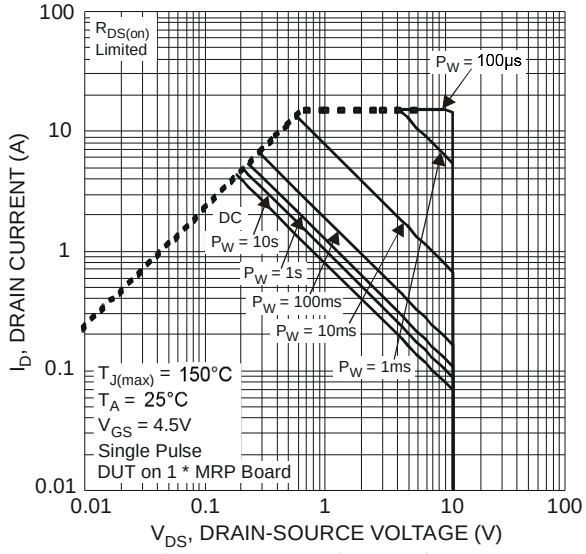


Figure 12 SOA, Safe Operation Area

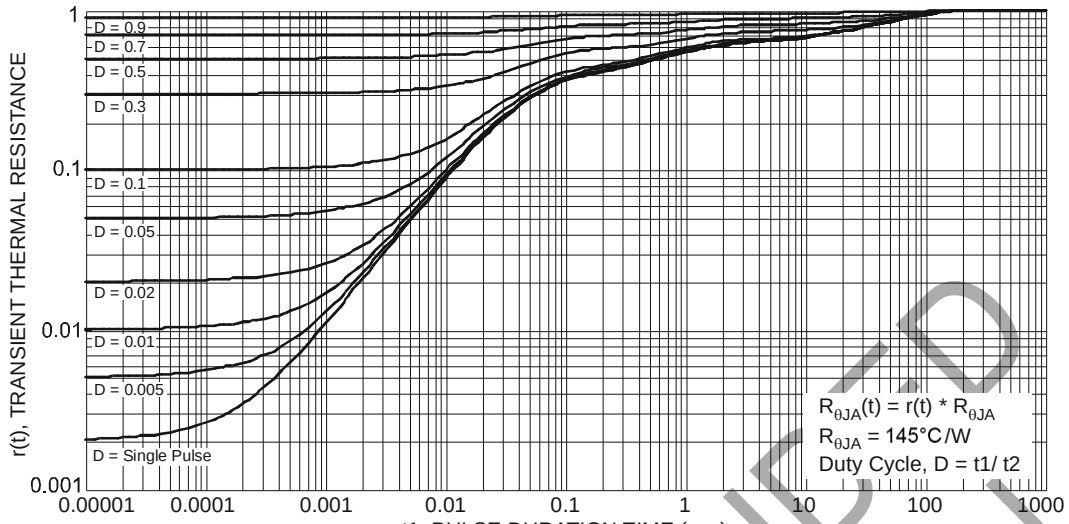
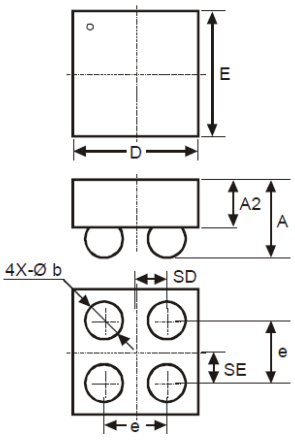


Figure 13 Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1010-4

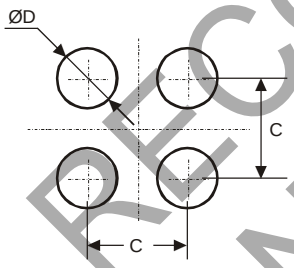


U-WLB1010-4			
Dim	**Min**	**Max**	**Typ**
D	0.95	1.05	1.00
E	0.95	1.05	1.00
A	–	0.62	–
A2	–	–	0.38
b	0.25	0.35	0.30
e	–	–	0.50
SD	–	–	0.25
SE	–	–	0.25
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1010-4



Dimensions	Value (in mm)
C	0.50
D	0.25

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