

Product Summary

$V_{(BR)DSS}$	$R_{DS(on) \max}$	I_D $T_A = 25^\circ\text{C}$
-50V	10 Ω @ $V_{GS} = -5\text{V}$	-130mA

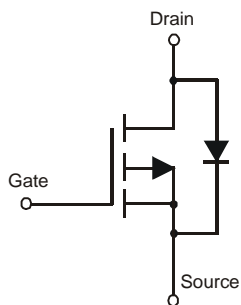
Description and Applications

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

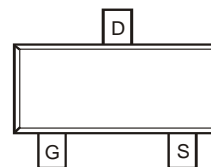
- General Purpose Interfacing Switch
- Power Management Functions
- Analog Switch



Top View



Equivalent Circuit



Top View

Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Lead, Halogen and Antimony Free, RoHS Compliant (Note 1)**
- **"Green" Device (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

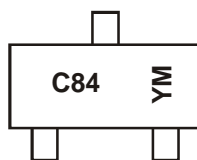
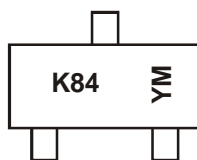
- Case: SOT23
- Case Material: UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish (Lead Free Plating) Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)

Ordering Information (Note 3)

Part Number	Qualification	Case	Packaging
BSS84-7-F	Commercial	SOT23	3000/Tape & Reel
BSS84Q-7-F	Automotive	SOT23	3000/Tape & Reel
BSS84-13-F	Commercial	SOT23	10000/Tape & Reel
BSS84Q-13-F	Automotive	SOT23	10000/Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. No purposely added lead. Halogen and Antimony free.
 2. Product manufactured with Date Code V9 (week 33, 2008) and newer are built with Green Molding Compound. Product manufactured prior to Date Code V9 are built with Non-Green Molding Compound and may contain Halogens or Sb_2O_3 Fire Retardants
 3. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



K = SAT (Shanghai Assembly / Test site)
 C = CAT (Chengdu Assembly / Test site)
 84 = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: N = 2002)
 M = Month (ex: 9 = September)

Date Code Key

Year	1998	1999	2000	2001	2002	2003	2004	...	2011	2012	2013	2014	2015	2016	2017
Code	J	K	L	M	N	P	R	...	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V _{DSS}	-50	V
Drain-Gate Voltage R _{GS} ≤ 20KΩ	V _{DGR}	-50	V
Gate-Source Voltage Continuous	V _{GSS}	±20	V
Drain Current (Note 4) Continuous	I _D	-130	mA
Pulsed Drain Current	I _{DM}	-1.2	A

Thermal Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 4)	P _D	300	mW
Thermal Resistance, Junction to Ambient	R _{θJA}	417	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 5)						
Drain-Source Breakdown Voltage	BV _{DSS}	-50	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-15	μA	V _{DS} = -50V, V _{GS} = 0V, T _J = 25°C
		—	—	-60	μA	V _{DS} = -50V, V _{GS} = 0V, T _J = 125°C
		—	—	-100	nA	V _{DS} = -25V, V _{GS} = 0V, T _J = 25°C
Gate-Body Leakage	I _{GSS}	—	—	±10	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage	V _{GS(th)}	-0.8	—	-2.0	V	V _{DS} = V _{GS} , I _D = -1mA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	—	10	Ω	V _{GS} = -5V, I _D = -0.100A
Forward Transconductance	g _{FS}	0.05	—	—	S	V _{DS} = -25V, I _D = -0.1A
DYNAMIC CHARACTERISTICS (Note 6)						
Input Capacitance	C _{iss}	—	—	45	pF	V _{DS} = -25V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	—	25	pF	
Reverse Transfer Capacitance	C _{rss}	—	—	12	pF	
SWITCHING CHARACTERISTICS (Note 6)						
Turn-On Delay Time	t _{D(ON)}	—	10	—	ns	V _{DD} = -30V, I _D = -0.27A,
Turn-Off Delay Time	t _{D(OFF)}	—	18	—	ns	R _{GEN} = 50Ω, V _{GS} = -10V

- Notes:
- Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com>.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing

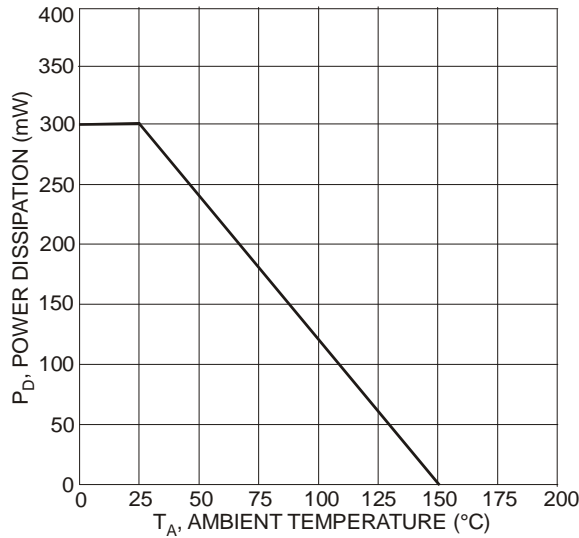


Fig. 1 Max Power Dissipation vs. Ambient Temperature

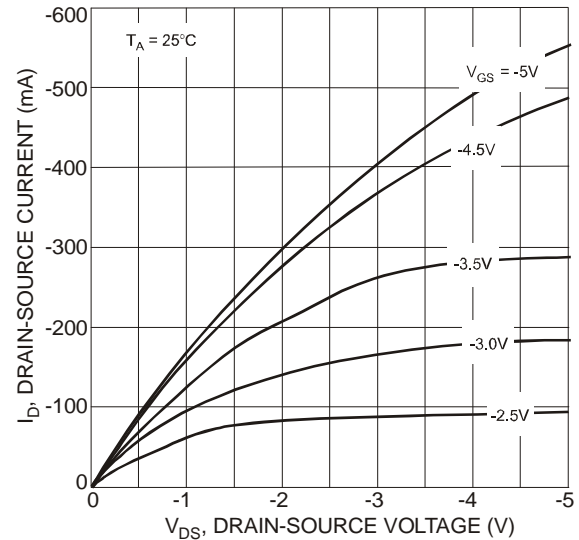


Fig. 2 Drain-Source Current vs. Drain-Source Voltage

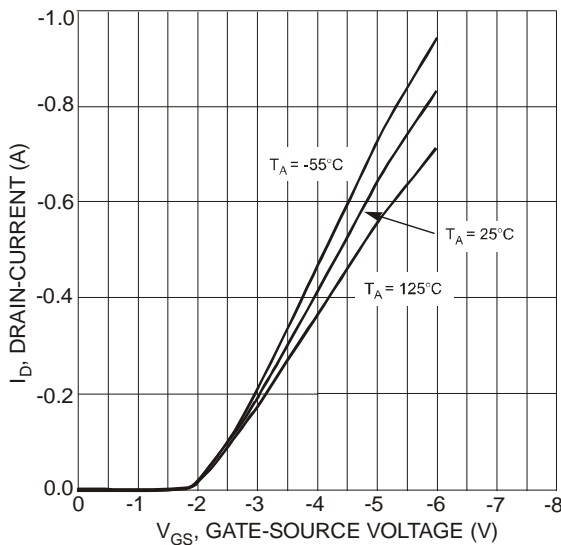


Fig. 3 Drain-Current vs. Gate-Source Voltage

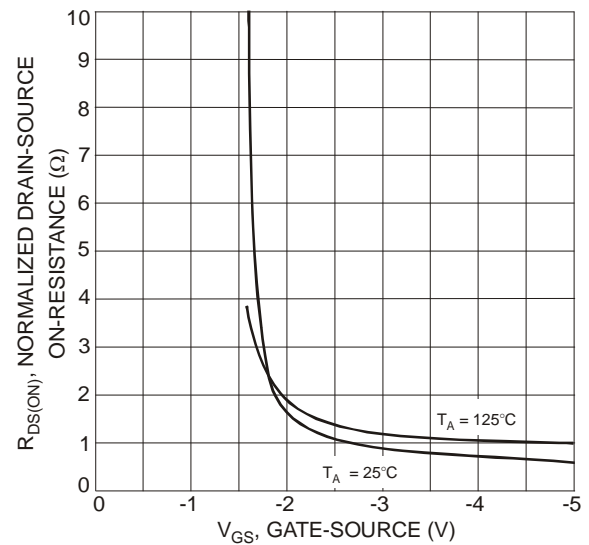


Fig. 4 On-Resistance vs. Gate-Source Voltage

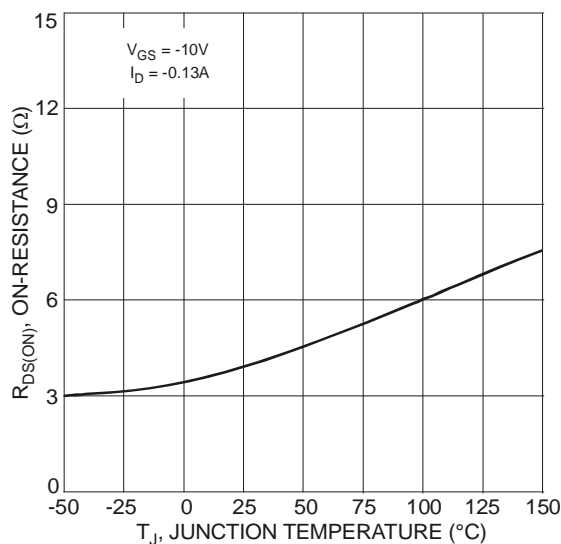


Fig. 5 On-Resistance vs. Junction Temperature

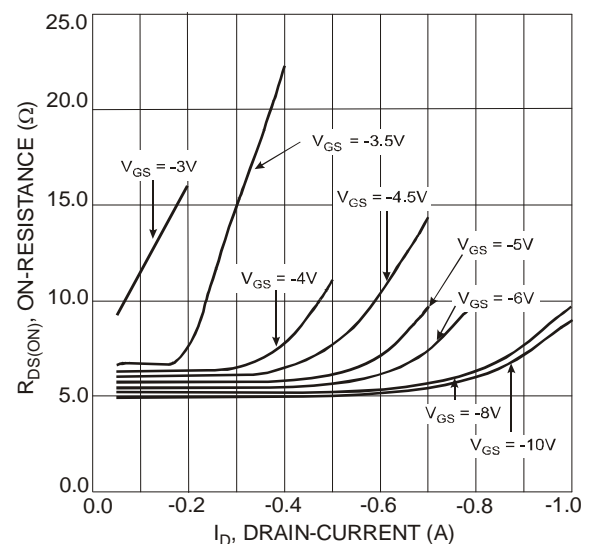
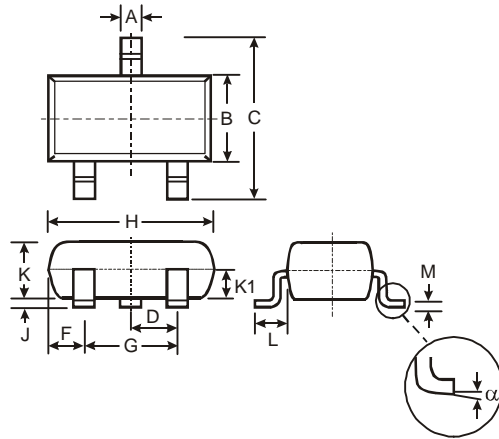


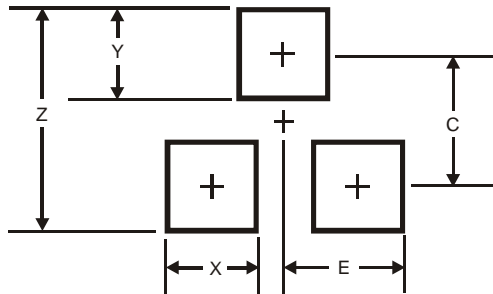
Fig. 6 On-Resistance vs. Drain-Current

Package Outline Dimensions



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.903	1.10	1.00
K1	-	-	0.400
L	0.45	0.61	0.55
M	0.085	0.18	0.11
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35

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