



P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _C = +25°C		
-12V	11.7m Ω @ V _{GS} = -4.5V	-19A		
-120	18.6m Ω @ V _{GS} = -2.5V	-15A		

Description

This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Backlighting
- Power Management Functions
- DC-DC Converters

Features and Benefits

- Low R_{DS(ON)} Ensures On-State Losses are Minimized
- Small Form Factor Thermally Efficient Package Enables Higher Density End Products (PowerDI[®])
- Occupies just 33% of the Board Area Occupied by SO-8 Enabling Smaller End Product
- ESD Protected Up To 3kV
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

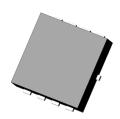
Mechanical Data

- Case: PowerDI3333-8 (Type UX)
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
 Terminals: Finish Matte Tin Annealed over Copper Leadframe.

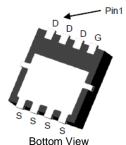
 Solderable per MIL-STD-202, Method 208 (§3)
- Weight: 0.072grams (Approximate)

PowerDI3333-8 (Type UX)

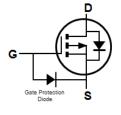








Pin Configuration



Equivalent Circuit

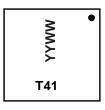
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP1011LFV-7	PowerDI3333-8 (Type UX)	2,000/Tape & Reel
DMP1011LFV-13	PowerDI3333-8 (Type UX)	3,000/Tape & Reel

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.

- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



T41 = Product Marking Code YYWW = Date Code Marking YY = Last Two Digits of Year (ex: 17 for 2017) WW = Week Code (01 to 53)

PowerDI is a registered trademark of Diodes Incorporated.



Maximum Ratings (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage			V _{DSS}	-12	V
Gate-Source Voltage			V _{GSS}	- 6	V
Continuous Drain Current (Note C) // 45//	t<10s	$T_A = +25$ °C $T_A = +70$ °C	l _D	-13 -10	А
Continuous Drain Current (Note 6) V _{GS} = 4.5V	Steady State	$T_C = +25$ °C $T_C = +70$ °C	l _D	-19 -15	А
Maximum Continuous Body Diode Forward Current (Note 6)			I _S	3	Α
Pulsed Drain Current (380µs Pulse, Duty Cycle = 1%)			I _{DM}	70	Α
Avalanche Current (Note 7) L = 0.3mH			I _{AS}	24	А
Avalanche Energy (Note 7) L = 0.3mH			Eas	86	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)		P_D	1.05	W
Thermal Begintenes, Junction to Ambient (Note 5)		2	118	°C/W
Thermal Resistance, Junction to Ambient (Note 5)	t<10s	$R_{\theta JA}$	83.5	C/VV
Total Power Dissipation (Note 6)		P_D	2.16	W
Thermal Begistenes, Junetion to Ambient (Note 6)		D	57	
Thermal Resistance, Junction to Ambient (Note 6)	t<10s	$R_{\theta JA}$	40.3	°C/W
Thermal Resistance, Junction to Case (Note 6)	$R_{ heta JC}$	11.7		
Operating and Storage Temperature Range		$T_{J_{i}}T_{STG}$	-55 to +150	°C

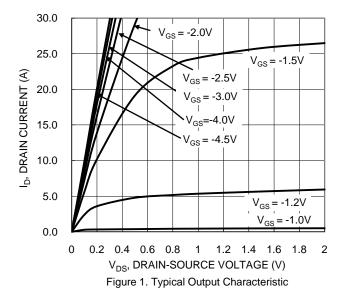
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage		-12	_	_	V	$V_{GS} = 0V, I_D = -250\mu A$	
Zero Gate Voltage Drain Current (T _J = +25°C)	I _{DSS}	1	_	-1	μA	$V_{DS} = -9.6V, V_{GS} = 0V$	
Gate-Source Leakage		_	_	-100	nA	$V_{GS} = -6V$, $V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	V _{GS(TH)}	-0.6	_	-1.2	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
Static Drain-Source On-Resistance	RDS(ON)	1	9.8	11.7	mΩ	$V_{GS} = -4.5V$, $I_{D} = -12A$	
Static Drain-Source Off-Resistance	KDS(ON)	1	14.6	18.6	11122	$V_{GS} = -2.5V, I_{D} = -9A$	
Diode Forward Voltage	V_{SD}	1	-0.8	-1.0	V	$V_{GS} = 0V, I_{S} = -16A$	
DYNAMIC CHARACTERISTICS (Note 9)							
Input Capacitance	Ciss	-	913	_		V _{DS} = -6V, V _{GS} = 0V, f = 1.0MHz	
Output Capacitance	Coss		458		pF		
Reverse Transfer Capacitance	C_{rss}		53	_			
Gate Resistance	R_g	_	1.85	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$	
Total Gate Charge (V _{GS} = -6V)	Q_g	1	9.5	_			
Total Gate Charge (V _{GS} = -4.5V)	Q_g		7.1	_	nC	Vps = -6V. Ip = -12A	
Gate-Source Charge	Q_{gs}	_	1.4	_	IIC	V _{DS} = -0V, I _D = -12A	
Gate-Drain Charge	Q_{gd}	_	1.1	_			
Turn-On Delay Time	t _{D(ON)}	_	6.3	_			
Turn-On Rise Time	t _R	_	2.6	_		$V_{DS} = -6V$, $V_{GS} = -4.5V$, $R_L = 1\Omega$, $R_g = 4.7\Omega$, $I_D = -12A$	
Turn-Off Delay Time	t _{D(OFF)}	_	14.4	_	ns		
Turn-Off Fall Time	t _F		3.9	_			
Body Diode Reverse Recovery Time	t _{RR}	_	13.5	_	ns	I _F = -12A, dI/dt = 100A/μs	
Body Diode Reverse Recovery Charge	Q_{RR}	_	2.5	_	nC	I _F = -12A, dl/dt = 100A/µs	

Notes:

- 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.
- 7. IAs and EAs ratings are based on low frequency and duty cycles to keep T_J = +25°C.
 8. Short duration pulse test used to minimize self-heating effect.
 9. Guaranteed by design. Not subject to production testing.





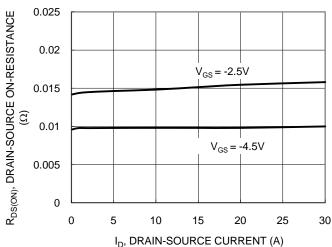


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

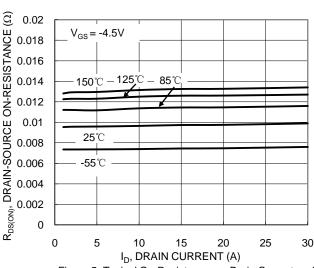
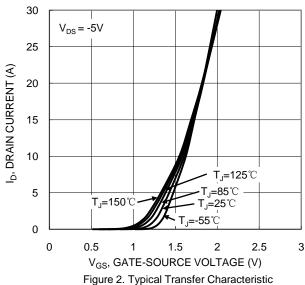


Figure 5. Typical On-Resistance vs. Drain Current and Temperature



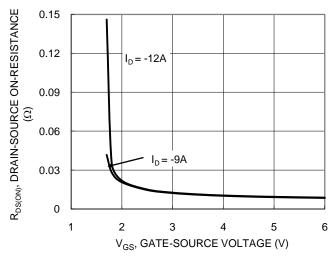


Figure 4. Typical Transfer Characteristic

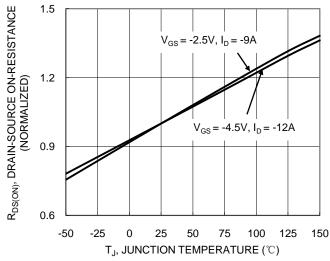


Figure 6. On-Resistance Variation with Temperature



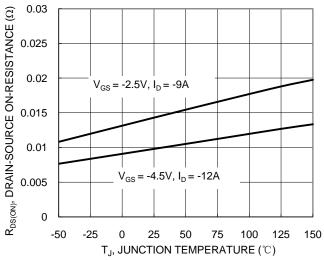


Figure 7. On-Resistance Variation with Temperature

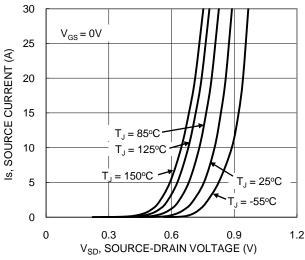
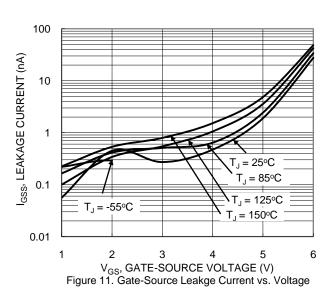


Figure 9. Diode Forward Voltage vs. Current



1.2 $V_{\text{GS}(TH)}$, GATE THRESHOLD VOLTAGE (V) $I_D = -1mA$ 8.0 $I_{D} = -250 \mu A$ 0.6 0.4 0.2 0 -50 -25 25 50 75 100 125 150 T_J , JUNCTION TEMPERATURE ($^{\circ}$ C)

Figure 8. Gate Threshold Variation vs. Junciton Temperature

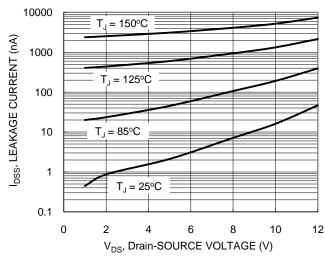
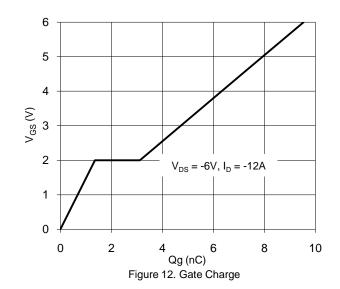
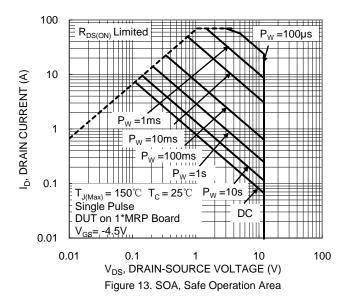
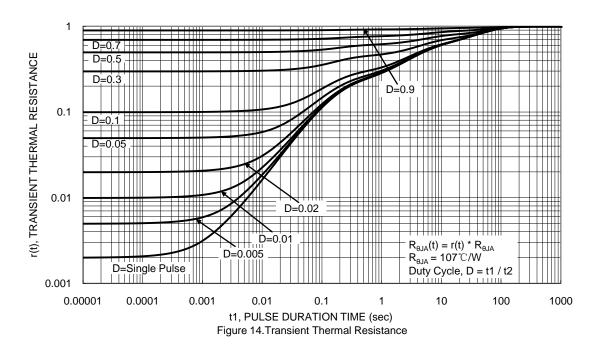


Figure 10. Typical Drain-Source Leakge Current vs. Voltage







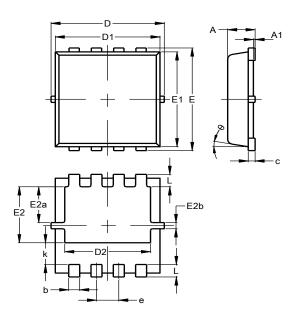




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8 (Type UX)

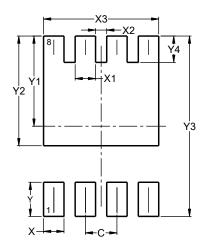


PowerDI3333-8 (Type UX)					
Dim	Min	Max	Тур		
Α	0.75	0.85	0.80		
A1	0.00	0.05	-		
b	0.25	0.40	0.32		
С	0.10	0.25	0.15		
D	3.20	3.40	3.30		
D1	2.95	3.15	3.05		
D2	2.30	2.70	2.50		
Е	3.20	3.40	3.30		
E1	2.95	3.15	3.05		
E2	1.60	2.00	1.80		
E2a	0.95	1.35	1.15		
E2b	0.10	0.30	0.20		
е	0.65 BSC				
k	0.50	0.90	0.70		
L	0.30	0.50	0.40		
θ	0°	12°	10°		
All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8 (Type UX)



Dimensions	Value (in mm)		
С	0.650		
X	0.420		
X1	0.420		
X2	0.230		
Х3	2.370		
Y	0.700		
Y1	1.850		
Y2	2.250		
Y3	3.700		
Y4	0.540		



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