

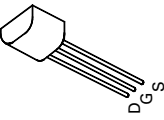
ZVP3310A

P-CHANNEL ENHANCEMENT
MODE VERTICAL DMOS FET

ISSUE 2 – MARCH 94

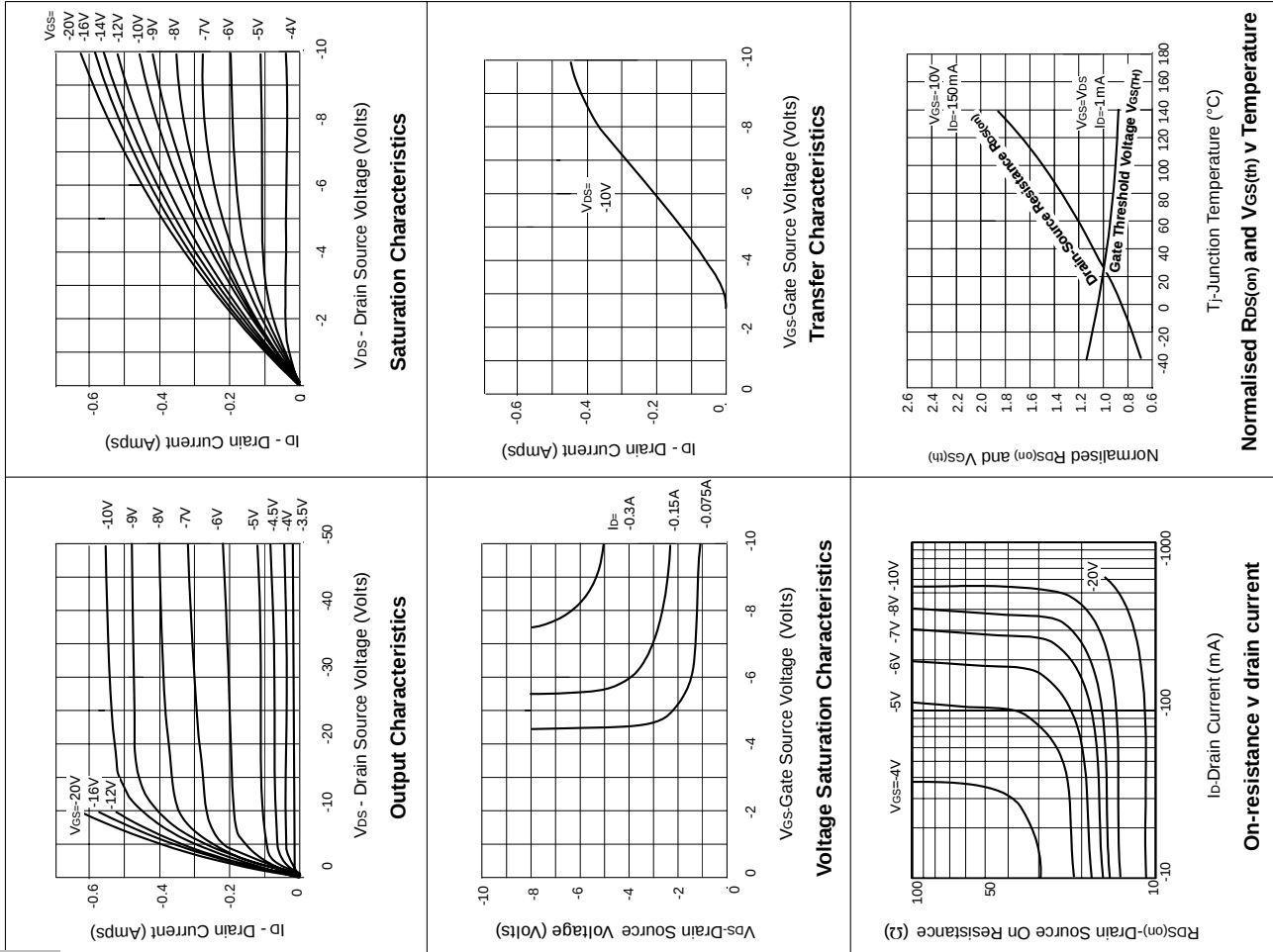
FEATURES

- * 100 Volt V_{DS}
- * $R_{DS(on)}=20\Omega$



E-Line
TO92 Compatible

TYPICAL CHARACTERISTICS



P-CHANNEL ENHANCEMENT
MODE VERTICAL DMOS FET

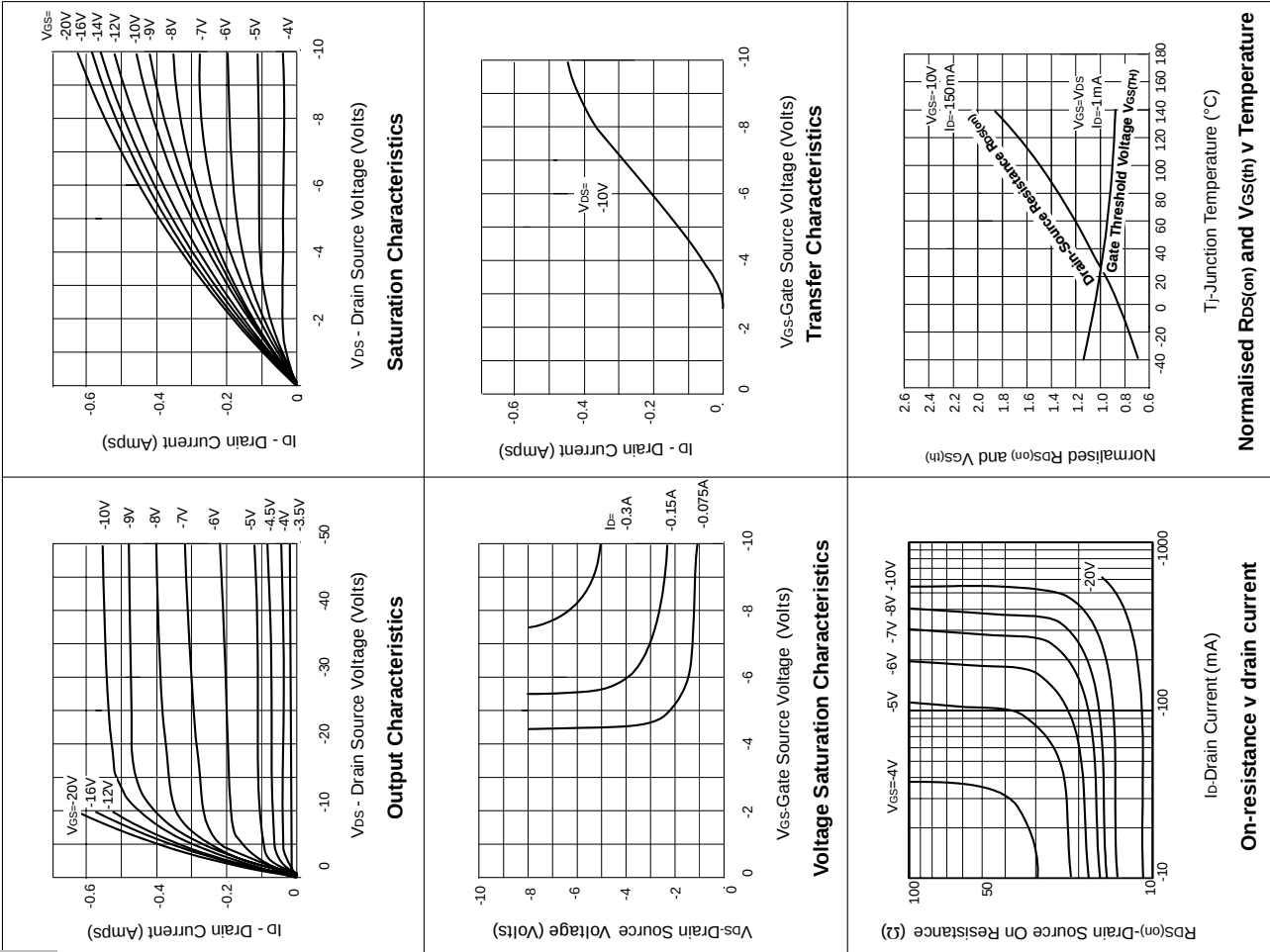
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FEATURES

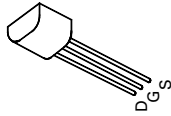
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ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	-100	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	I_D	-140	mA
Pulsed Drain Current	I_{DM}	-1.2	A
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}C$	P_{tot}	625	mW
Operating and Storage Temperature Range	T_j, T_{stg}	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	-100		V	$I_D = -1mA, V_{GS} = 0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	$I_D = -1mA, V_{DS} = V_{GS}$
Gate-Body Leakage	I_{GSS}		20	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Zero Gate Voltage Drain Current	I_{DSS}		-1	μA	$V_{DS} = -100V, V_{GS} = 0$
On-State Drain Current (1)	$I_{D(on)}$	-300		mA	$V_{DS} = -80V, V_{GS} = 0V, T = 125^{\circ}C(2)$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		20	Ω	$V_{DS} = -25V, V_{GS} = -10V$
Forward Transconductance (1)(2)	g_{fs}	50		mS	$V_{DS} = -10V, I_D = -150mA$
Input Capacitance (2)	C_{iss}		50	pF	$V_{DS} = -25V, I_D = -150mA$
Common Source Output Capacitance (2)	C_{oss}		15	pF	$V_{DS} = -25V, V_{GS} = 0V, f = 1MHz$
Reverse Transfer Capacitance (2)	C_{rss}		5	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		8	ns	
Rise Time (2)(3)	t_r		8	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		8	ns	$V_{DD} = -25V, I_D = -150mA$
Fall Time (2)(3)	t_f		8	ns	

(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$

(2) Sample test.

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TYPICAL CHARACTERISTICS

