

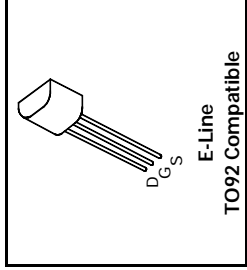
# ZVN3306A

## N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

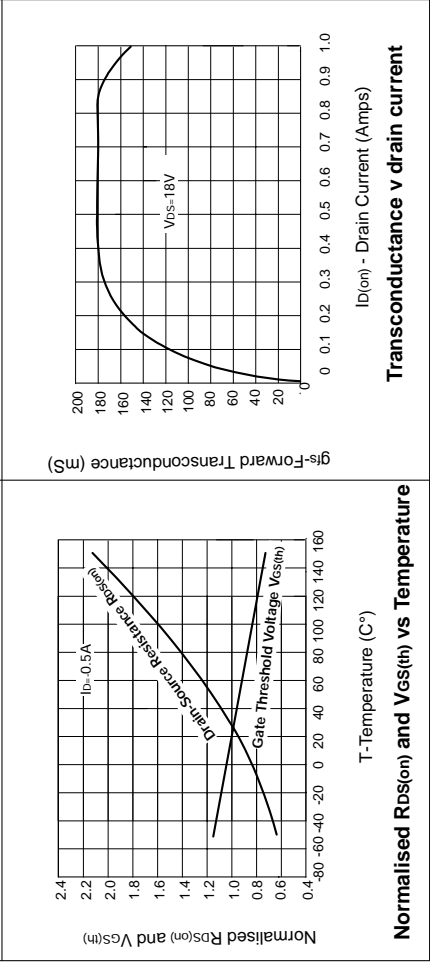
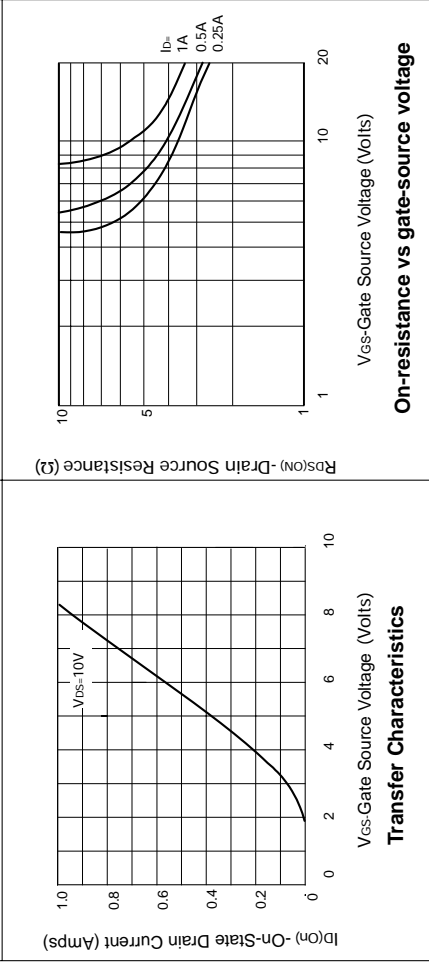
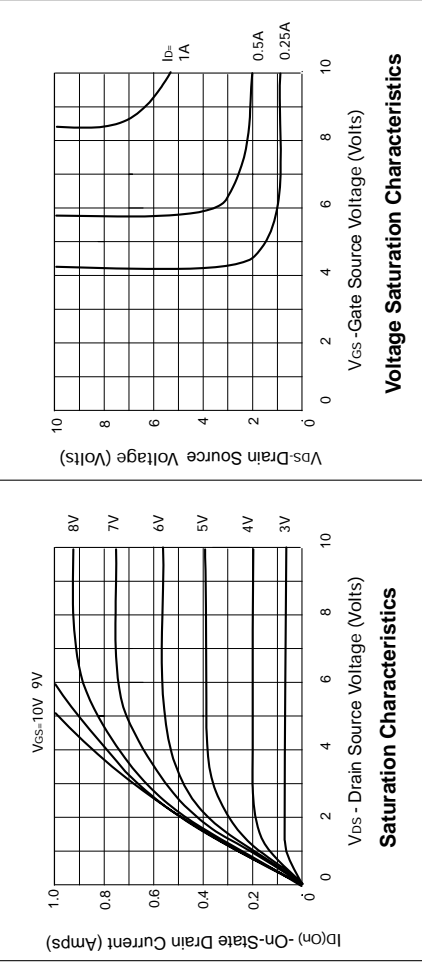
ISSUE 2 – MARCH 94

### FEATURES

- \* 60 Volt  $V_{DS}$
- \*  $R_{DS(on)} = 5\Omega$



### TYPICAL CHARACTERISTICS



# ZVN3306A

### ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	$V_{DS}$	60	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	$I_D$	270	mA
Pulsed Drain Current	$I_{DM}$	3	A
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation at $T_{amb}=25^{\circ}C$	$P_{tot}$	625	mW
Operating and Storage Temperature Range	$T_j, T_{stg}$	-55 to +150	$^{\circ}C$

### ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	$BV_{DSS}$	60		V	$I_D = 1mA, V_{GS} = 0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.8	2.4	V	$I_D = 1mA, V_{DS} = V_{GS}$
Gate-Body Leakage	$I_{GSS}$		20	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Zero Gate Voltage Drain Current	$I_{DSS}$		0.5 50	$\mu A$ $\mu A$	$V_{DS} = 60V, V_{GS} = 0$ $V_{DS} = 48V, V_{GS} = 0V, T = 125^{\circ}C(2)$
On-State Drain Current(1)	$I_{D(on)}$	750		mA	$V_{DS} = 18V, V_{GS} = 10V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		5	$\Omega$	$V_{GS} = 10V, I_D = 500mA$
Forward Transconductance(1)(2) $g_{fs}$		150		mS	$V_{DS} = 18V, I_D = 500mA$
Input Capacitance (2)	$C_{iss}$		35	pF	
Common Source Output Capacitance (2)	$C_{oss}$		25	pF	$V_{DS} = 18V, V_{GS} = 0V, f = 1MHz$
Reverse Transfer Capacitance (2)	$C_{riss}$		8	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		5	ns	
Rise Time (2)(3)	$t_r$		7	ns	$V_{DD} = 18V, I_D = 500mA$
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		6	ns	
Fall Time (2)(3)	$t_f$		8	ns	

(1) Measured under pulsed conditions. Width=300 $\mu s$ . Duty cycle  $\leq 2\%$   
3-375

(2) Sample test.

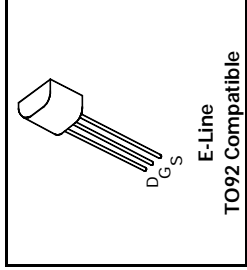
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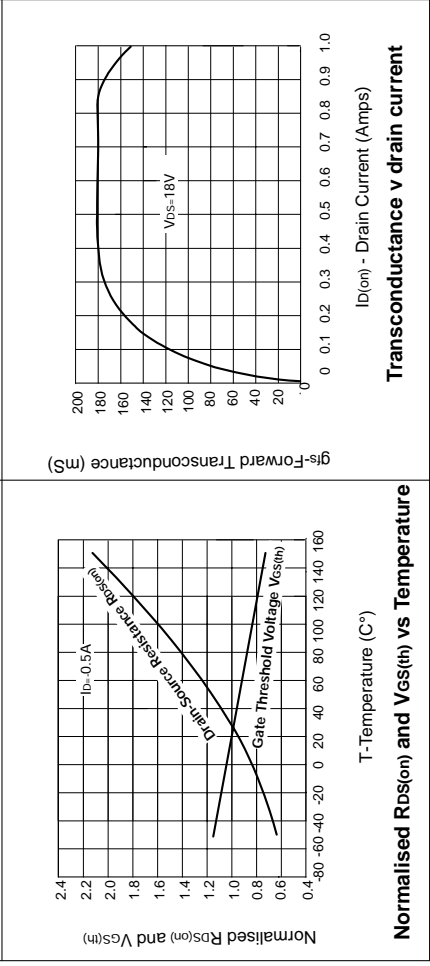
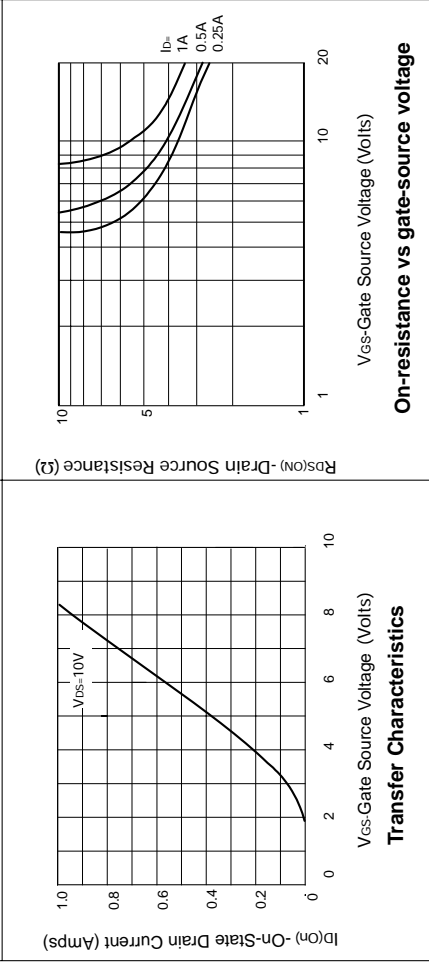
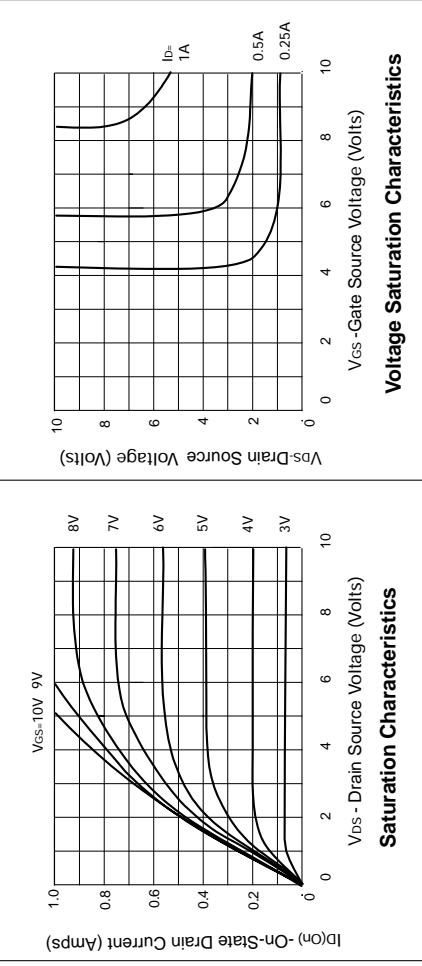
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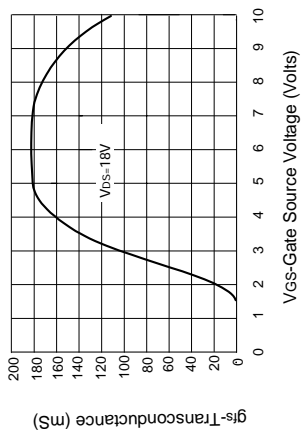
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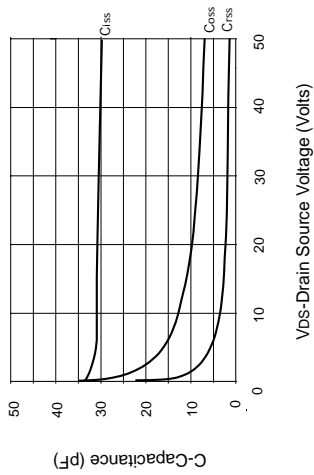
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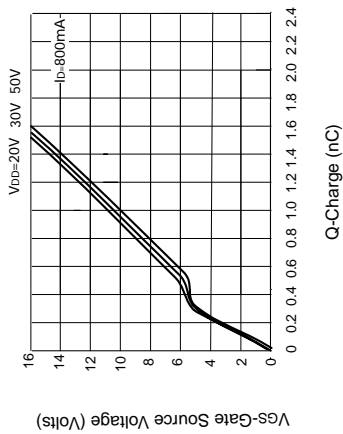
## TYPICAL CHARACTERISTICS



**Transconductance v gate-source voltage**



**Capacitance v drain-source voltage**



**Gate charge v gate-source voltage**