

P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ISSUE 2 – MARCH 94

FEATURES

- * 200 Volt V_{DS}
- * $R_{DS(on)}=25\Omega$

REFER TO ZVP2120A FOR GRAPHS

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	-200	V
Continuous Drain Current at $T_{amb}=25^{\circ}\text{C}$	I_D	-120	mA
Pulsed Drain Current	I_{DM}	-1.2	A
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}\text{C}$	P_{tot}	700	mW
Operating and Storage Temperature Range	T_j, T_{stg}	-55 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	-200		V	$I_D=-1\text{mA}, V_{GS}=0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	$I_D=-1\text{mA}, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		20	nA	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}		-10 -100	μA μA	$V_{DS}=200\text{V}, V_{GS}=0$ $V_{DS}=160\text{V}, V_{GS}=0\text{V}, T=125^{\circ}\text{C}(2)$
On-State Drain Current(1)	$I_{D(on)}$	-300		mA	$V_{DS}=25\text{V}, V_{GS}=-10\text{V}$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		25	Ω	$V_{GS}=-10\text{V}, I_D=-150\text{mA}$
Forward Transconductance (1)(2)	g_{fs}	50		mS	$V_{DS}=-25\text{V}, I_D=-150\text{mA}$
Input Capacitance (2)	C_{iss}		100	pF	
Common Source Output Capacitance (2)	C_{oss}		25	pF	$V_{DS}=-25\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$
Reverse Transfer Capacitance (2)	C_{rss}		7	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	
Rise Time (2)(3)	t_r		15	ns	$V_{DD}=-25\text{V}, I_D=-150\text{mA}$
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		12	ns	
Fall Time (2)(3)	t_f		15	ns	

(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$

(2) Sample test.

(3) Switching times measured with 50 Ω source impedance and $\leq 5\text{ns}$ rise time on a pulse generator

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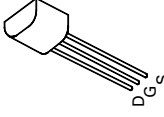
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	-200		V	$I_D=-1\text{mA}, V_{GS}=0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	$I_D=-1\text{mA}, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		20	nA	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}		-10 -100	μA μA	$V_{DS}=200\text{V}, V_{GS}=0$ $V_{DS}=160\text{V}, V_{GS}=0\text{V}, T=125^{\circ}\text{C}(2)$
On-State Drain Current(1)	$I_{D(on)}$	-300		mA	$V_{DS}=25\text{V}, V_{GS}=-10\text{V}$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		25	Ω	$V_{GS}=-10\text{V}, I_D=-150\text{mA}$
Forward Transconductance (1)(2)	g_{fs}	50		mS	$V_{DS}=-25\text{V}, I_D=-150\text{mA}$
Input Capacitance (2)	C_{iss}		100	pF	
Common Source Output Capacitance (2)	C_{oss}		25	pF	$V_{DS}=-25\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$
Reverse Transfer Capacitance (2)	C_{rss}		7	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	
Rise Time (2)(3)	t_r		15	ns	$V_{DD}=-25\text{V}, I_D=-150\text{mA}$
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		12	ns	
Fall Time (2)(3)	t_f		15	ns	

(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$

(2) Sample test.

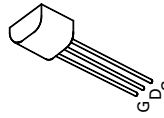
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ZVP2120A



E-Line
TO92 Compatible

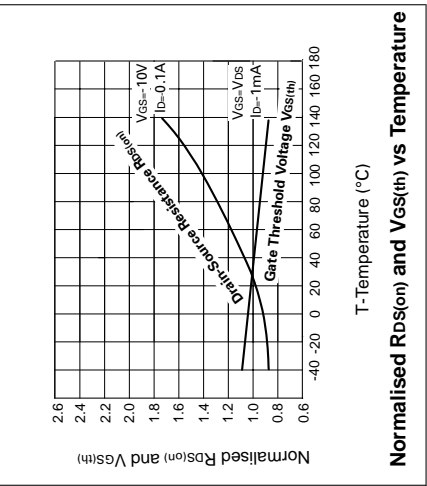
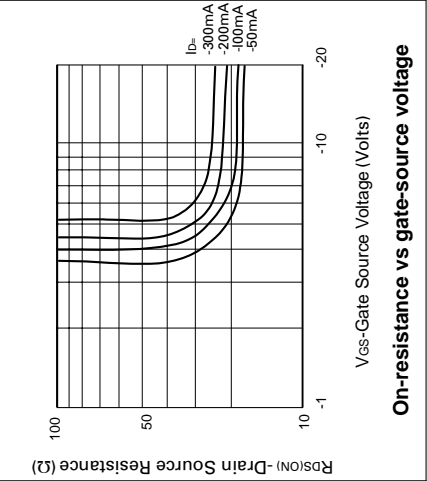
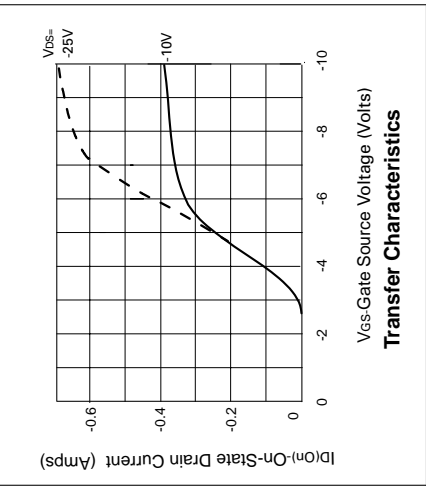
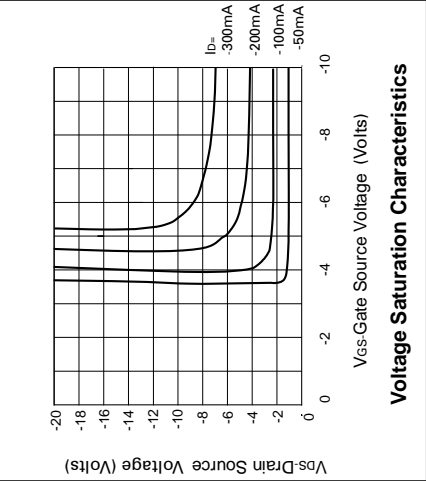
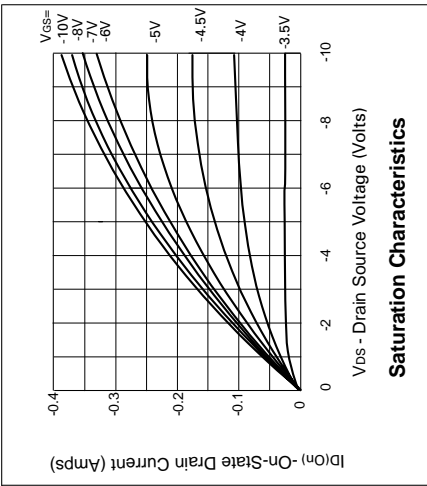
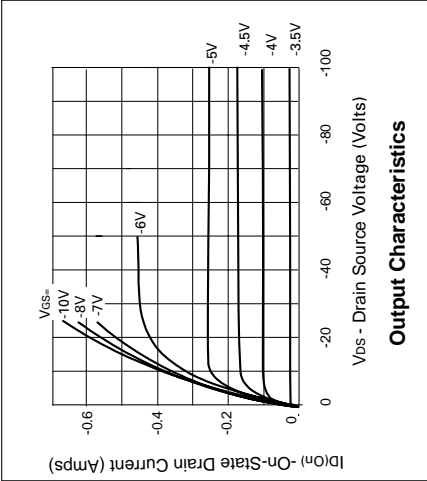
ZVP2120C



E-Line
TO92 Compatible

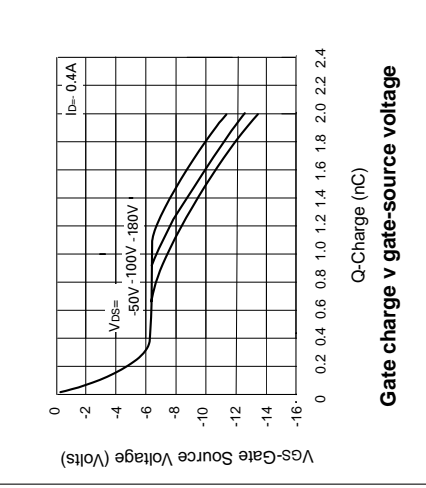
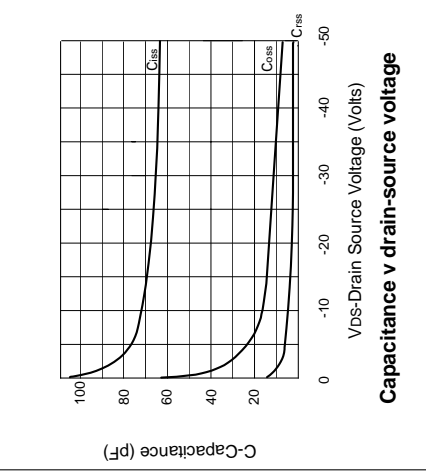
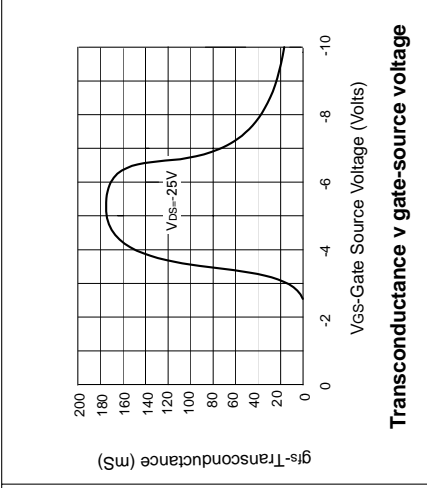
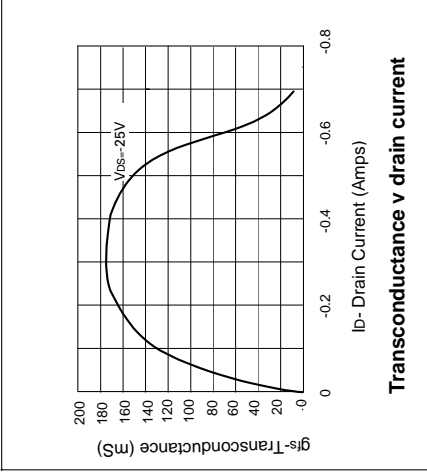
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TYPICAL CHARACTERISTICS



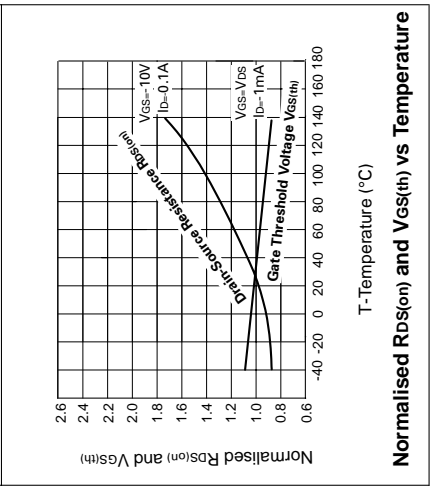
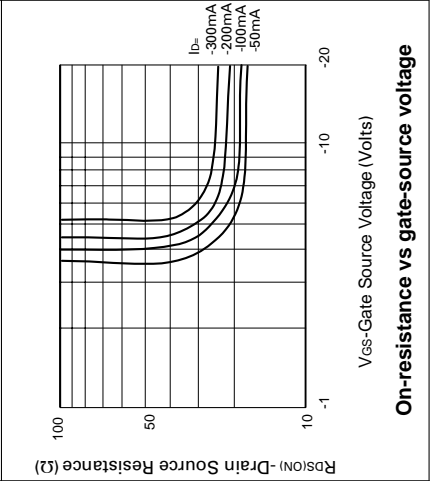
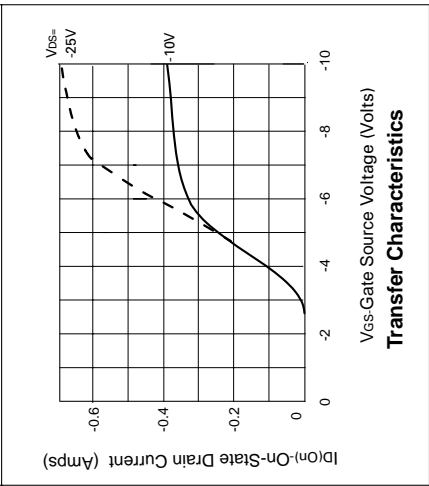
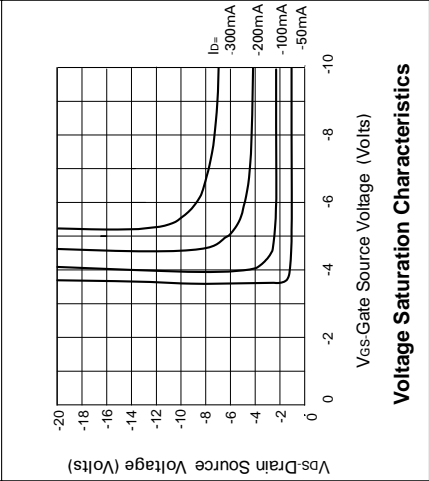
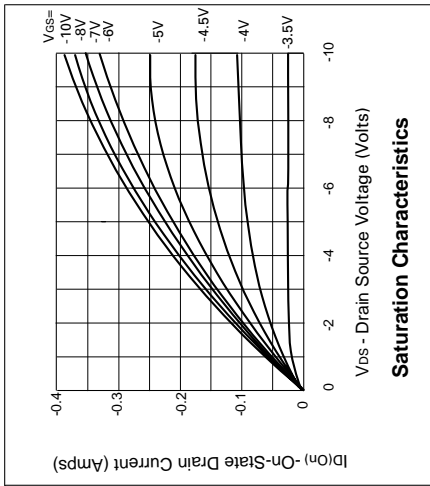
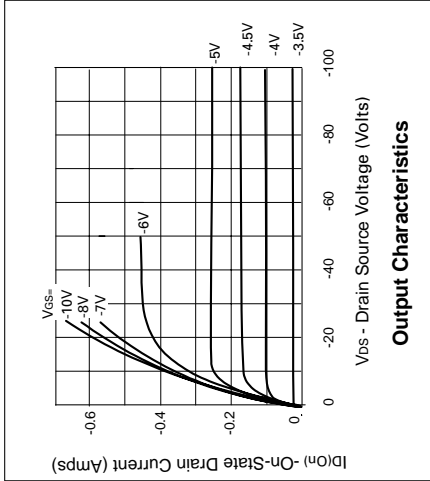
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