





N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{DS(ON)} max	I _D max
50V	4Ω @ $V_{GS} = 4V$	160mA

Features and Benefits

- Low On-Resistance
- Very Low Gate Threshold Voltage
- Low Input Capacitance
- ESD Protected Gate to 2kV
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control
 (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and
 manufactured in IATF 16949 certified facilities), please
 contact us or your local Diodes representative.

https://www.diodes.com/quality/product-definitions/

Description and Applications

This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Motor Driving
- Power Management Functions
- Load Switching

Mechanical Data

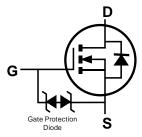
- Case: SOT523
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 Leadframe. Solderable per MIL-STD-202, Method 208 (3)
- Terminal Connections: See Diagram
- Weight: 0.002 grams (Approximate)

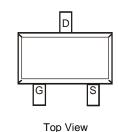




SOT523

Top View





Equivalent Circuit

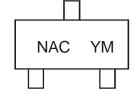
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN55D0UT-7	SOT523	3,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



NAC = Product Type Marking Code YM = Date Code Marking Y or \overline{Y} = Year (ex: H = 2020) M = Month (ex: 9 = September)

Date Code Key

Date Code Ney												
Year	2008		2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	V		Η		J	K	L	М	Ν	0	Р	R
						_		_	_			
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	VDSS	50	V
Gate-Source Voltage	V _{GSS}	±12	V
Drain Current (Note 5) Continuous	ID	160	mA
Pulsed Drain Current (Note 5)	I _{DM}	560	mA

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	PD	200	mW
Thermal Resistance, Junction to Ambient	RθJA	625	°C/W
Operating and Storage Temperature Range	TJ, TSTG	-55 to +150	°C

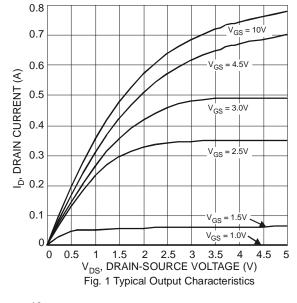
Electrical Characteristics (@TA = +25°C, unless otherwise specified.)

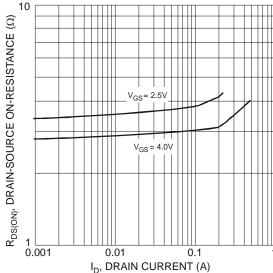
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)	Cyllida	141111	ıур	Wax	Oint	rest condition
Drain-Source Breakdown Voltage	BV _{DSS}	50			V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current	IDSS			1	μA	V _{DS} = 50V, V _{GS} = 0V
Gate-Source Leakage	Igss	_	_	1.0 5.0	μA	$V_{GS} = \pm 8V, V_{DS} = 0V$ $V_{GS} = \pm 12V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	V _{GS(TH)}	0.7	0.8	1.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
Chatia Dunin Course On Registeres		_	3.1	4	0	$V_{GS} = 4V, I_{D} = 100mA$
Static Drain-Source On-Resistance	RDS(ON)	_	4	5	Ω	$V_{GS} = 2.5V, I_{D} = 80mA$
Forward Transconductance	g FS	180			mS	$V_{DS} = 10V$, $I_D = 100mA$, $f = 1.0kHz$
Diode Forward Voltage	VsD	_	0.70	1.3	V	V _{GS} = 0V, I _S = 100mA
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	Ciss	_	25		pF	
Output Capacitance	Coss		5		рF	V _{DS} = 10V, V _{GS} = 0V, f = 1.0MHz
Reverse Transfer Capacitance	Crss		2.1		рF	
Gate Resistance	Rg	_	500	_	Ω	$f = 1MHz$, $V_{GS} = 0V$, $V_{DS} = 0V$
Total Gate Charge (V _{GS} = 4V)	QG	_	295	_	рC	
Total Gate Charge (V _{GS} = 8V)	QG	_	636	_	рC	V _{DS} = 10V,
Gate-Source Charge	Q _{GS}	_	72	_	рC	$I_D = 100 \text{mA}$
Gate-Drain Charge	Q _{GD}	_	18	_	рC	
Turn-On Delay Time	td(ON)	_	6.0	_	ns	
Turn-On Rise Time	t _R	_	4.4	_	ns	$V_{DD} = 10V, V_{GS} = 4V,$
Turn-Off Delay Time	tD(OFF)	_	23.4	_	ns	$R_G = 25\Omega$, $I_D = 100mA$
Turn-Off Fall Time	tF	_	11.0	_	ns	

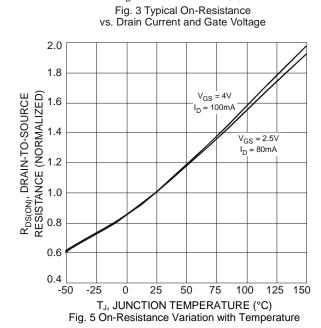
Notes:

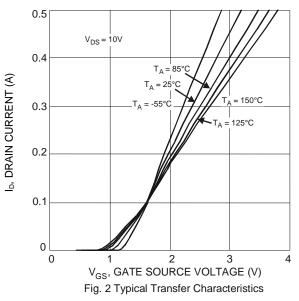
- 5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
- 6. Short duration pulse test used to minimize self-heating effect.
- 7. Guaranteed by design. Not subject to product testing.











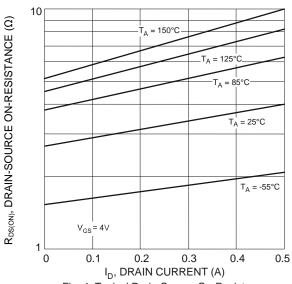
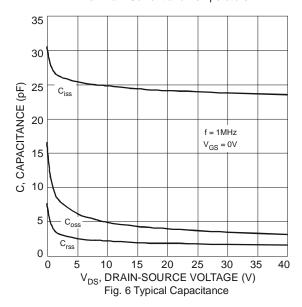


Fig. 4 Typical Drain-Source On-Resistance vs. Drain Current and Temperature





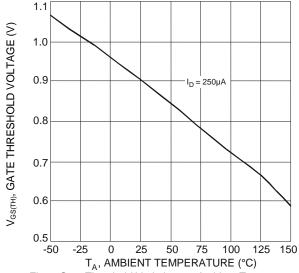
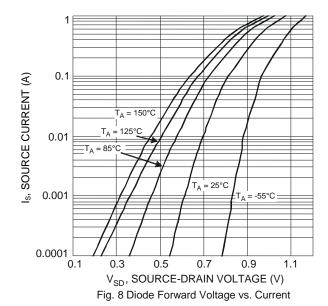
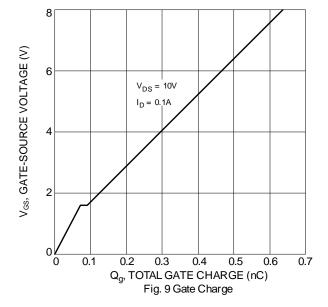


Fig. 7 Gate Threshold Variation vs. Ambient Temperature





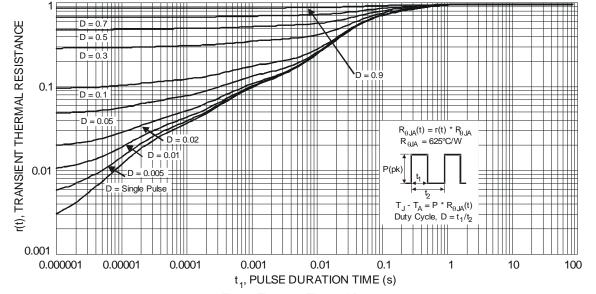


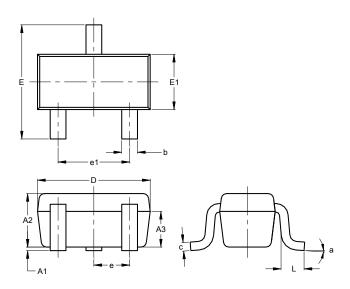
Fig. 10 Transient Thermal Response



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

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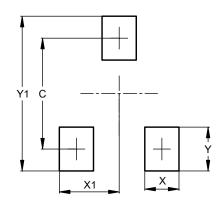


	SOT523						
Dim	Min	Max	Тур				
A1	0.00	0.10	0.05				
A2	0.60	0.80	0.75				
A3	0.45	0.65	0.50				
b	0.15	0.30	0.22				
С	0.10	0.20	0.12				
D	1.50	1.70	1.60				
Е	1.45	1.75	1.60				
E1	0.75	0.85	0.80				
е	0.50 BSC						
e1	0.90	1.10	1.00				
L	0.20	0.40	0.33				
а	0°		8°				
All Dimensions in mm							

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT523



Dimensions	Value (in mm)
С	1.29
Х	0.40
X1	0.70
Y	0.51
Y1	1.80



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