

AP22953

SWITCH FOR VBUS LINE WITH OVERVOLTAGE, SURGE, AND ESD PROTECTION

Description

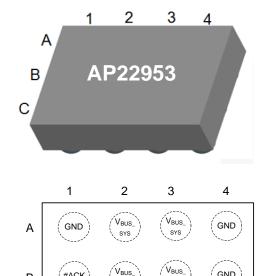
The AP22953 device is a single-chip solution for USB 2.0/3.0/Type-C connector VBUS line protection. The bidirectional MOSFET switch ensures normal current flow in both charging and host mode while protecting the internal circuits from overvoltage conditions at the V_{BUS CON} pin. On the V_{BUS CON} pin, the device has overvoltage protection up to 30V. After the #EN pin is pulled low, the AP22953 counts 20ms before turning on the MOSFET via soft-start delay. The #ACK pin indicates the MOSFET is fully turned ON.

The typical application interface for the AP22953 is the V_{BUS} line in USB connectors. Typical end equipment for the AP22953 include smartphones, tablet PCs, wearables, and electronic-point-of-sale (EPOS) systems. The AP22953 can also be used with other devices that use a 5V power rail interface.

Overtemperature protection turns off the switch at 145°C (typical).

The AP22953 is available in the wafer level chip scale W-WLB2013-12 1.988mm x 1.288mm x 0.64mm package with backside laminate.

Pin Assignments



 V_{BUS}

SYS

 $V_{BUS_{-}}$

CON

WL-CSP (Top View)

CON

. V_{BUS}

CON

GND

GND

Features

- Surge protection
 - IEC61000-4-5 >100V
- Integrated 39mΩ (typ) N-Channel MOSFET Switch
- Overvoltage Protection (OVP) at V_{BUS CON} Up to 30VDC
- Integrated Input Enable and Status Output Signal
- Overtemperature Protection (OTP)
- **ESD Protection**
 - Human Body Model >4kV
 - Charged Device Model >1kV
 - IEC61000-4-2 Air Discharge >15kV
 - IEC61000-4-2 Contact Discharge >15kV
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

https://www.diodes.com/quality/product-definitions/

Applications

- **Smartphones**
- Tablet PCs
- Wearables
- Electronic-Point-of-Sale (EPOS) Systems

#ACK

#EN

В

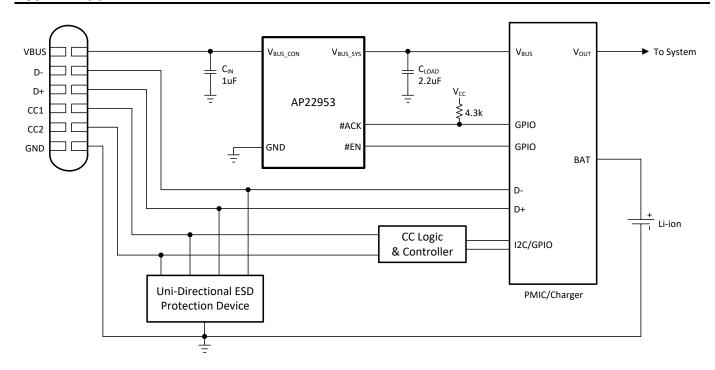
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Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + CI) and <1000ppm antimony compounds.



Typical Applications Circuit

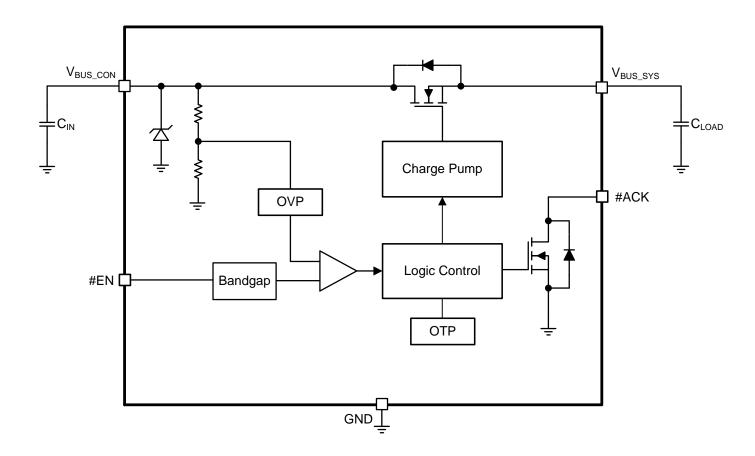


Pin Descriptions

Pin Name	Pin Number	I/O	Function
V _{BUS_CON}	B3, C2, C3	I/O	Supply voltage from USB connector V_{BUS} pin. Bypass V_{BUS_CON} with a 1 μ F ceramic capacitor as close as possible to the device.
V _{BUS_SYS}	A2, A3, B2	I/O	Internal supply voltage rail to PMIC V_{BUS} plane. Bypass V_{BUS_SYS} with a 2.2 μ F ceramic capacitor as close as possible to the device.
#ACK	B1	0	Open-Drain Acknowledge pin.
#EN	C1	I	Enable Active-Low Input. Drive #EN low to enable the switch. Drive #EN high to disable the switch.
GND	A1, A4, B4, C4	Ground	Device ground. Connect to PCB ground plane



Functional Block Diagram





Absolute Maximum Ratings (@ T_A = +25°C, unless otherwise specified.)

Symbol		Parameter	Ratings	Unit
НВМ		Human Body Model ESD Protection	4	kV
CDM		Charged Device Model ESD Protection	1	kV
ESD	IEC system level	IEC 61000-4-2. Contact Discharge, V _{BUS_CON} (Note 4)	15	kV
	IEC system level	IEC 61000-4-2. Air Gap Discharge, V _{BUS_CON} (Note 4)	15	kV
Surge		IEC 61000-4-5 Surge Protection, V _{BUS_CON} (Note 4)	100	V
V _{BUS_CON}		Supply voltage from USB connector	-0.3 to +30	V
	V _{BUS_SYS}	Internal supply DC voltage rail on the PCB	-0.3 to +7	V
	#ACK, #EN	V _{#ACK} , V _{#EN} Voltages	-0.3 to +7	V
I _{CON} , I _{SYS}		Switch I/O Current (Continuous)	3.5	Α
T _A		Operating Ambient Temperature	-40 to +85	°C
T _{ST}		Storage Temperature Range	-40 to +150	°C
P _D		Power Dissipation	670	mW
Reja		Thermal Resistance, Junction to Ambient	89	°C/W
ReJC		Thermal Resistance, Junction to Case	0.6	°C/W

Notes:

Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Recommended Operating Conditions (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Nom	Max	Unit
V _{BUS_CON}	Supply voltage from USB connector	_	_	5.9	V
V _{BUS_SYS}	Internal supply DC voltage rail on the PCB	_	_	5.9	V
C _{LOAD}	Output load capacitance, V _{BUS_SYS} pin	_	2.2	_	μF
C _{IN}	Input capacitance, V _{BUS_CON} pin	_	1	_	μF
R _{PULL-UP}	Pull-up resistor, #ACK	_	4.3	100	kΩ
I _{VBUS}	Continuous current on V _{BUS_CON} and V _{BUS_SYS} pins	_	_	3.5	А
I _{DIODE}	Continuous current through the MOSFET body diode	_	_	1	Α

^{4.} The JEDEC high-K (2s2p) board used to derive this data was a 3in x 3in, multilayer board with 1oz internal power and ground planes with 2oz copper traces on top and bottom of the board.

5. EVM has been tested per typical circuit with capacitors connected to the V_{BUS_CON} and V_{BUS_SYS}.



$\textbf{Electrical Characteristics} \ (\textcircled{@} \ T_{A} = +25^{\circ}C, \ unless \ otherwise \ specified. \ C_{IN} = 1 \mu F, \ C_{OUT} = 2.2 \mu F.$

Typical values are at $V_{BUS} = +5.0V$, $I_{VBUS} \le 3.5A$) (Note 6)

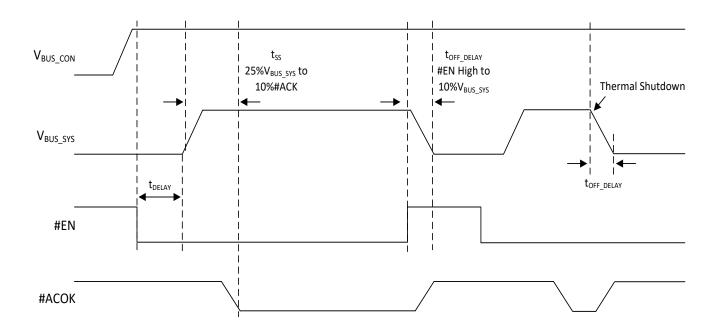
HOST_LEAK I/O Voltage Pro VovP_RISING VHYS_OVP VOVP_FALLING VUVLO	V _{BUS_CON} operating current consumption V _{BUS_CON} operating current consumption Host mode leakage current otection Input overvoltage protection threshold, V _{BUS_CON} Hysteresis on OVP, V _{BUS_CON} Input overvoltage protection threshold, V _{BUS_CON} Input overvoltage protection threshold, V _{BUS_CON} Input overvoltage lockout, V _{BUS_CON} Hysteresis on UVLO, V _{BUS_CON}	Measured at V _{BUS_CON} pin, V _{BUS_CON} = 5V, #EN = 5V Measured at V _{BUS_CON} pin, V _{BUS_CON} = 5V, #EN = 0V and no load Measured at V _{BUS_SYS} pin, V _{BUS_SYS} = 5V, #EN = 0V and V _{BUS_CON} = Hi-Z Measured at V _{BUS_SYS} pin, V _{BUS_SYS} = 5V, #EN = 5V and V _{BUS_CON} = Hi-Z V _{BUS_CON} increasing from 5V V _{BUS_CON} decreasing from 7V to 5V V _{BUS_CON} decreasing from 7V to 5V V _{BUS_CON} voltage rising from 0V to 5V		30 175 175 110 6.2 50	70 373 373 — 6.4 —	μΑ μΑ μΑ μΑ ν ν
I VBUS SYS I HOST_LEAK I/O Voltage Pro VovP_RISING VHYS_OVP VOVP_FALLING VUVLO	consumption V _{BUS_CON} operating current consumption Host mode leakage current otection Input overvoltage protection threshold, V _{BUS_CON} Hysteresis on OVP, V _{BUS_CON} Input overvoltage protection threshold, V _{BUS_CON} Input undervoltage lockout, V _{BUS_CON}	Measured at V _{BUS_CON} pin, V _{BUS_CON} = 5V, #EN = 0V and no load Measured at V _{BUS_SYS} pin, V _{BUS_SYS} = 5V, #EN = 0V and V _{BUS_CON} = Hi-Z Measured at V _{BUS_SYS} pin, V _{BUS_SYS} = 5V, #EN = 5V and V _{BUS_CON} = Hi-Z V _{BUS_CON} increasing from 5V V _{BUS_CON} decreasing from 7V to 5V V _{BUS_CON} decreasing from 7V to 5V	- - - 6 -	175 175 110 6.2 50	373 373 — 6.4	μΑ μΑ μΑ
I_VBUS_SYS I_HOST_LEAK I/O Voltage Pro VovP_RISING VHYS_OVP VOVP_FALLING VUVLO	consumption V _{BUS_CON} operating current consumption Host mode leakage current otection Input overvoltage protection threshold, V _{BUS_CON} Hysteresis on OVP, V _{BUS_CON} Input overvoltage protection threshold, V _{BUS_CON} Input undervoltage lockout, V _{BUS_CON}	no load Measured at V_{BUS_SYS} pin, $V_{BUS_SYS} = 5V$, #EN = 0V and $V_{BUS_CON} = Hi-Z$ Measured at V_{BUS_SYS} pin, $V_{BUS_SYS} = 5V$, #EN = 5V and $V_{BUS_CON} = Hi-Z$ V_{BUS_CON} increasing from 5V V_{BUS_CON} decreasing from 7V to 5V V_{BUS_CON} decreasing from 7V to 5V	_	175 110 6.2 50	373 — 6.4	μA μA V
I _{HOST_LEAK} I/O Voltage Pro V _{OVP_RISING} V _{HYS_OVP} V _{OVP_FALLING} V _{UVLO}	consumption Host mode leakage current otection Input overvoltage protection threshold, V _{BUS_CON} Hysteresis on OVP, V _{BUS_CON} Input overvoltage protection threshold, V _{BUS_CON} Input undervoltage lockout, V _{BUS_CON}	V _{BUS_CON} = Hi-Z Measured at V _{BUS_SYS} pin, V _{BUS_SYS} = 5V, #EN = 5V and V _{BUS_CON} = Hi-Z V _{BUS_CON} increasing from 5V V _{BUS_CON} decreasing from 7V to 5V V _{BUS_CON} decreasing from 7V to 5V	_	6.2	6.4	μA
VOVP_FALLING VUVLO	Input overvoltage protection threshold, V _{BUS_CON} Hysteresis on OVP, V _{BUS_CON} Input overvoltage protection threshold, V _{BUS_CON} Input undervoltage lockout, V _{BUS_CON}	V _{BUS_CON} = Hi-Z V _{BUS_CON} increasing from 5V V _{BUS_CON} decreasing from 7V to 5V V _{BUS_CON} decreasing from 7V to 5V	_	6.2		V
V _{OVP_RISING} V _{HYS_OVP} V _{OVP_FALLING} V _{UVLO}	Input overvoltage protection threshold, V _{BUS_CON} Hysteresis on OVP, V _{BUS_CON} Input overvoltage protection threshold, V _{BUS_CON} Input undervoltage lockout, V _{BUS_CON}	V _{BUS_CON} decreasing from 7V to 5V V _{BUS_CON} decreasing from 7V to 5V	_	50		
Vovp_rising Vhys_ovp Vovp_falling Vuvlo	threshold, V _{BUS_CON} Hysteresis on OVP, V _{BUS_CON} Input overvoltage protection threshold, V _{BUS_CON} Input undervoltage lockout, V _{BUS_CON}	V _{BUS_CON} decreasing from 7V to 5V V _{BUS_CON} decreasing from 7V to 5V	_	50		
V _{OVP_FALLING}	Input overvoltage protection threshold, V _{BUS_CON} Input undervoltage lockout, V _{BUS_CON}	V _{BUS_CON} decreasing from 7V to 5V	— 5.93		_	mV
V _{OVP_} FALLING V _{UVLO}	threshold, V _{BUS_CON} Input undervoltage lockout, V _{BUS_CON}		5.93	_		
	V _{BUS_CON}	V _{BUS_CON} voltage rising from 0V to 5V			6.37	V
	Hysteresis on UVLO, V _{BUS_CON}		2.3	2.75	3.2	V
V_{HYS_UVLO}		Difference between rising and falling UVLO thresholds	_	100		mV
	Input undervoltage lockout, V _{BUS_CON}	$V_{\scriptsize BUS_CON}$ voltage rising from 5V to 0V	_	2.65	_	V
V _{UVLO_SYS}	V _{BUS_SYS} undervoltage lockout, V _{BUS_SYS}	V _{BUS_SYS} voltage rising from 0V to 5V	2.9	3.35	3.8	V
V _{HYS_UVLO_SYS}	V _{BUS_SYS} UVLO Hysteresis, V _{BUS_SYS}	Difference between rising and falling UVLO thresholds on V _{BUS_SYS}	_	700	_	mV
V _{UVLO_SYS_FALL}	V _{BUS_SYS} undervoltage lockout, v _{BUS_SYS}	V _{BUS_SYS} voltage falling from 7V to 5V	_	2.65	_	V
t _{OVP_RES}	OVP response time	Measured from OVP condition to MOSFET Turn Off. V _{BUS_CON} rises at 1V /100 ns (Notes 8)	_	_	100	ns
t _{OVP_RECOV}	Recovery time	Measured from OVP Clear to MOSFET Turn ON (Notes 9)	_	15	_	ms
Switching Cha	racteristics					
R _{DS(on)}	Switch ON-resistance	$V_{BUS_CON} = 5 \text{ V}, I_{OUT} = 1 \text{ A}, T_A = 25^{\circ}\text{C}$	_	39	50	mΩ
Digital Signals	3					
V _{IH}	High-level input voltage, #EN	_	1.2	_	_	V
V _{IL}	Low-level input voltage, #EN	_	_		0.7	V
I _{IL}	Input leakage current, #EN	$V_1 = 3.3V$		_	1	μΑ
V_{OL}	Low-level output voltage, #ACK	I _{OL} = 1 mA	_	_	0.4	V
Timing Charac	cteristics					
t _{DELAY}	USB charging turn-on delay	Measured from #EN asserted Low to MOSFET Turn On, excluding soft-start time	_	15	_	ms
t _{SS}	USB charging rise time (soft-start delay)	Measure from V_{BUS_SYS} rises above 25% until #ACK goes Low 10%, R_{LOAD} = 1M Ω and C_{LOAD} = NC	_	18	_	ms
t _{OFF_DELAY}	USB charging turn-off time	Measured from #EN asserted High to V_{BUS_SYS} falling to 10%, R_{LOAD} = 10 Ω and C_{LOAD} =NC	_	4	_	ns
Thermal Prot	tection					
T _{SHDN}	Thermal Shutdown	Junction temperature	_	145		°C
	Thermal Shutdown Hysteresis	Junction temperature	_	35	_	°C

Notes:

- 6. Specifications are over -40°C to +85°C and are guaranteed by characterization and design.7. Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
- 8. Parameters provided for reference only, and do not constitute part of DIODES's published device specifications.
- 9. Excludes soft-start time.



$\textbf{Timing Diagrams} \text{ ($V_{BUS_CON} = 5$V$, $C_{IN} = 1$\muF, $C_{LOAD} = 2.2$\muF, $\#EN = Enable$, $T_{A} = 25°C.$) }$



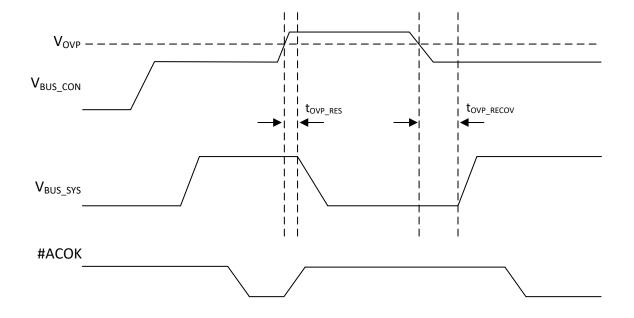
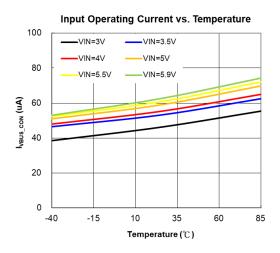
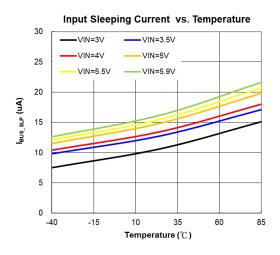


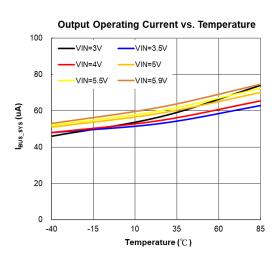
Figure 1. Timing for Power up, Normal operation, OTP and OVP protection

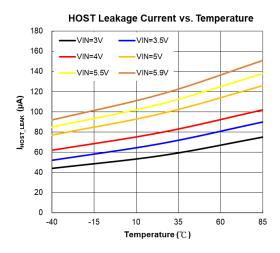


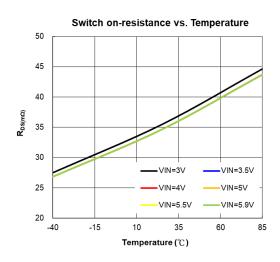
Typical Performance Characteristics ($C_{IN} = 1 \mu F$, $C_{LOAD} = 2.2 \mu F$, unless otherwise specified.)

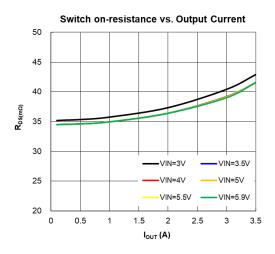






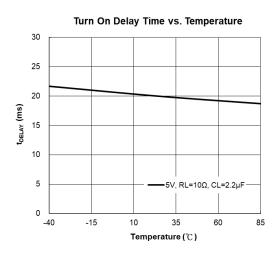


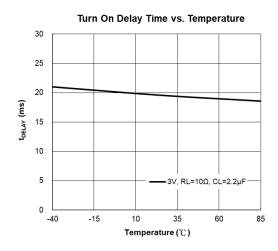


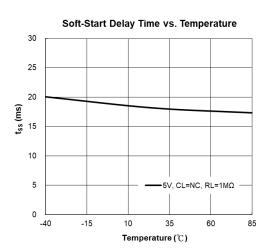


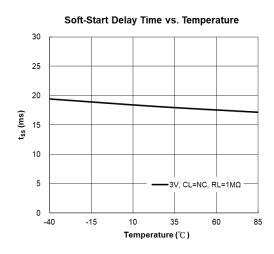


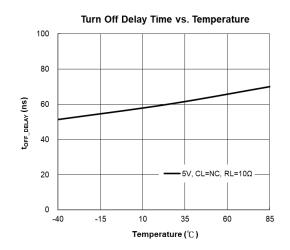
Typical Performance Characteristics ($C_{IN} = 1 \mu F$, $C_{LOAD} = 2.2 \mu F$, unless otherwise specified.)

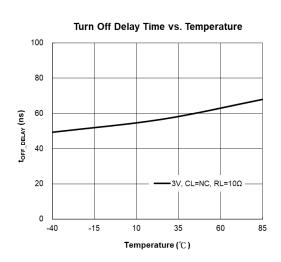








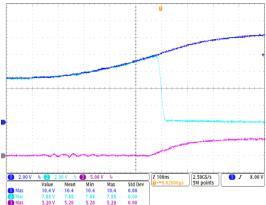






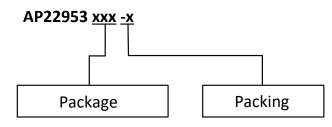
Typical Performance Characteristics ($C_{IN} = 1 \mu F$, $C_{LOAD} = 2.2 \mu F$, unless otherwise specified.)

OVP Response Time CH1 = V_{BUS_CON} , CH2 = V_{BUS_SYS} , CH3 = #ACK V_{BUS_CON} ramp from 5V to 10V





Ordering Information



-7: Tape & Reel CW12: W-WLB2013-12

Dort Number	Posterio Codo	Dooksaina	7" Tape and Reel		
Part Number	Package Code	Packaging	Quantity	Part Number Suffix	
AP22953CW12-7	CW12	W-WLB2013-12	3,000/Tape & Reel	-7	

Marking Information

W-WLB1318-12

(Top View)



XX: Identification Code

Y: Year: 0~9

W: Week: A~Z: 1~26 week; a~z: 27~52 week; z represents

52 and 53 week X: Internal Code

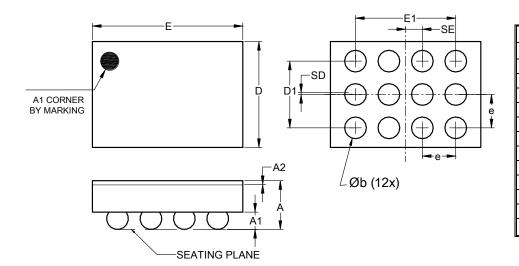
Part Number	Package	Identification Code
AP22953CW12-7	W-WLB2013-12	HW



Package Outline Dimensions

Please see https://www.diodes.com/design/support/packaging/ for the latest version.

(1) Package Type: W-WLB2013-12

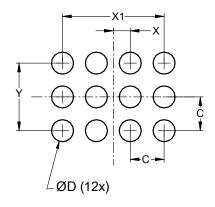


W-WLB2013-12				
Dim	Min	Тур	Max	
Α	0.597	0.64	0.683	
A1	0.182	0.202	0.222	
A2	0.022	0.025	0.028	
D	1.238	1.288	1.338	
Е	1.938	1.988	2.038	
D1	0.750	0.800	0.850	
E1	1.150	1.200	1.250	
b	0.232	0.262	0.292	
е	0.400 BSC			
SD	0.000 BSC			
SE	0.200 BSC			
All Dimensions in mm				

Suggested Pad Layout

Please see https://www.diodes.com/design/support/packaging/ for the latest version.

(1) Package Type: W-WLB1318-12



Dimensions	Value (in mm)	
С	0.400	
D	0.230	
Х	0.200	
X1	1.200	
Υ	0.800	



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