

Description

ZXGD3105N8 synchronous controller is designed for driving a MOSFET as an ideal rectifier. This is to replace a diode for increasing the power transfer efficiency.

Proportional Gate drive control monitors the reverse voltage of the MOSFET such that if body diode conduction occurs a positive voltage is applied to the MOSFET's Gate Pin. Once the positive voltage is applied to the Gate the MOSFET switches on allowing reverse current flow. The controllers' output voltage is then proportional to the MOSFET Drain-Source voltage and this is applied to the Gate via the driver. This action minimizes body diode conduction whilst enabling a rapid MOSFET turn-off as the Drain current decays to zero.

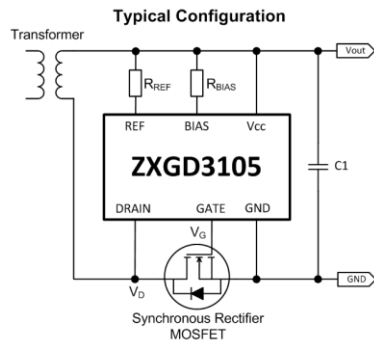
Applications

Flyback Converters in:

- Low Voltage AC- DC Adaptors
- Set-Top-Box
- PoE Power Devices

Resonant Converters in:

- Telecoms PSU
- Laptop Adaptors
- Computing Power Supplies – ATX and Server PSU

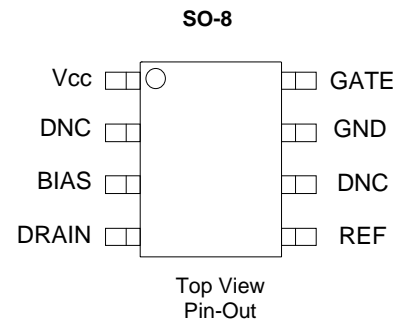


Features

- Proportional Gate Drive to Minimize Body Diode Conduction
- Low Standby Power with Quiescent Supply Current <1mA
- 4.5V Operation Enables Low Voltage Supply
- 25V V_{CC} Rating
- 100V Drain Voltage Rating
- Operation up to 500kHz
- Critical Conduction Mode (CrCM) & Continuous Mode (CCM)
- Compliant with Eco-Design Directive
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.074 grams (Approximate)

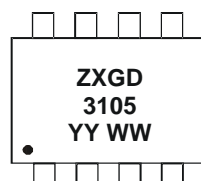


Ordering Information (Note 4)

| Product | Marking | Reel Size (inches) | Tape Width (mm) | Quantity per Reel |
|--------------|----------|--------------------|-----------------|-------------------|
| ZXGD3105N8TC | ZXGD3105 | 13 | 12 | 2,500 |

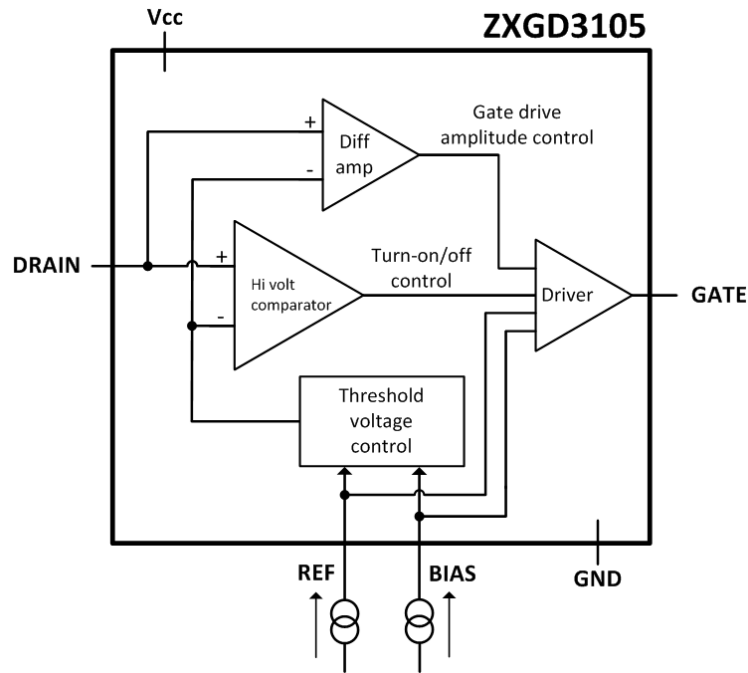
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen and Antimony free, "Green" and Lead-Free.
 3. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



- ZXGD = Product Type Marking Code, Line 1
- 3105 = Product Type Marking Code, Line 2
- YY = Year (ex: 11 = 2011)
- WW = Week (01 - 53)

Functional Block Diagram



| Pin Number | Pin Name | Description |
|------------|-----------------|--|
| 1 | V _{CC} | Power Supply This supply pin should be closely decoupled to ground with a ceramic capacitor. |
| 2 | DNC | Do Not Connect Leave pin floating. |
| 3 | BIAS | Bias Connect this pin to V _{CC} via R _{BIAS} resistor. Select R _{BIAS} to source 0.54mA into this pin. Refer to Table 1 and 2, in Application Information section. |
| 4 | DRAIN | Drain Sense Connect directly to the synchronous MOSFET drain terminal. |
| 5 | REF | Reference Connect this pin to V _{CC} via R _{REF} resistor. Select R _{REF} to source 1.02mA into this pin. Refer to Table 1 and 2, in Application Information section. |
| 6 | DNC | Do Not Connect Leave pin floating. |
| 7 | GND | Ground Connect this pin to the synchronous MOSFET source terminal and ground reference point. |
| 8 | GATE | Gate Drive This pin sinks and sources the I _{SINK} and I _{SOURCE} current to the synchronous MOSFET gate. |

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

| Characteristic | Symbol | Value | Unit |
|---------------------------------|--------------|--------------------|------|
| Supply Voltage, Relative to GND | V_{CC} | 25 | V |
| Drain Pin Voltage | V_D | -3 to +100 | V |
| Gate output Voltage | V_G | -3 to $V_{CC} + 3$ | V |
| Gate Driver Peak Source Current | I_{SOURCE} | 4 | A |
| Gate Driver Peak Sink Current | I_{SINK} | 9 | A |
| Reference Voltage | V_{REF} | V_{CC} | V |
| Reference Current | I_{REF} | 25 | mA |
| Bias Voltage | V_{BIAS} | V_{CC} | V |
| Bias Current | I_{BIAS} | 100 | mA |

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

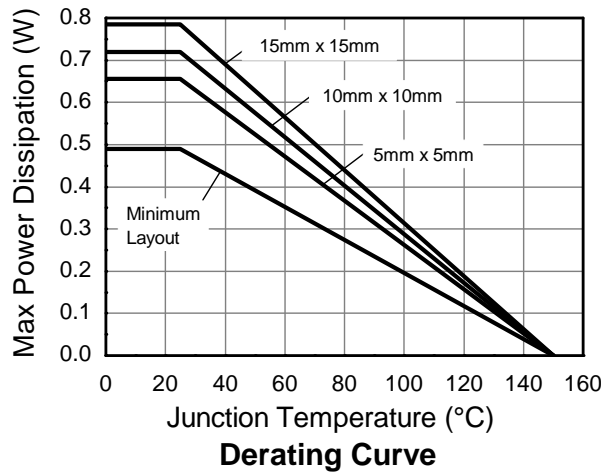
| Characteristic | Symbol | Value | Unit |
|---|-----------------|-------------|----------------------------|
| Power Dissipation Linear Derating Factor | P_D | 490 | mW mW/ $^\circ\text{C}$ |
| | | 3.92 | |
| | | 655 | |
| | | 5.24 | |
| | | 720 | |
| | | 5.76 | |
| | | 785 | |
| | | 6.28 | |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 255 | $^\circ\text{C/W}$ |
| | | 191 | |
| | | 173 | |
| | | 159 | |
| Thermal Resistance, Junction to Lead | $R_{\theta JL}$ | 55 | $^\circ\text{C/W}$ |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 45 | $^\circ\text{C/W}$ |
| Operating Temperature Range | T_J | -40 to +150 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{STG} | -55 to +150 | |

ESD Ratings (Note 11)

| Characteristic | Symbol | Value | Unit | JEDEC Class |
|--|---------|-------|------|-------------|
| Electrostatic Discharge - Human Body Model | ESD HBM | 4,000 | V | 3A |
| Electrostatic Discharge - Machine Model | ESD MM | 200 | V | B |

- Notes:
- For a device surface mounted on minimum recommended pad layout FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 - Same as Note (5), except pin 1 (V_{CC}) and pin 7 (GND) are both connected to separate 5mm x 5mm 1oz copper heatsinks.
 - Same as Note (6), except both heatsinks are 10mm x 10mm.
 - Same as Note (6), except both heatsinks are 15mm x 15mm.
 - Thermal resistance from junction to solder-point at the end of each lead on Pin 1 (V_{CC}) or Pin 7 (GND).
 - Thermal resistance from junction to top of the case.
 - Refer to JEDEC specification JESD22-A114 and JESD22-A115.

Thermal Derating Curve

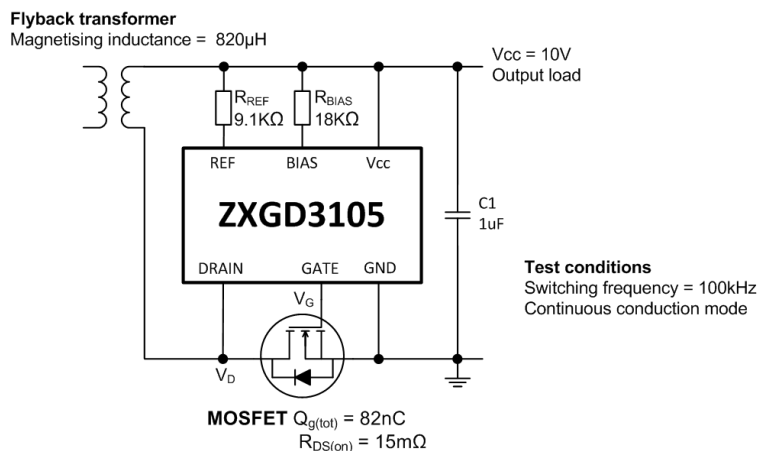


Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

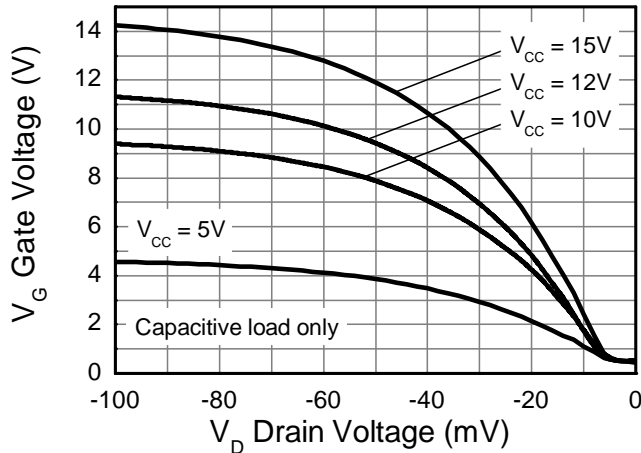
V_{CC} = 10V; R_{BIAS} = 18kΩ (I_{BIAS} = 0.54mA); R_{REF} = 9.1kΩ (I_{REF} = 1.02mA)

| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|------------------------------------|----------------------|-----|------|-----|------|---|
| Input Supply | | | | | | |
| Quiescent Current | I _Q | — | 1.56 | — | mA | V _{DRAIN} ≥ 0mV |
| Gate Driver | | | | | | |
| Gate Peak Source Current | I _{SOURCE} | — | 1.2 | — | A | Capacitive Load: C _L = 10nF |
| Gate Peak Sink Current | I _{SINK} | — | 5 | — | | |
| Detector under DC condition | | | | | | |
| Turn-Off Threshold Voltage | V _T | -20 | -10 | 0 | mV | V _G = 1V |
| Gate Output Voltage | V _{G(off)} | — | 0.2 | 0.6 | V | V _{DRAIN} ≥ 1V |
| | V _G | 5.0 | 7.8 | — | | V _{DRAIN} = -50mV |
| | | 8.0 | 9.4 | — | | V _{DRAIN} = -100mV |
| Switching Performance | | | | | | |
| Turn-On Propagation Delay | t _{d(rise)} | — | 118 | — | nS | Capacitive Load: C _L = 10nF Rise and Fall Measured 10% to 90% |
| Gate Rise Time | t _r | — | 77 | — | | |
| Turn-Off Propagation Delay | t _{d(fall)} | — | 14 | — | | |
| Gate Fall Time | t _f | — | 26 | — | | |

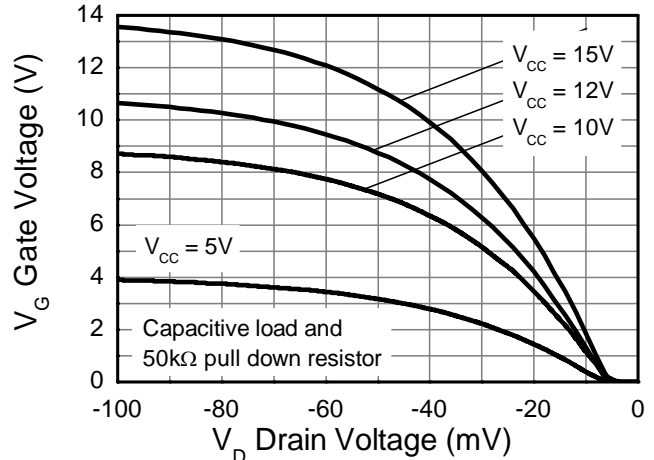
Test Circuit for Switching Performance



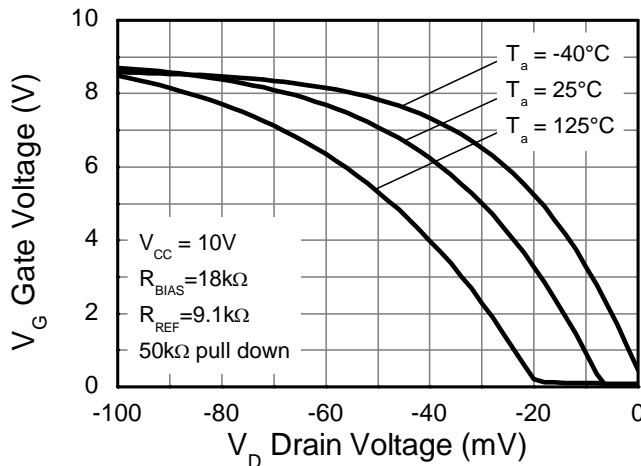
Typical Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)



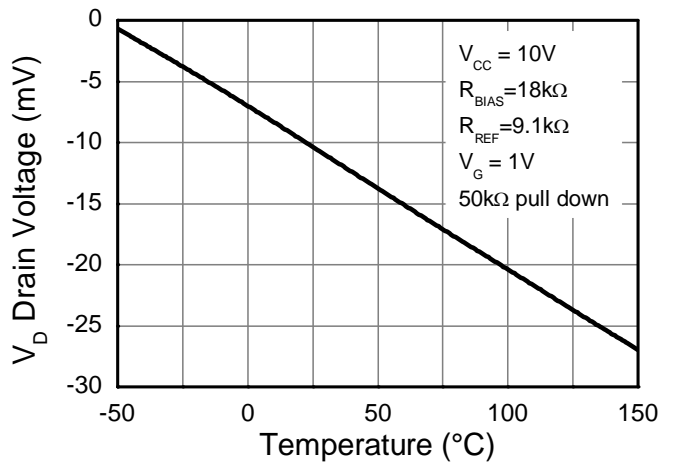
Transfer Characteristic



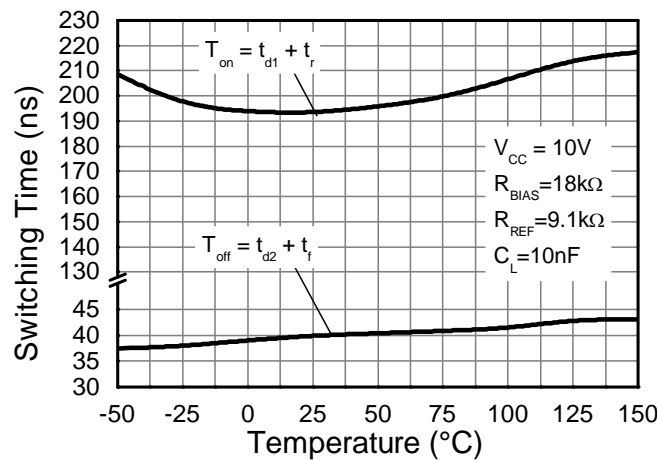
Transfer Characteristic



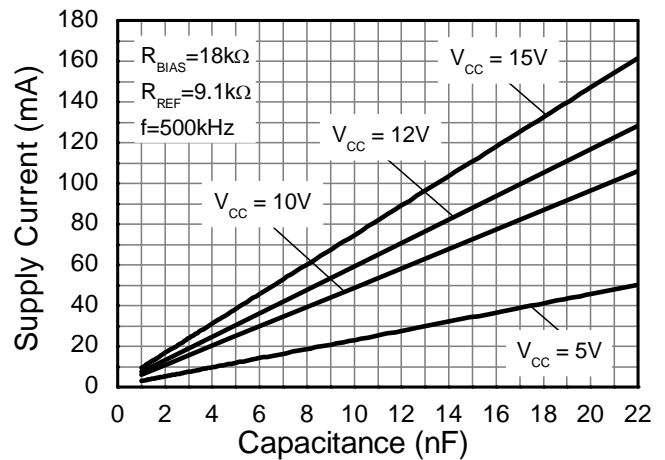
Transfer Characteristic



Drain Sense Voltage vs Temperature

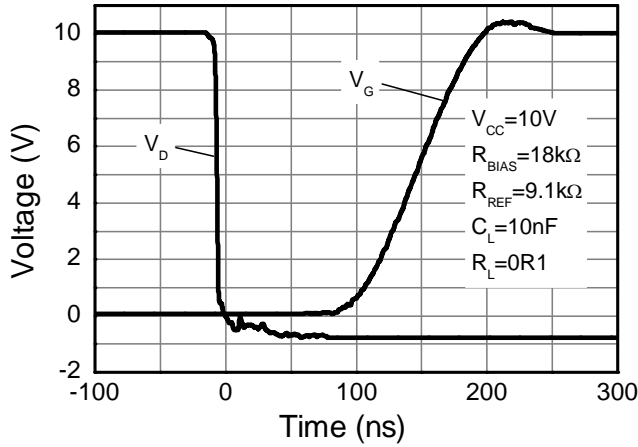


Switching vs Temperature

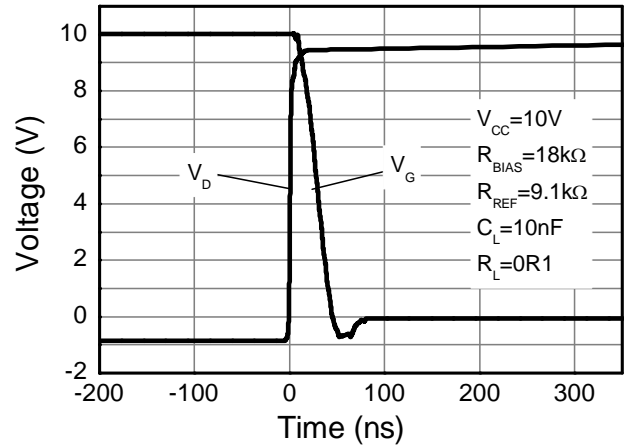


Supply Current vs Capacitive Load

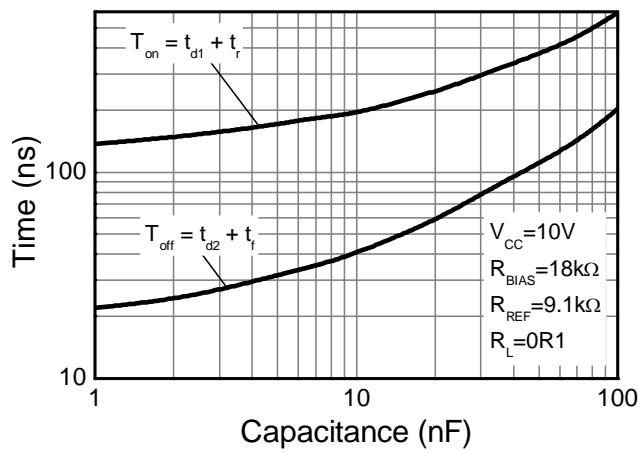
Typical Electrical Characteristics (Continued) (@T_A = +25°C, unless otherwise specified.)



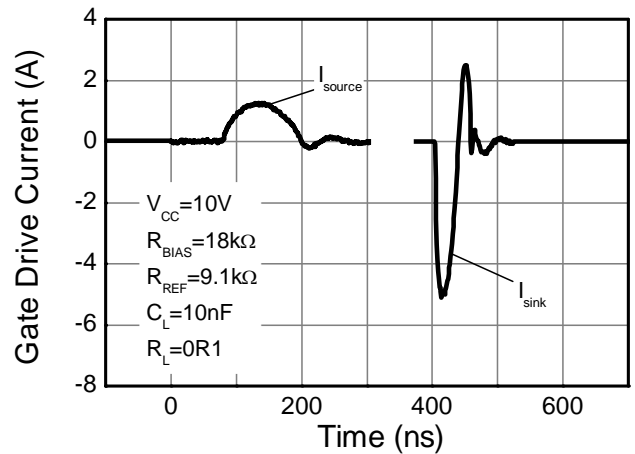
Switch On Speed



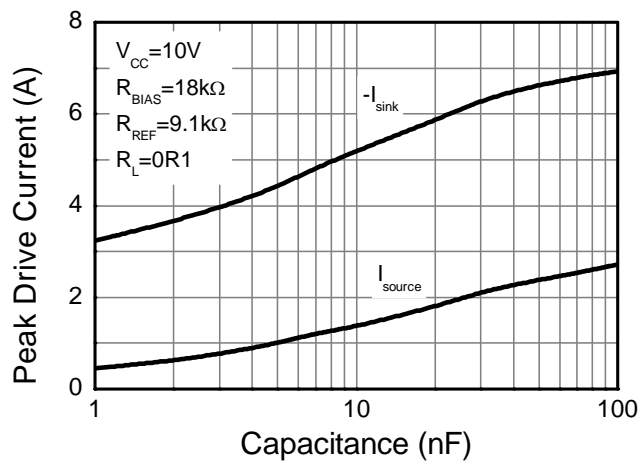
Switch Off Speed



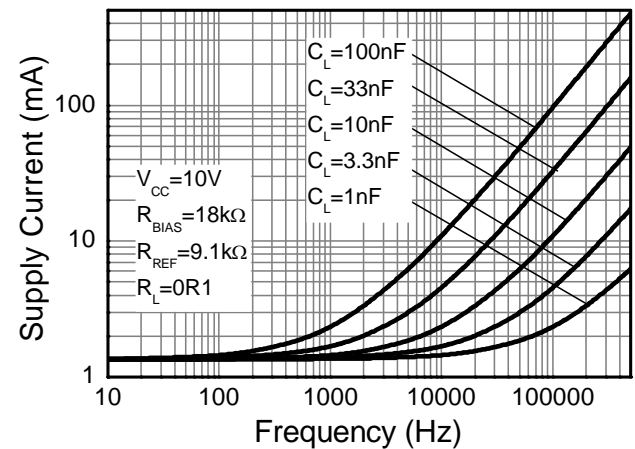
Switching vs Capacitive Load



Gate Drive Current



Gate Current vs Capacitive Load



Supply Current vs Frequency

Application Information

The purpose of the ZXGD3105 is to drive a MOSFET as a low V_F Schottky diode replacement in isolated AC-DC converter. When combined with a low $R_{DS(ON)}$ MOSFET, the controller can yield significant power efficiency improvement, whilst maintaining design simplicity and incurring minimal component count. Figure 1 shows the typical configuration of ZXGD3105 for synchronous rectification in a low output voltage flyback converter.

A typical circuit configuration of synchronous rectification with ZXGD3105 for use in resonant converter is shown in Figure 2. Two ZXGD3105 together with two synchronous MOSFETs should be used on the secondary side of the center tapped transformer winding.

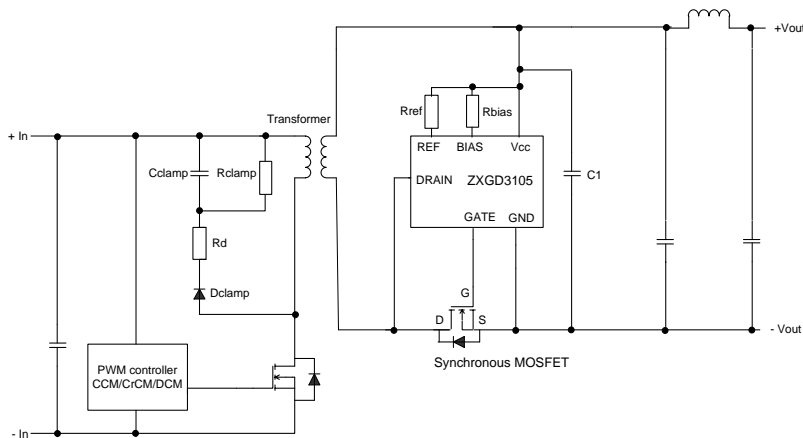


Figure 1 Typical Flyback Application Schematic

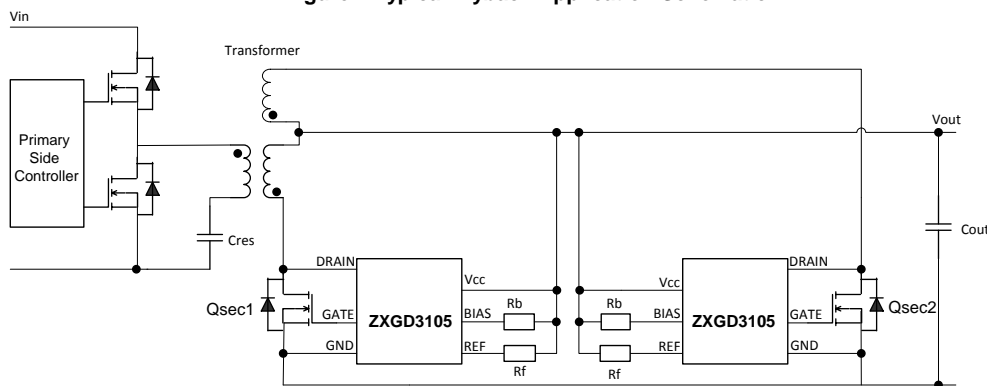


Figure 2 Synchronous Rectification in Resonant Converter

Threshold Voltage and Resistor Setting

The correct selection of external resistors R_{REF} and R_{BIAS} is important for optimum device operation. R_{REF} and R_{BIAS} supply fixed current into the I_{REF} and I_{BIAS} Pin of the controller. I_{REF} and I_{BIAS} combines to set the turn-off threshold voltage level, V_T . In order to set V_T to -10mV, the recommended I_{REF} and I_{BIAS} are 1.02mA and 0.54mA respectively.

The values for R_{REF} and R_{BIAS} are selected based on the V_{CC} voltage. If the V_{CC} Pin is connected to the power converter's output, the resistors should be selected based on the nominal converter's output voltage. Table 1 provides the recommended resistor values for different V_{CC} voltages.

| Supply, V_{CC} (V) | Bias Resistor, R_{BIAS} (k Ω) | Reference Resistor, R_{REF} (k Ω) |
|-------------------------|--|--|
| 5 | 9.6 | 4.3 |
| 10 | 18 | 9.1 |
| 12 | 24 | 11 |
| 15 | 30 | 15 |

Table 1 Recommended Resistor Values for Different V_{CC} Voltages

Application Information (Continued)

Functional Descriptions for Flyback Converter

The operation of the device is described step-by-step with reference to the timing diagram in Figure 3.

1. The detector stage monitors the MOSFET Drain-Source voltage.
2. When, due to transformer action, the MOSFET body diode is forced to conduct there is a negative voltage on the Drain Pin due to the body diode forward voltage.
3. As the negative Drain voltage crosses the turn-off threshold voltage (V_T), the detector stage outputs a positive voltage with respect to Ground after the turn-on delay time ($t_{d(fall)}$). This voltage is then fed to the MOSFET driver stage and current is sourced out of the Gate Pin.
4. The controller goes into proportional Gate drive control – the Gate output voltage is proportional to the MOSFET on-resistance-induced Drain-Source voltage. Proportional gate drive control ensures that the MOSFET conducts during the majority of the conduction cycle to minimize power loss in the body diode.
5. As the Drain current decays linearly toward zero, proportional gate drive control reduces the Gate voltage so the MOSFET can be turned off rapidly at zero current crossing. The Gate voltage falls to 1V when the Drain-Source voltage crosses the detection threshold voltage to minimize reverse current flow.
6. At zero Drain current, the controller Gate output voltage is pulled low to $V_{G(off)}$ to ensure that the MOSFET is off.

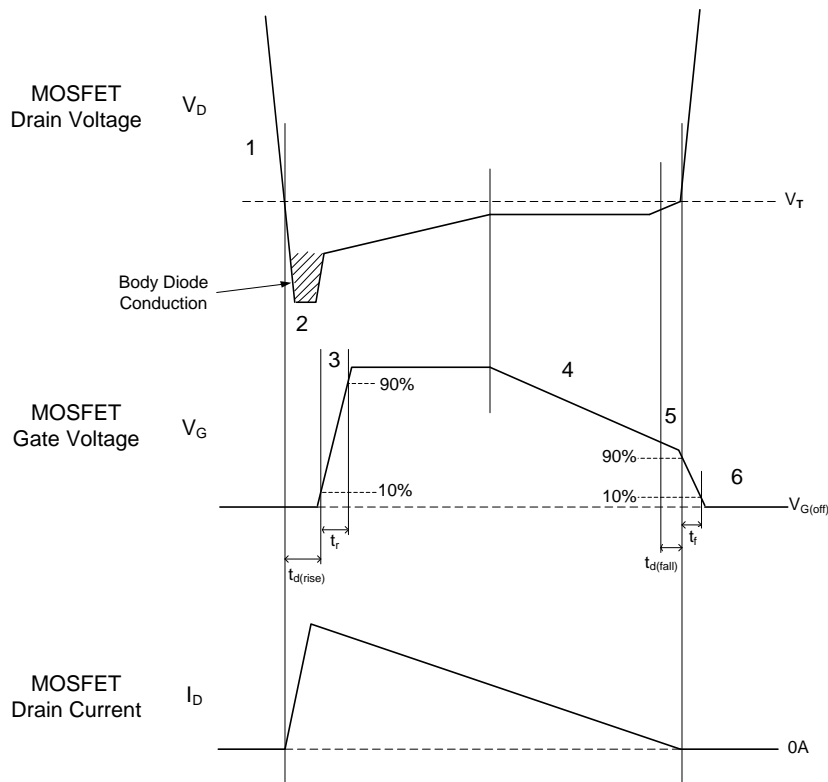


Figure 3 Timing Diagram for a Critical Conduction Mode Flyback Converter

Application Information (Cont.)

Functional Descriptions for Resonant Converter

The operation of the ZXGD3105 in resonant converter is described with reference to Figure 4.

1. The detector stage monitors the MOSFET Drain-GND voltage.
2. When the MOSFET body diode is forced to conduct, due to transformer action, there is a negative voltage on the Drain Pin due to the body diode forward voltage.
3. As the negative Drain voltage crosses the threshold voltage (V_T), the detector stage outputs a positive voltage with respect to Ground after the turn-on delay time ($t_{d(rise)}$). This voltage is then fed to the MOSFET driver stage and current is sourced out of the Gate pin.
4. The controller goes into proportional Gate drive control. The Gate voltage now varies according to the MOSFET's Drain-GND voltage. During this phase, the relationship of V_G vs. V_D is shown by the Transfer Characteristic Graph on Page 5 of this datasheet. As the Drain current decays linearly, the Gate voltage reduces so the MOSFET can be turned off rapidly at zero current crossing.

Proportional Gate drive control also ensures that the Gate voltage is supplied to the MOSFET Gate until the Drain current is virtually zero. This eliminates any parasitic diode conduction after the MOSFET switches off.

5. The Gate voltage falls to 1V when the Drain-GND voltage reaches V_T . The MOSFET is turned off precisely when the sinusoidal current goes to zero, with little or no reverse current. Threshold voltage (V_T) is defined as the Drain voltage V_D level, at which the Gate voltage V_G is 1V (refer to Electrical Characteristics Table on Page 4).
6. At zero Drain current, the Gate voltage is pulled low to $V_{G(off)}$ to ensure that the MOSFET is off.

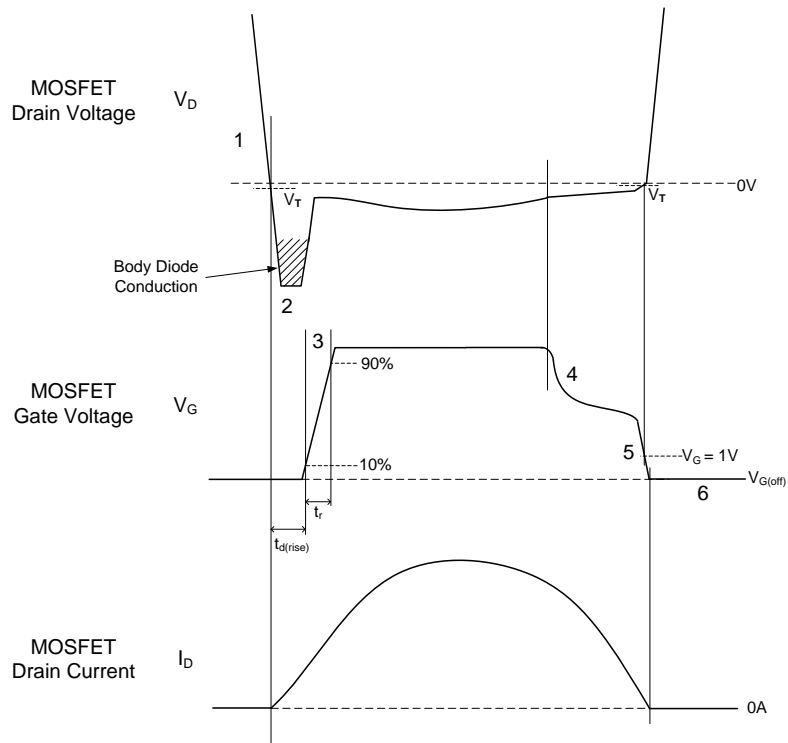


Figure 4 Timing Diagram of Synchronous Rectification in the Resonant Converter

Application Information (Cont.)

Besides that, Proportional Gate drive control improves the rectifier efficiency even at light to medium load condition by ensuring that the MOSFETs conduct during majority of the conduction cycle as shown in Figure 5a.

At reduced load condition, early termination of the Gate drive voltage is likely for digital-level Gate drive due to the low current, which means that the threshold V_T is breached. With the early termination of the Gate drive voltage, the MOSFET turns off and the body diode conducts, see Figure 5. This is shown by an increase in Drain-GND voltage for the remaining time of the current waveform. With the current flowing through the body diode there will be an increase in power developed within the MOSFET. The efficiency impact due to early termination of digital-level Gate driver increases with lower $R_{DS(ON)}$ MOSFET and/or higher operating frequency.

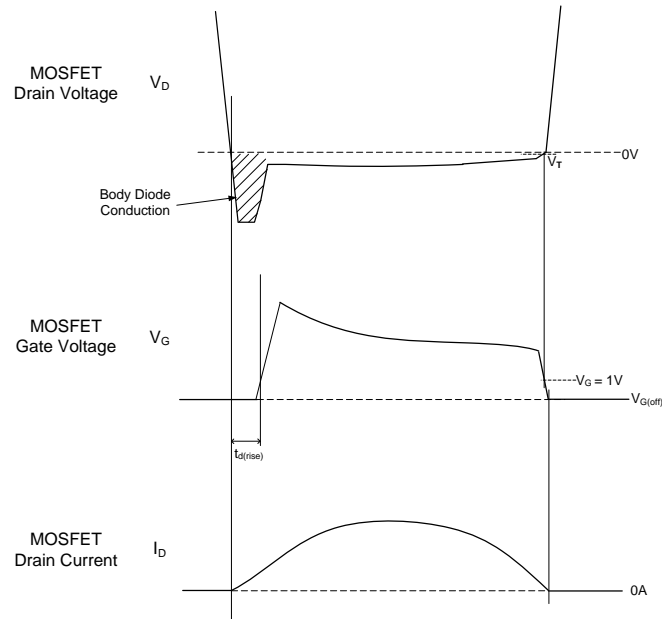
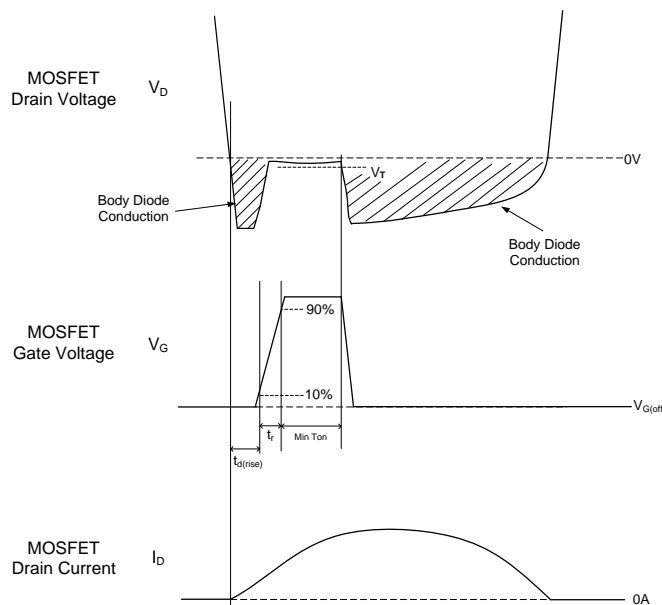


Figure 5 Timing Diagram of Synchronous Rectification in the Resonant Converter (a) Proportional Gate Drive



(b) Digital-Level Gate Drive

Application Information (Cont.)

Layout Guidelines

When laying out the PCB, care must be taken in decoupling the ZXGD3105 closely to V_{CC} and Ground with 1μF low-ESR, low-ESL X7R type ceramic bypass capacitor. If the converter's output voltage is higher than 20V, a 12V zener diode should be connected from the Bias Pin to GND to clamp the Gate voltage and protect the synchronous MOSFET. Figure 7 shows the Typical Connection Diagram.

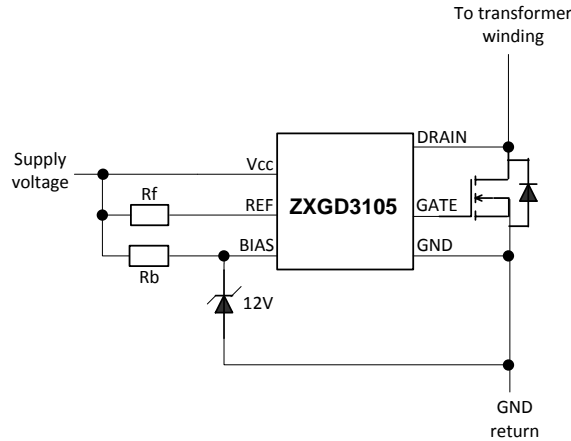


Figure 7 Zener Voltage Clamp Arrangement

GND is the Ground reference for the internal high voltage amplifier as well as the current return for the Gate driver. So the Ground return loop should be as short as possible. Sufficient PCB copper area should be allocated to the V_{CC} and GND Pin for heat dissipation especially for high switching frequency application.

Any stray inductance involved by the load current may cause distortion of the Drain-to-Source voltage waveform, leading to premature turn-off of the synchronous MOSFET. In order to avoid this issue, Drain voltage sensing should be done as physically close to the Drain terminals as possible. The PCB track length between the controller Drain Pin and the MOSFET's terminal should be kept less than 10mm. MOSFET packages with low internal wire bond inductance are preferred for high switching frequency power conversion to minimize body diode conduction.

After the primary MOSFET turns off, its Drain voltage oscillates due to reverse recovery of the snubber diode. These high frequency oscillations are reflected across the transformer to the Drain terminal of the synchronous MOSFET. The synchronous controller senses the Drain voltage ringing, causing its Gate output voltage to oscillate. The synchronous MOSFET cannot be fully enhanced until the Drain voltage stabilizes.

In order to prevent this issue, the oscillations on the primary MOSFET can be damped with either a series resistor R_D to the snubber diode or an R-C network across the diode (refer to Figure 8). Both methods reduce the oscillations by softening the snubber diode's reverse recovery characteristic.

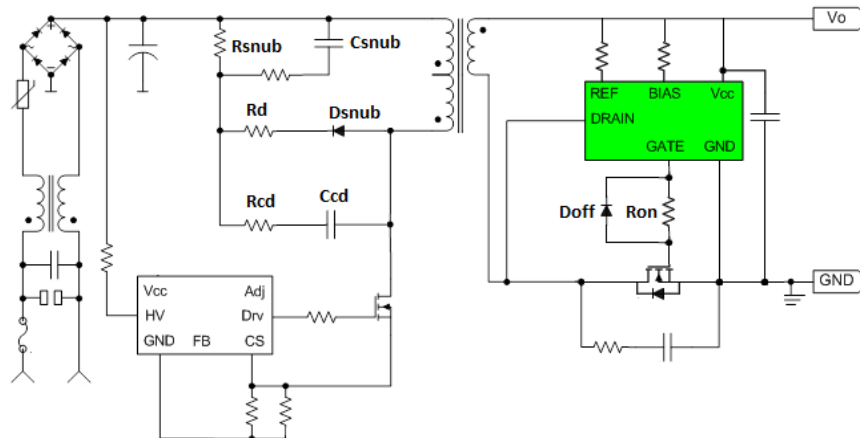
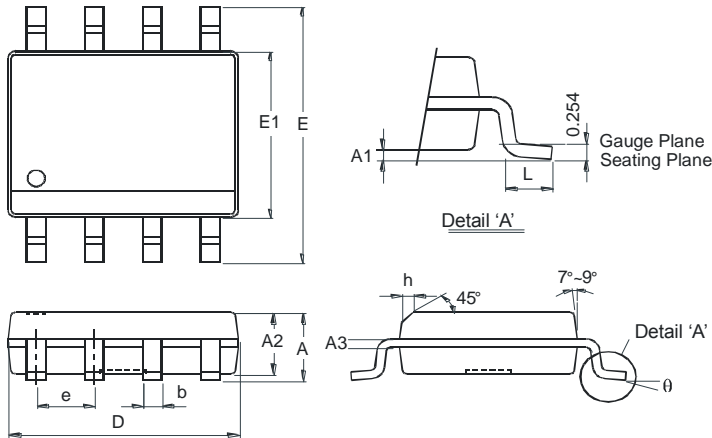


Figure 8 Primary Side Snubber Network to Reduce Drain Voltage Oscillations

Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.

SO-8

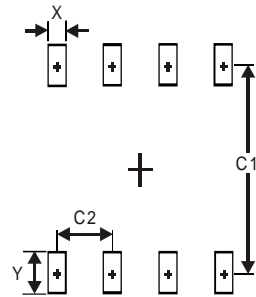


| SO-8 | | |
|-----------------------------|----------|------|
| Dim | Min | Max |
| A | – | 1.75 |
| A1 | 0.10 | 0.20 |
| A2 | 1.30 | 1.50 |
| A3 | 0.15 | 0.25 |
| b | 0.3 | 0.5 |
| D | 4.85 | 4.95 |
| E | 5.90 | 6.10 |
| E1 | 3.85 | 3.95 |
| e | 1.27 Typ | |
| h | – | 0.35 |
| L | 0.62 | 0.82 |
| θ | 0° | 8° |
| All Dimensions in mm | | |

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

SO-8



| Dimensions | Value (in mm) |
|------------|---------------|
| X | 0.60 |
| Y | 1.55 |
| C1 | 5.4 |
| C2 | 1.27 |

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