

UNIDIRECTIONAL ESD PROTECTION DIODE

STAND-OFF VOLTAGE- **5.0** Volts POWER DISSIPATION - **25** WATTS

GENERAL DESCRIPTION

 The L02ESD5V0F6-5 is a low capacitance 5-fold ESD array in the ultra small SOT666 plastic package designed to protect up to five transmission or data lines from the damage caused by Electrostatic Discharge(ESD).

FEATURES

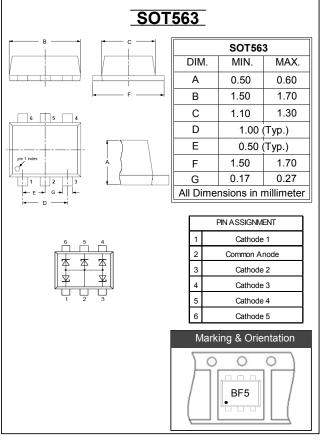
- Uni-directional ESD protection of up to five lines.
- Bi-directional ESD protection of up to four lines.
- Max.peak pulse power: Ppp = 25W at tp = 8/20 us
- ESD protection > 20 KV
- IEC 61000-4-2, level 4 (ESD), > 15KV (air); > 8KV (contact).
- IEC 61000-4-5 (surge); Ipp = 2.5A at tp = 8/20 us.
- Low clamping voltage; Vcl < 12V at Ipp = 2.5A
- Low capacitance device.

APPLICATION

- Computers and peripherals.
- · Communication system.
- · Cellular handsets and accessories.
- Audio & video equipment.
- Portable electronics.

MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/EC



MAXIMUM RATINGS (Tj= 25°C unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak pulse Power (8/20us Waveform) notes 1 and 2	РРРМ	25	W
Operating Junction Temperature Range	TJ	-55 to + 150	°
Storage Temperature Range	Tstg	-55 to + 150	ပ္
Soldering Temperature, t max = 10s	TL	260	${\mathbb C}$

NOTE;1.Non-repetitive current pulse 8/20 us exponentially decaying waveform.

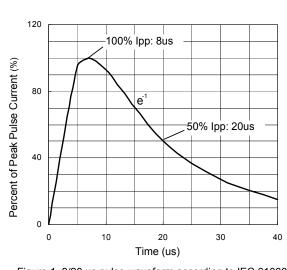
2. Measured from any of pins 1,3,4,5 or 6 to pin2.

ELECTRICAL CHARACTERISTICS (Tj= 25°C unless otherwise noticed)

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Parameter	Symbol	Conditions	MIn	Max	Unit			
Reverse standoff voltage	VDRM			5.0	V			
Reverse leakage current	IRM	V _{DRM} = 5 V		25	nA			
Breakdown voltage	VBR	IR = 1 mA	6.4	7.2	V			
Diode capacitance	CJ	VR = 0 V , f = 1MHz		19	pF			
Clamping voltage	VCL	IPP = 1A		10	V			
Clamping voltage	VcL	IPP = 2.5A		12	V			

REV. 2, Oct-2010, KSIR12





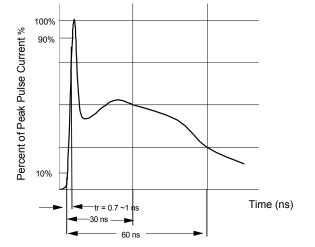
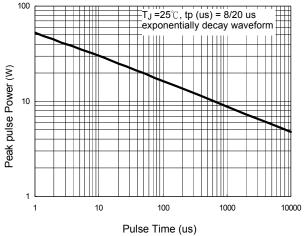


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

Figure 2. ESD pulse waveform according to IEC 61000-4-2



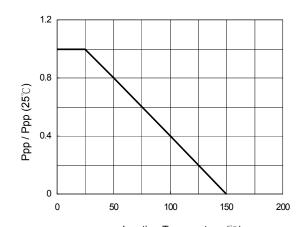
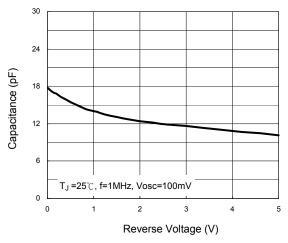


Figure 3. Power Dissipation versus Pulse Time

Junction Temperature ($^{\circ}$ C) Figure 4. Peak pulse power versus TJ



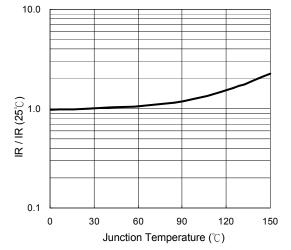


Figure 5. Typical Junction Capactiance

Figure 6. Reverse Leakage Current versus TJ



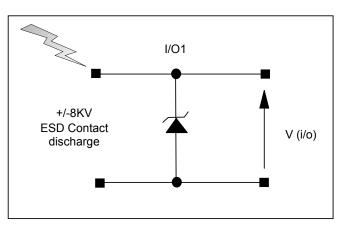


Figure 7. ESD Test Configuration

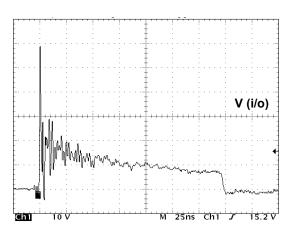


Figure 8. Clamped +8 kV ESD voltage waveform

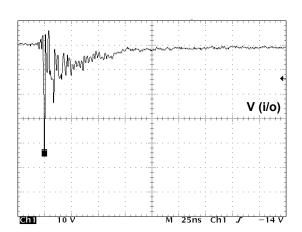


Figure 9. Clamped -8 kV ESD voltage waveform



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