Features

- Very Low Dropout Voltage
- Low Current Consumption: Typ. 50µA
- Output Voltage: 3.3V
- Guaranteed 600mA (min) Output
- Input Range up to 5.5V
- Current Limiting
- Stability with Low ESR Capacitors
- Thermal shutdown Protection
- Low Temperature Coefficient
- SOP-8L and SOP-8L-EP: Available in “Green” Molding Compound (No Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

General Description

The AP7217A low-dropout linear regulator operates from a 3.3V to 5.5V supply and delivers a guaranteed 600mA (min) continuous load current.

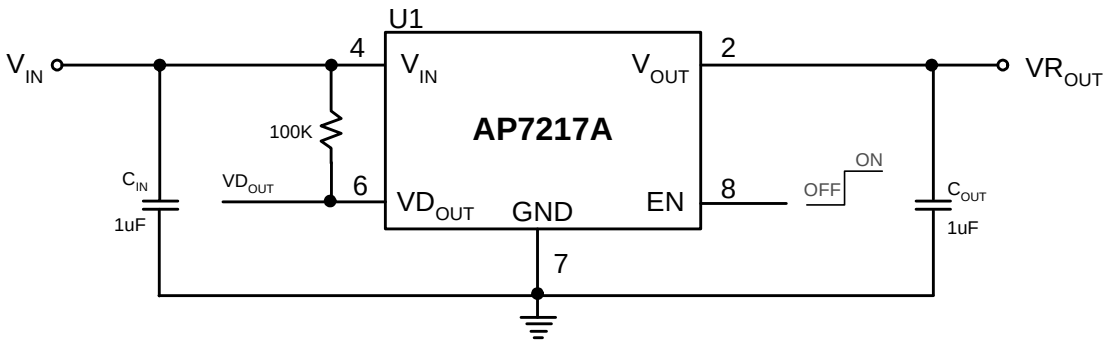
The high-accuracy output voltage is preset to an internally trimmed voltage. An active-low open-drain reset output remains asserted for at least 200ms (TYP) after output voltage reaches regulation.

The space-saving SOP-8L and SOP-8L-EP packages are suitable for “pocket” and hand-held application.

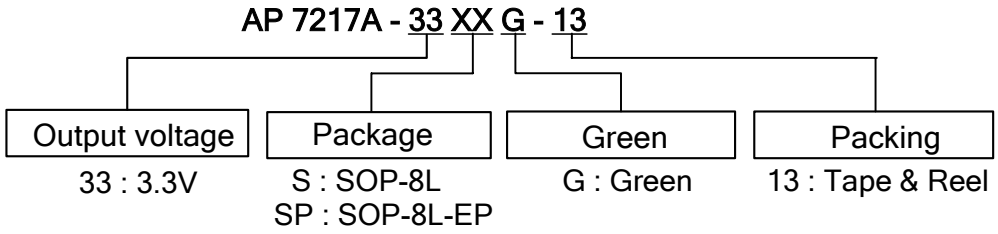
Applications

- HD/ Blue Ray DVD & MP3/4 Players
- CD and MP3 Players
- Cellular and PCS Phones
- Digital Still Camera
- Hand-Held Computers

Typical Application Circuit



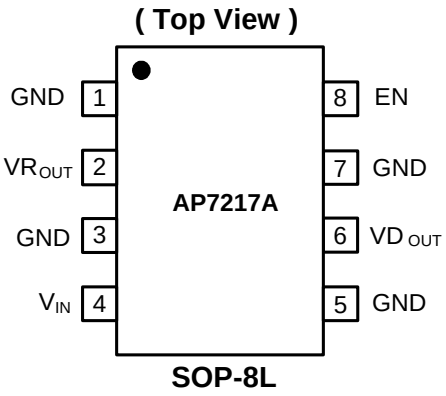
Ordering Information

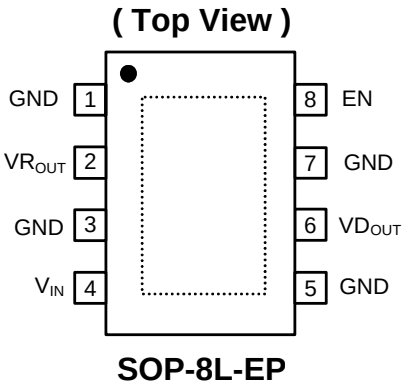


Device	Package Code	Packaging (Note 2)	13" Tape and Reel	
			Quantity	Part Number Suffix
AP7217A-33SG-13	S	SOP-8L	2500/Tape & Reel	-13
AP7217A-33SPG-13	SP	SOP-8L-EP	2500/Tape & Reel	-13

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.
2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

Pin Assignments

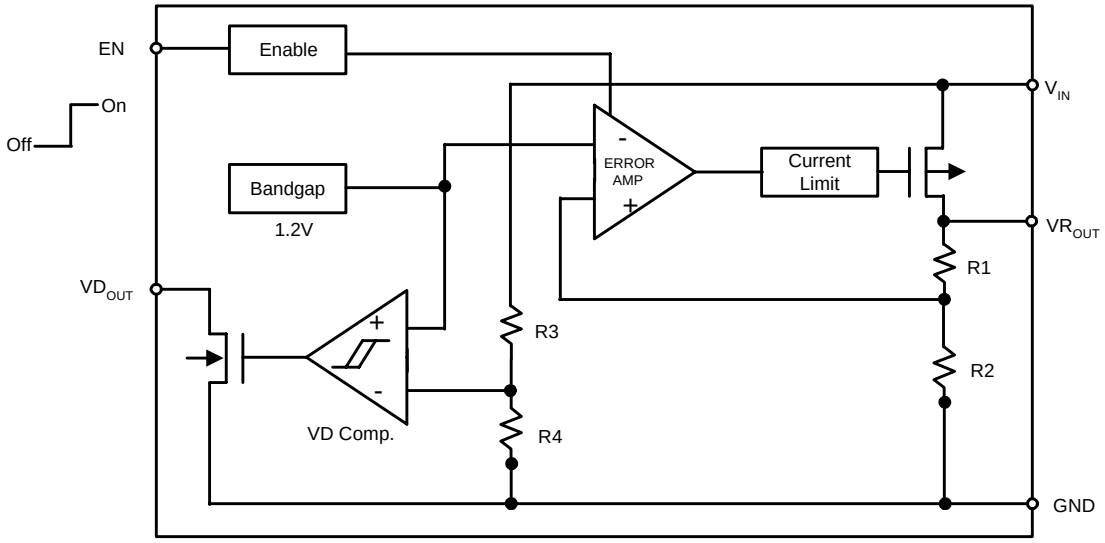




Pin Descriptions

Pin Name	Pin No.	Description
GND	1, 3, 5, 7	Ground
VR_{OUT}	2	Voltage Output
V_{IN}	4	Supply Voltage
VD_{OUT}	6	V_D Output (Reset on I/P)
EN	8	Enable (V_R On/Off)

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
ESD HBM	Human Body Model ESD Protection		3.5	KV
ESD MM	Machine Model ESD Protection		500	V
V_{IN}	Input Voltage		+6	V
I_{OUT}	Output Current		$P_D/ (V_{IN}-V_O)$	mA
VR_{OUT}	Output Voltage		GND - 0.3 ~ V_{IN}+ 0.3	V
P_D	Power Dissipation	SOP-8L	1010	mW
		SOP-8L-EP	1650	
T_J	Operating Junction Temperature Range		-40 to +125	ºC

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	3.3	5.5	V
I_{OUT}	Output Current	0	600	mA
T_A	Operating Ambient Temperature	-40	85	ºC

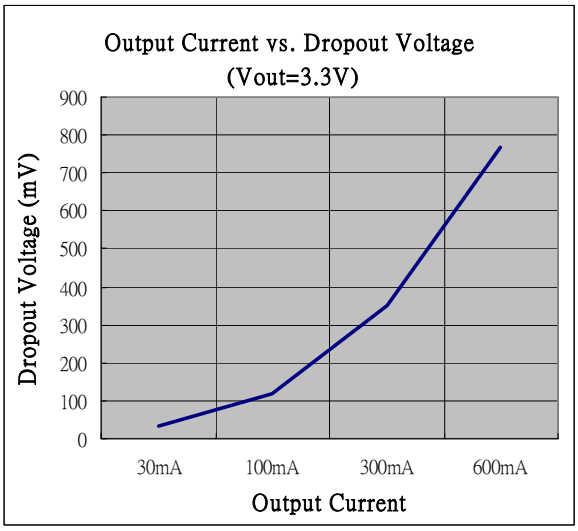
Electrical Characteristics

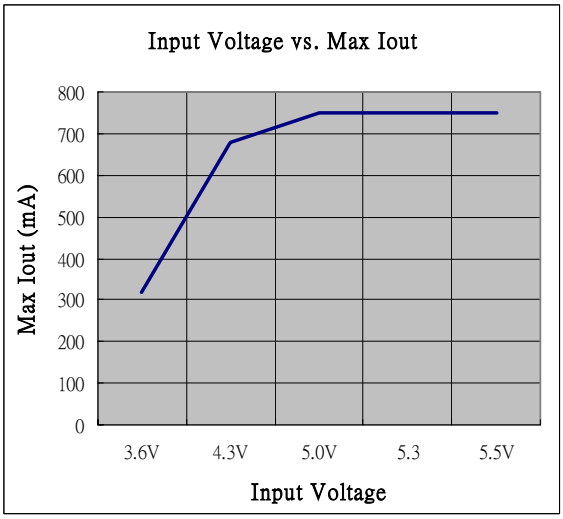
(T_A = 25°C, C_{IN} = 1µF, C_{OUT} = 1µF, V_{EN} = V_{IN}, unless otherwise noted)

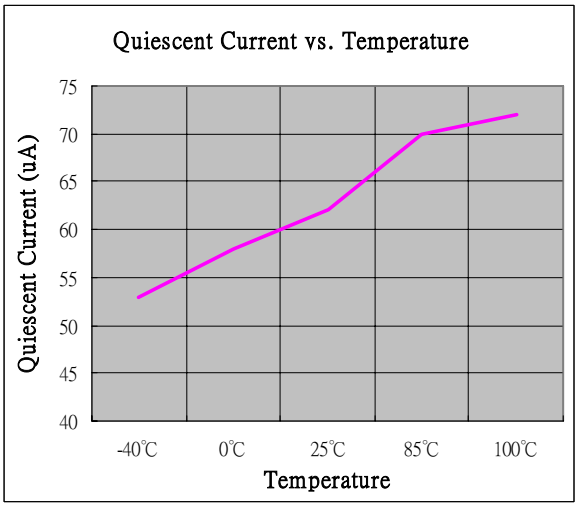
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_Q	Quiescent Current	I_O = 0mA	-	50	80	µA
I_{STB}	Standby Current	V_{EN} = Off V_{IN} = 5.0V		15	25	µA
VR_{OUT}	Output Voltage Accuracy	I_O = 30mA, V_{IN} = 5V	3.234	3.300	3.366	V
	V_{OUT} Temperature Coefficient	-40°C to 85°C, I_{OUT} = 30mA		±100		ppm / °C
$V_{DROPOUT}$	Dropout Voltage	I_{OUT} = 300mA		350	400	mV
		I_{OUT} = 600mA		800	900	
I_{OUT}	Maximum Output Current	V_{IN} = 5.3V	600			mA
I_{LIMIT}	Current Limit	V_{IN} = 5.3V		750		mA
I_{short}	Short Circuit Current	V_{IN} = 5.3V		50		mA
$\Delta V_{LINE}/\Delta V_{IN}/V_{OUT}$	Line Regulation	4.3V ≤ V_{IN} ≤ 5.5V; I_{OUT} = 30mA		0.01	±0.2	%/V
ΔV_{OUT}	Load Regulation	1mA ≤ I_{OUT} ≤ 100mA, V_{IN} = 5.3V		15	50	mV
PSRR	Power Supply Rejection	V_{IN} = 4.3V+ 0.5Vp-pAC, I_{OUT} = 50mA, F = 1KHz		55		dB
V_{EH}	EN Input Threshold	Output ON	1.6			V
V_{EL}		Output OFF			0.25	V
I_{EN}	Enable Pin Current		-0.1		0.1	µA
V_{DF}	Detect fall voltage		3.23	3.3	3.37	V
V_D Hysteresis Range	$V_{Hysteresis}$		V_{DF} x1.02	V_{DF} x1.05	V_{DF} x1.08	V
I_{VDout}	VD Supply Current	VDout = 0.5V V_{IN} = 2.0V 3.0V		20 30		mA
t_{RP}	V_{DOUT} Delay Time	V_{IN} = 1.8V to VDF+ 1V	180	200	-	mSec
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOP-8L (Note 3)		134		°C/W
		SOP-8L-EP (Note 4)		82		
θ_{JC}	Thermal Resistance Junction-to-Case	SOP-8L (Note 3)		28		°C/W
		SOP-8L-EP (Note 4)		12		

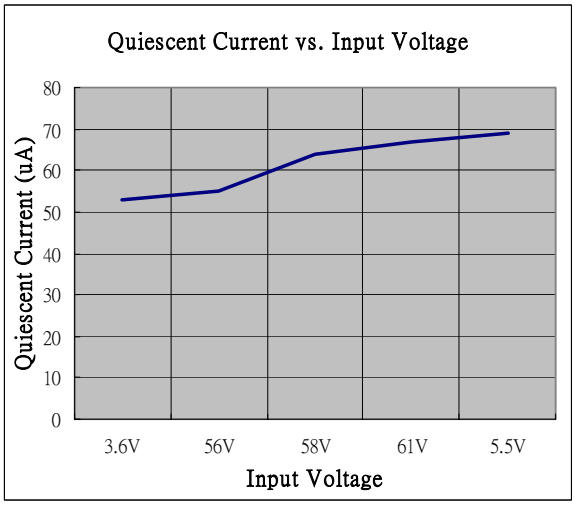
Notes: 3. Test condition for SOP-8L: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
4. Test condition for SOP-8L-EP: Device mounted on 2oz copper, minimum recommended pad layout on top & bottom layer with thermal vias, double sided FR-4 PCB.

Typical Performance Characteristics

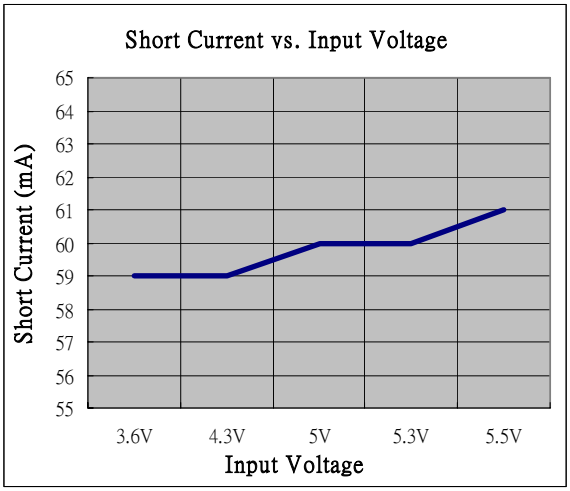


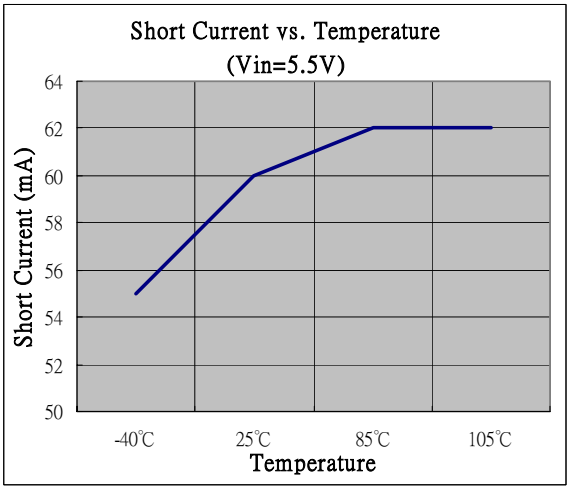


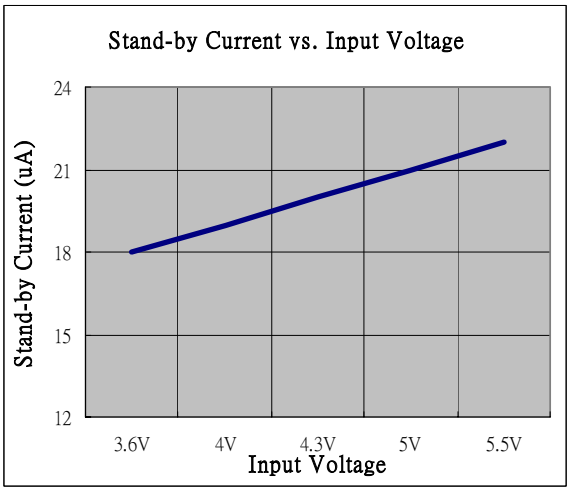


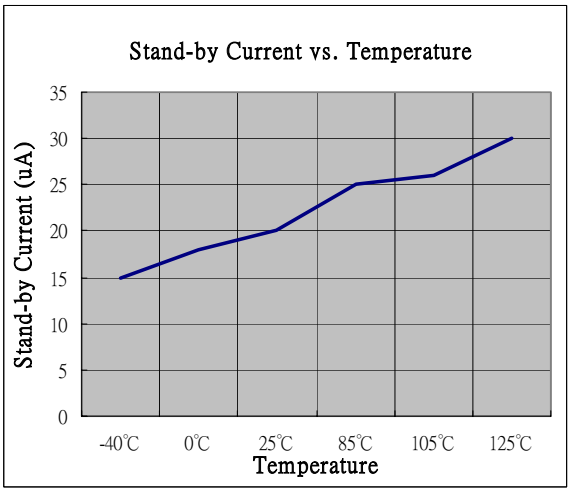


Typical Performance Characteristics (Continued)

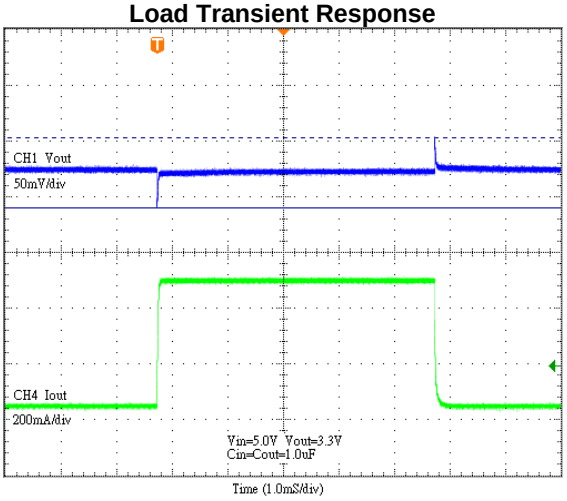




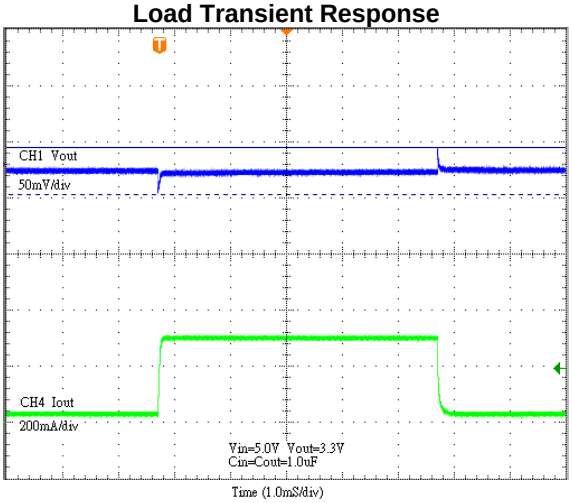




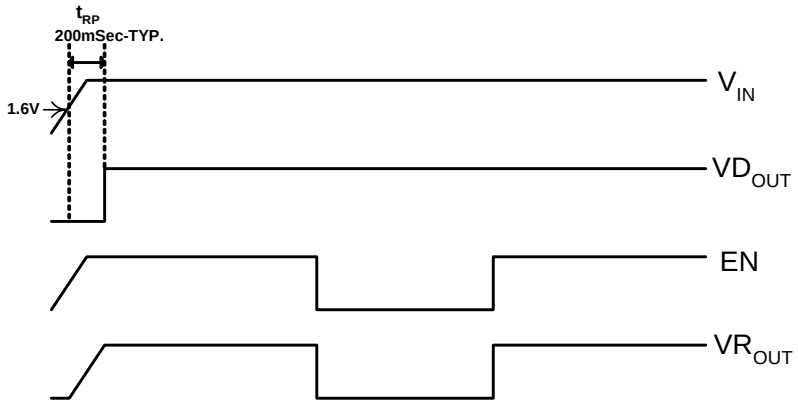
Load Transient Response



Load Transient Response



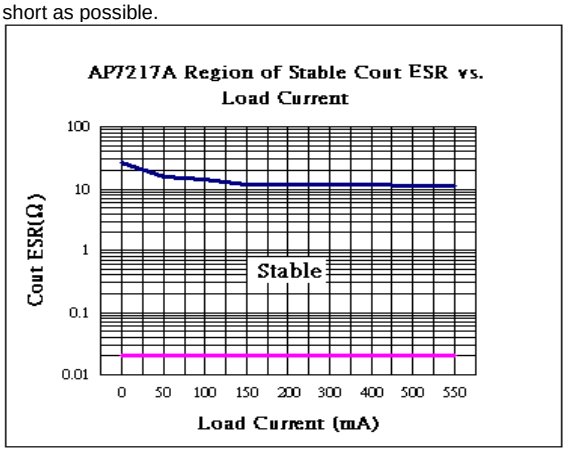
Timing Diagram



Application Note

Input Capacitor
A 1μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. A lower ESR (Equivalent Series Resistance) capacitor allows the use of less capacitance, while higher ESR type requires more capacitance. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor
The output capacitor is required to stabilize and help the transient response of the LDO. The AP7217A is designed to have excellent transient response for most applications with a small amount of output capacitance. The AP7217 is stable with any small ceramic output capacitors of 1.0μF or higher value, and the temperature coefficients of X7R or X5R type. Additional capacitance helps to reduce undershoot and overshoot during transient. For PCB layout, the output capacitor must be placed as close as possible to OUT and GND pins, and keep the leads as short as possible.



ENABLE/SHUTDOWN Operation
The AP7217A is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

	VR_{OUT}	VD_{OUT}
EN=0	0V	Φ
EN=1	3.3V	Φ

Thermal Considerations
Thermal Shutdown Protection limits power dissipation in AP7217A. When the operation junction temperature exceeds 150°C, the Over Temperature Protection circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 40°C. For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is:

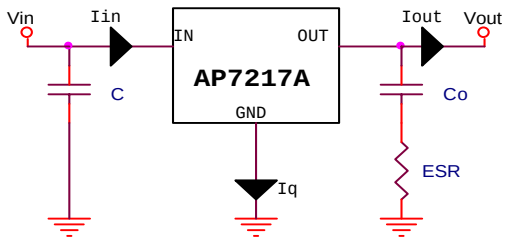
$$P_D = (V_{IN} - V_{OU}T) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - TA) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

Application Note (Continued)



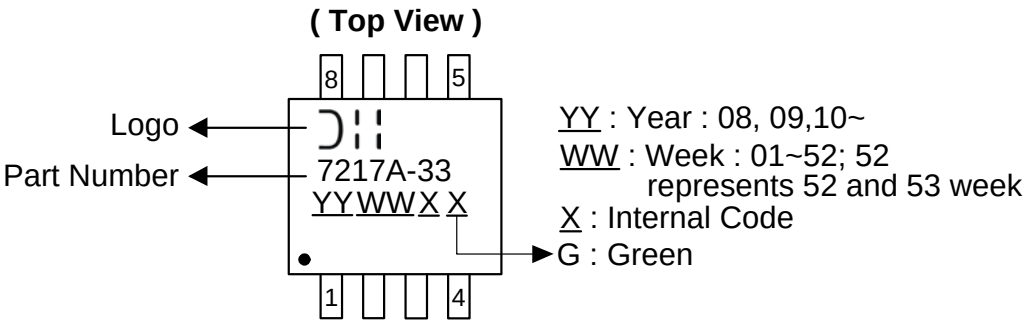
Current Limit Protection
When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 750mA to prevent over-current and to protect the regulator from damage due to overheating.

Short circuit protection
When VR_{OUT} pin is shorted to GND or VR_{OUT} voltage is less than 200mV, short circuit protection will be triggered and clamp the output current to approximately 50mA.

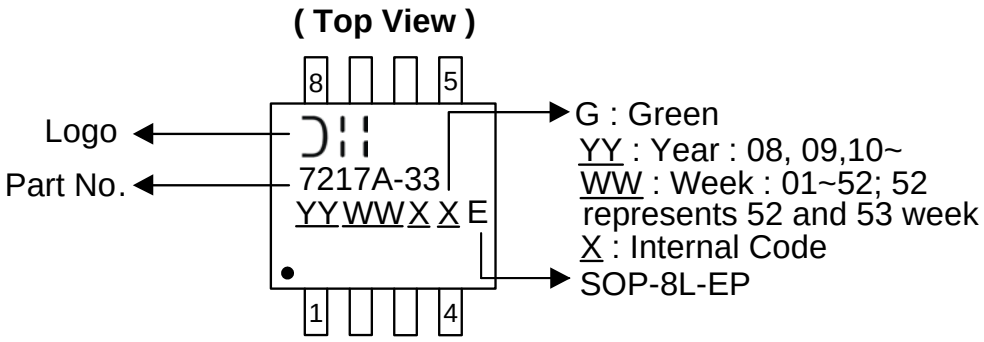
VD_{OUT} (reset output)
---Open-Drain Active-Low reset output---
In general, VD_{OUT} is pulled up by a resistor (100Kohm) to V_{IN}. The AP7217A microprocess (uP) supervisory circuitry asserts a guaranteed logic-low reset during power-up and power-down. Reset is asserted asserts when V_{IN} is below the reset threshold and remain asserted for at least t_{RP} after V_{IN} rises above the reset threshold.
As long as V_{IN} is lower than the reset threshold, VD_{OUT} remains at logic "0". When V_{IN} become higher than V_{TH}, a logic "1" is asserted after a time delay defined by t_{RP}.

Marking Information

(1) SOP-8L

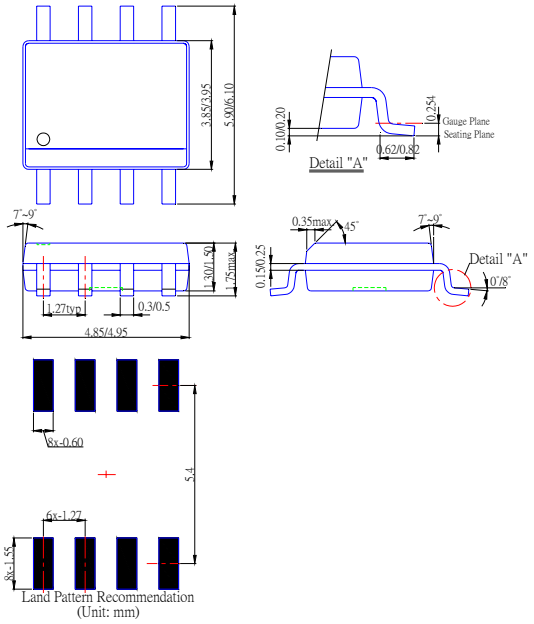


(2) SOP-8L-EP

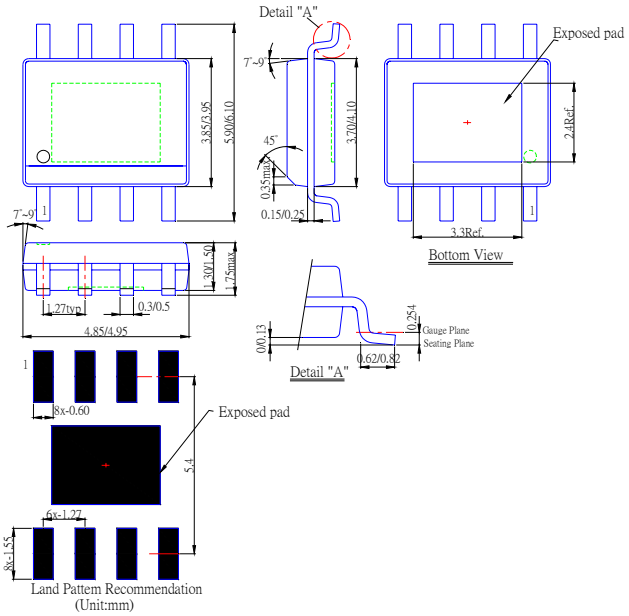


Package Information (All Dimensions in mm)

(1) Package Type: SOP-8L



(2) Package Type: SOP-8L-EP



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