

**BIDIRECTIONAL
ESD PROTECTION DIODE**

STAND-OFF VOLTAGE - **5.0** Volts
POWER DISSIPATION - **30** WATTS

GENERAL DESCRIPTION

The L03ESDL5V0CA2 is designed to protect sensitive electronics from damage or latch up due to ESD, lightning, and other voltage induced transient events.

FEATURES

- Bi-directional ESD Protection of one line.
- Max. peak pulse power : Ppp = 30W at tp = 8/20 us
- Low clamping voltage
- IEC 61000-4-2, level 4 (ESD), > 25KV (air) ; > 11KV (contact).

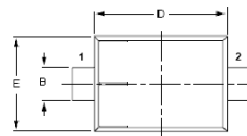
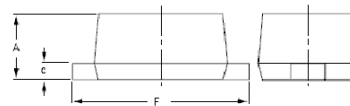
APPLICATION

- Computers and peripherals
- Communication system
- Audio & video equipment
- Portable Instrumentation

MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br,Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/EC

SOD-523



SOD-523		
DIM.	MIN.	MAX.
A	0.51	0.77
B	0.25	0.35
C	0.08	0.15
D	1.10	1.30
E	0.75	0.85
F	1.50	1.70

All Dimensions in millimeter

PIN ASSIGNMENT	
1	Cathode
2	Cathode

MAXIMUM RATINGS (Tj= 25°C unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak pulse Power (8/20us Waveform)	PPPM	30	W
Peak Pulse Current (8/20us Waveform)	IPP	2	A
Operating Junction Temperature Range	TJ	-55 to + 105	°C
Storage Temperature Range	Tstg	-55 to + 150	°C
Soldering Temperature, t max = 10s	TL	260	°C

ELECTRICAL CHARACTERISTICS (Tj= 25°C unless otherwise noticed)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reverse standoff voltage	VDRM	---	---	---	5.0	V
Reverse leakage current	IRM	VDRM = 5 V	---	---	100	nA
Breakdown voltage	VBR	IR = 1 mA	5.5	---	9.5	V
Junction capacitance	CJ	VR = 0 V , f = 1MHz	---	3.0	3.5	pF
Clamping voltage	VCL	IPP = 1 A (8/20us)	---	---	12	V
Clamping voltage	VCL	IPP = 2 A (8/20us)	---	---	15	V

REV.2, Aug-2014, KSIR50

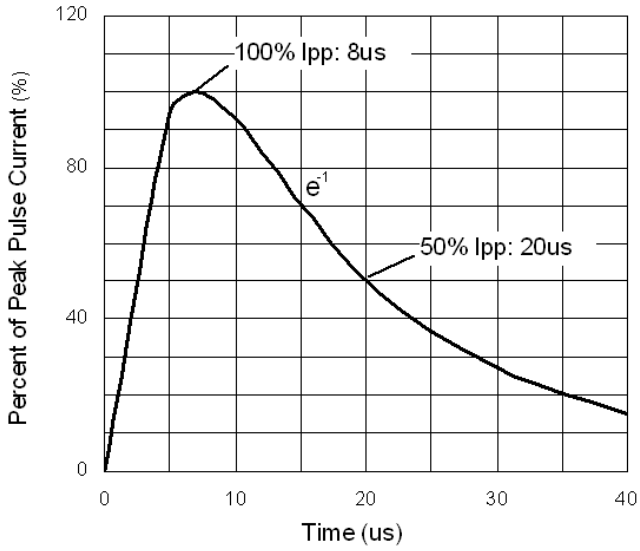


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

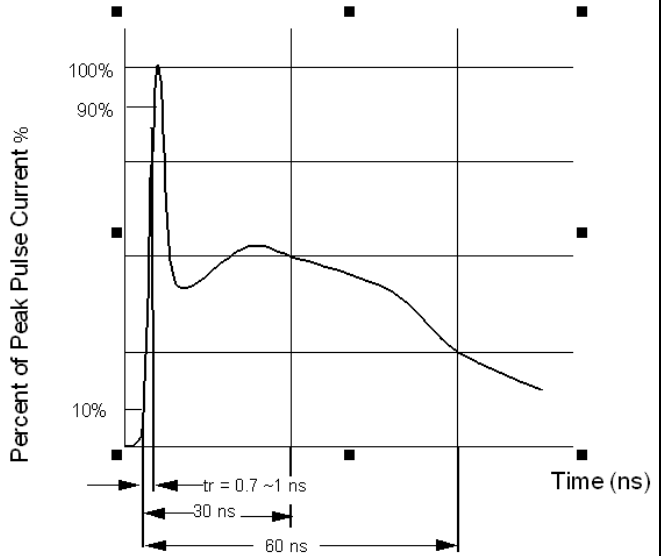


Figure 2. ESD pulse waveform according to IEC 61000-4-2

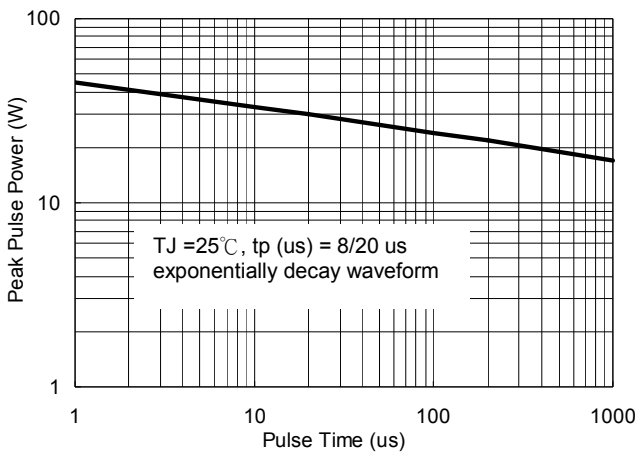


Figure 3. Power Dissipation versus Pulse Time

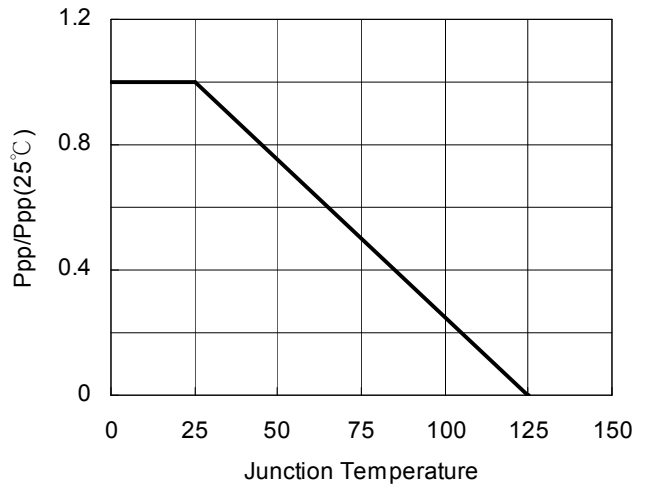


Figure 4. Peak pulse power versus TJ

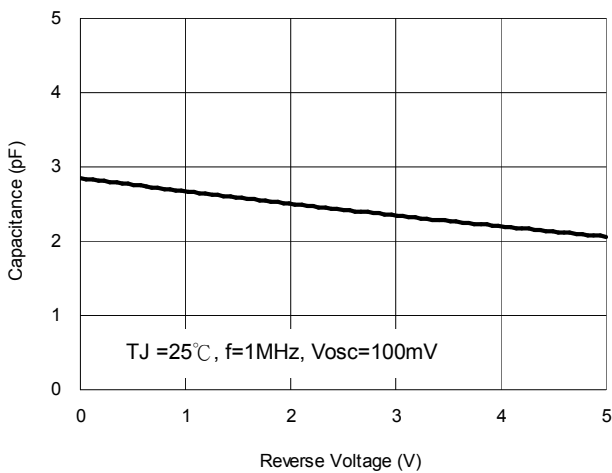


Figure 5. Typical Junction Capacitance

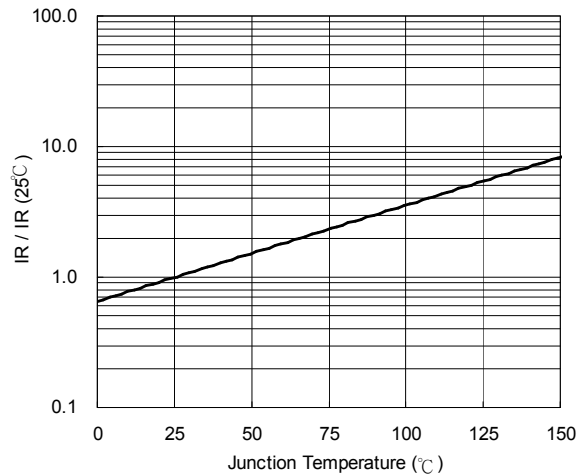


Figure 6. Reverse Leakage Current versus TJ

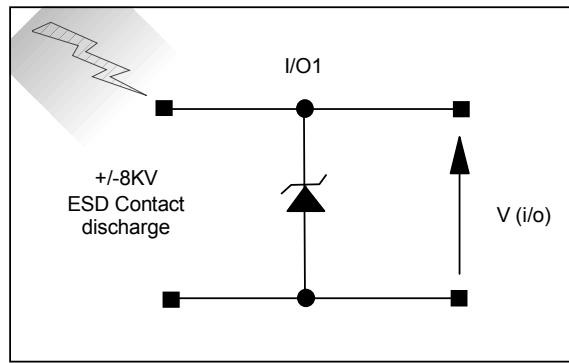


Figure 7. ESD Test Configuration

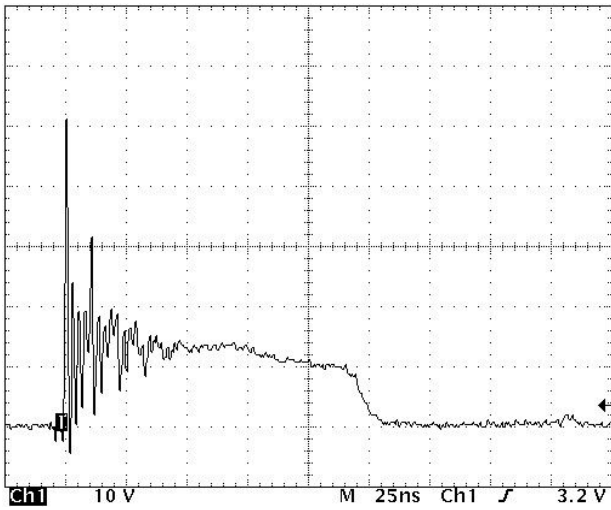


Figure 8. Clamped +8 kV ESD voltage waveform

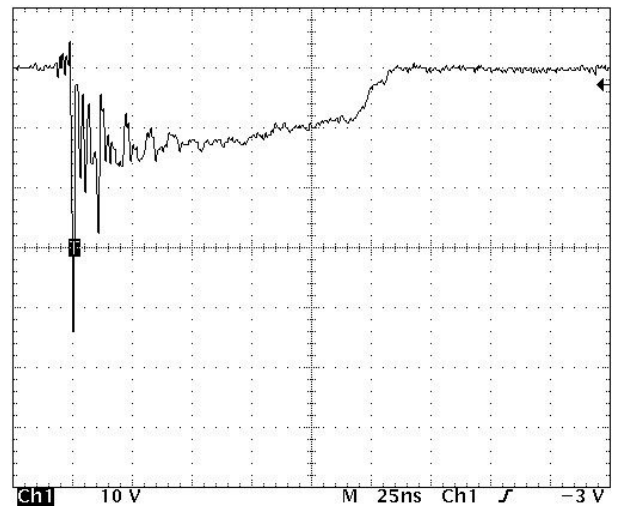
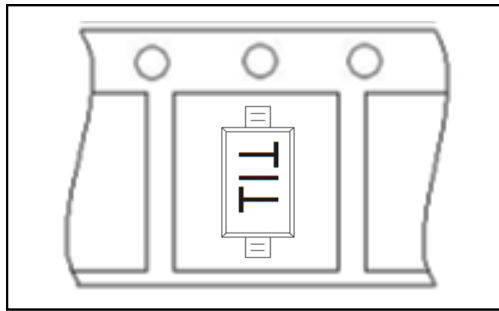


Figure 9. Clamped -8 kV ESD voltage waveform

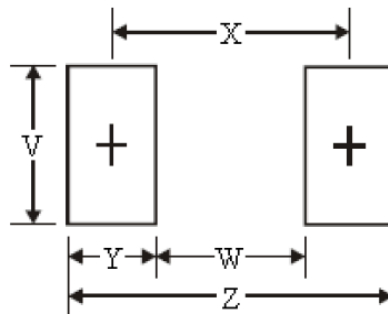
Marking & Orientation



Packaging Information

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L03ESDL5V0CA2	3000	7	45000	90K/180K

SOD-523 Soldering Pad Layout



Dim.	Millimeters	Inches
Z	2.30	0.090
X	1.50	0.059
W	0.70	0.027
Y	0.80	0.031
V	0.60	0.023

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