

**DUAL ESD PROTECTION DIODES**

STAND-OFF VOLTAGE - 5 Volts  
POWER DISSIPATION - 340 WATTS

**GENERAL DESCRIPTION**

- The L30ESDL5V0C3-2 is a ultra low capacitance Electrostatic Discharge (ESD) protection diode in a SOT23 (TO236AB) small SMD plastic package designed to protect one high speed data line from the damage caused by ESD and other transients.

**FEATURES**

- Unidirectional ESD protection of two line.
- Max. peak pulse power : Ppp = 340W at tp = 8/20 us
- IEC 61000-4-2, level 4
- IEC 61000-4-2 (ESD), >+30KV(air) ;>+23KV(contact) .
- IEC 61000-4-5, level 1
- Low clamping voltage
- Qualified to AEC-Q101 Rev\_C

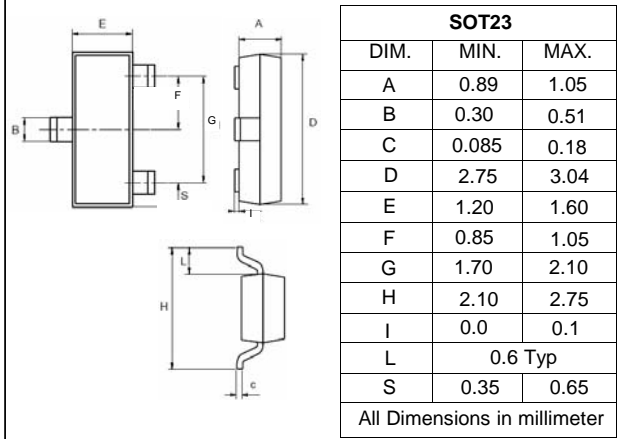
**APPLICATION**

- Computers and peripherals
- Communication system
- 10/100/1000 Ethernet
- Local Area Network (LAN) equipment.
- High speed data line
- 100%Tin Matte finish (Lead-Free Product)

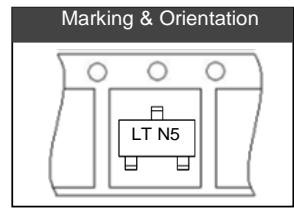
**MECHANICAL DATA**

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2011/65/EU
- Weight :0.009 grams

**SOT23**



PIN ASSIGNMENT	
1	Cathode
2	Cathode



**MAXIMUM RATINGS (Tj= 25°C unless otherwise noticed)**

Rating	Symbol	Value	Unit
Peak pulse Power ( 8/20us Waveform)	PPPM	340	W
Operating Junction Temperature Range	TJ	-55 to + 125	°C
Storage Temperature Range	Tstg	-55 to + 150	°C
Soldering Temperature, t max = 10s	TL	260	°C

**ELECTRICAL CHARACTERISTICS (Tj= 25°C unless otherwise noticed)**

Parameter	Symbol	Conditions	Min	Max	Unit
Reverse standoff voltage	VDRM	---	---	5.0	V
Reverse leakage current	IRM	VDRM = 5.0V	---	5	uA
Breakdown voltage	VBR	IR = 1 mA	6.4	---	V
Diode capacitance	CJ	VR = 0 V , f = 1MHz	---	1.2	pF
Clamping Voltage	VC	Ipp= 1 A	---	9.8	V
Clamping Voltage	VC	Ipp= 17 A	---	20	V
Max.peak pulse current	Ipp	8/20 us	---	17	A

REV. 11, Mar-2017, KSIR07

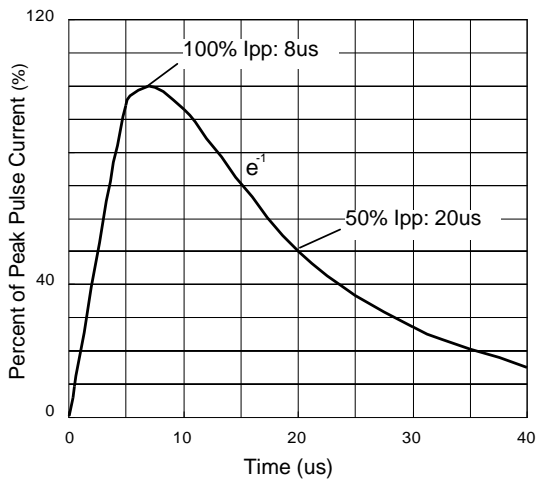


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

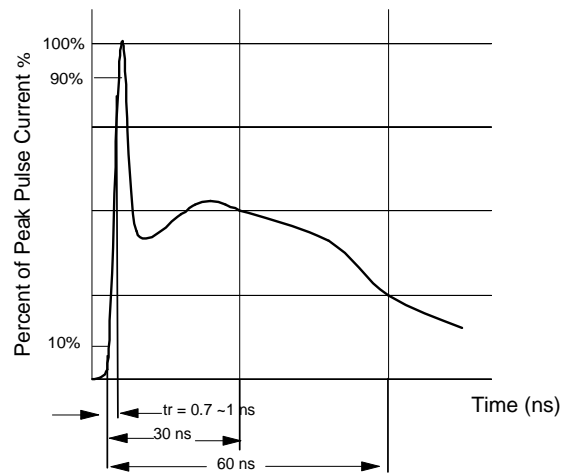


Figure 2. ESD pulse waveform according to IEC 61000-4-2

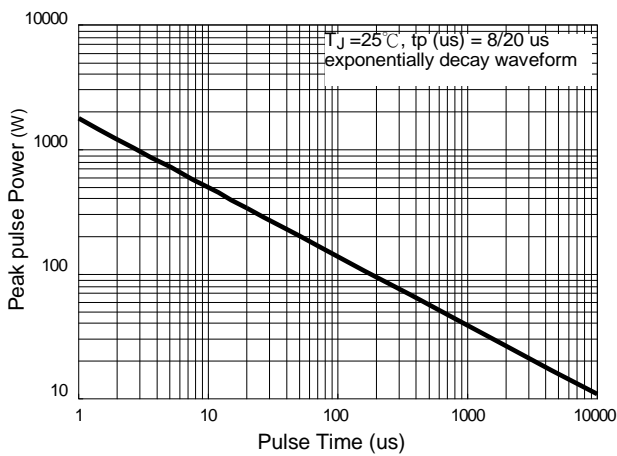


Figure 3. Power Dissipation versus Pulse Time

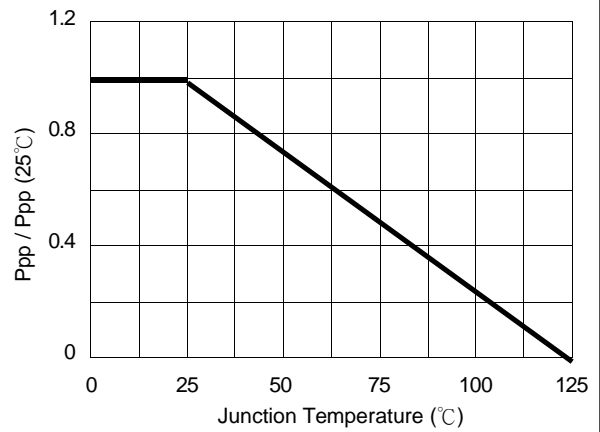


Figure 4. Peak pulse power versus TJ

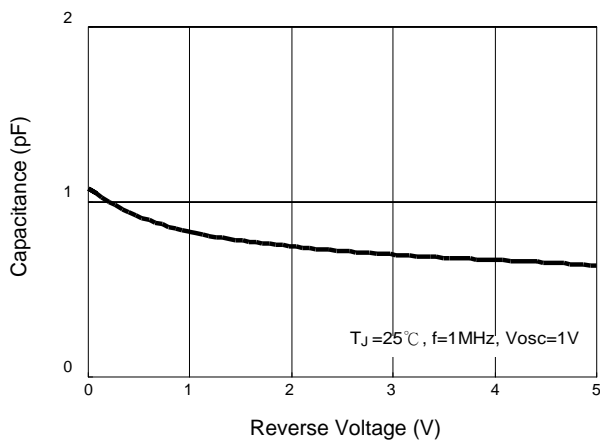


Figure 5. Typical Junction Capacitance

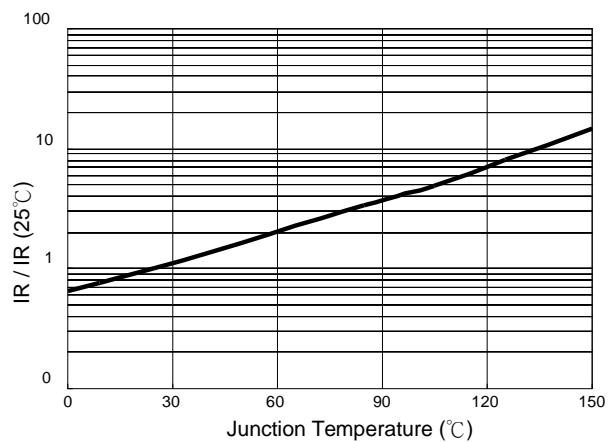


Figure 6. Reverse Leakage Current versus TJ

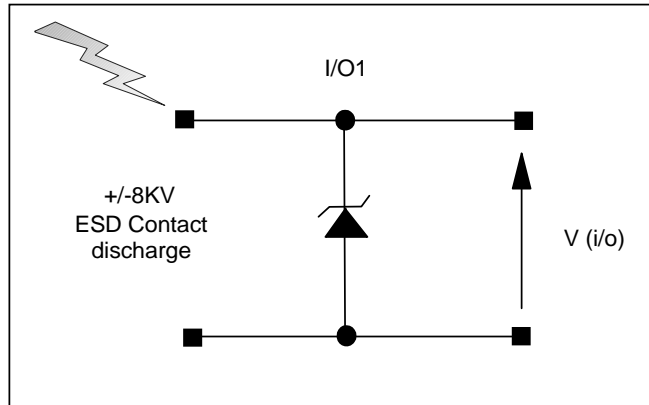


Figure 6. ESD Test Configuration

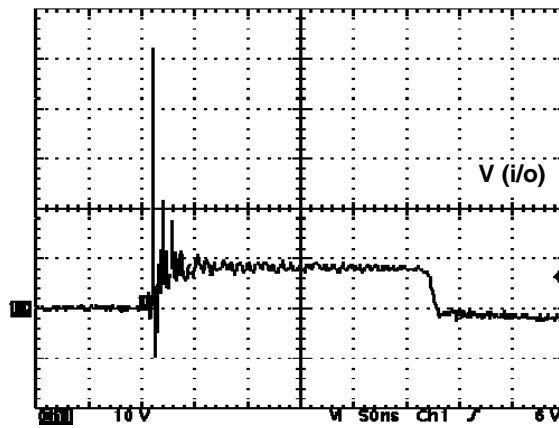


Figure 8. Clamped +8 kV ESD voltage waveform

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