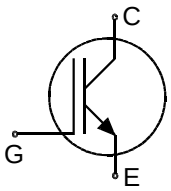
SIGC121T120R2C

IGBT Chip in NPT-technology

Features:
- 1200V NPT technology
- low turn-off losses
- short tail current
- positive temperature coefficient
- easy paralleling
- integrated gate resistor

This chip is used for:
- power module
  BSM 75GD120DN2

Applications:
- drives



Chip Type	V_{CE}	I_C	Die Size	Package
SIGC121T120R2C	1200V	75A	11.08 X 11.08 mm^2	sawn on foil

Mechanical Parameter

Raster size	11.08 X 11.08	mm^2
Emitter pad size	8 x (2.99 x 1.97)	
Gate pad size	1.46 x 0.8	
Area total	122.8	
Thickness	200	µm
Wafer size	150	mm
Max.possible chips per wafer	106	
Passivation frontside	Photoimide	
Pad metal	3200 nm AlSiCu	
Backside metal	Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	Electrically conductive glue or solder	
Wire bond	Al, <500µm	
Reject ink dot size	∅ 0.65mm ; max 1.2mm	
Recommended storage environment	Store in original container, in dry nitrogen, in dark environment, < 6 month at an ambient temperature of 23°C	

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Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, T_{vj} =25 °C	V_{CE}	1200	V
DC collector current, limited by $T_{vj\,max}$	I_C	1)	A
Pulsed collector current, t_p limited by $T_{vj\,max}$	$I_{c,puls}$	225	A
Gate emitter voltage	V_{GE}	±20	V
Junction temperature range	T_{vj}	-55 ... +175	°C
Operating junction temperature	T_{vj}	-55...+150	°C
Short circuit data 2) V_{GE} = 15V, V_{CC} = 900V, T_{vj} = 150°C	t_{SC}	10	µs
Reverse bias safe operating area 2) (RBSOA)	$I_{C,max}$ = 150A, $V_{CE,max}$ = 1200V $T_{vj} \leq 150$°C		

1) depending on thermal properties of assembly

2) not subject to production test - verified by design/characterization

Static Characteristic (tested on wafer), T_{vj} =25 °C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V , I_C= 4mA	1200			V
Collector-Emitter saturation voltage	V_{CEsat}	V_{GE}=15V, I_C=75A	2.0	2.5	3.0	
Gate-Emitter threshold voltage	$V_{GE(th)}$	I_C=3mA , V_{GE}=V_{CE}	4.5	5.5	6.5	
Zero gate voltage collector current	I_{CES}	V_{CE}=1200V , V_{GE}=0V			9.2	µA
Gate-Emitter leakage current	I_{GES}	V_{CE}=0V , V_{GE}=20V			480	nA
Integrated gate resistor	r_G			5		Ω

Dynamic Characteristic (not subject to production test - verified by design / characterization), T_{vj} =25 °C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	C_{ies}	V_{CE}=25V,		5100		pF
Output capacitance	C_{oes}	V_{GE}=0V,		720		
Reverse transfer capacitance	C_{res}	f=1MHz		380		

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Further Electrical Characteristic

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

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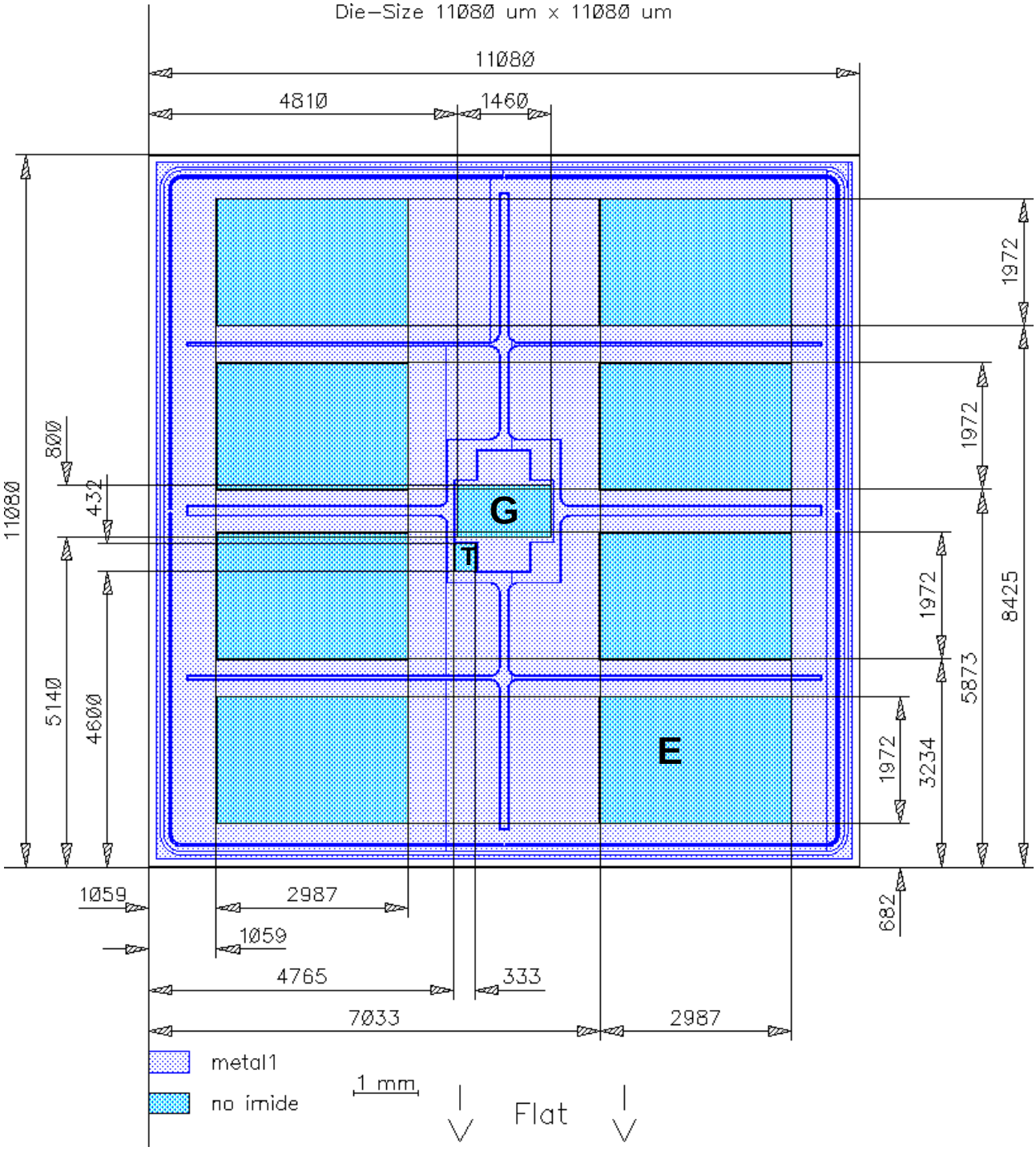
Chip Drawing



E = Emitter pad
G = Gate pad
T = Test pad do not contact

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Description

AQL 0,65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

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