A product Line of
Diodes Incorporated

PI4ULS3V4857

6-Bit Bi-directional Level Shifter for SD 3.0-SDR104 Compliant Memory Card Application

Features

- Supports up to 208 MHz clock rate
- Supports 1.2V to 1.8V host side interface voltage
- Voltage translation supports SDR104, SDR50, DDR50, SDR25, SDR12, High-Speed and Default-Speed modes and comply SD 3.0 specification
- Automatic enable and disable through VSD supply pin
- Built-in 100mA Low dropout voltage regulator to supply the voltage of memory card I/Os
- Integrated pull-up and pull-down resistors
- Integrated EMI filters for digital I/Os
- On card side, supports 8 kV ESD protection(IEC 61000-4-2, level 4)
- Level shifting buffers keep ESD stress away from the host
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen- and Antimony-Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 20-ball (WLCSP), pitch 0.4 mm

Description

The device is an SD 3.0-compliant bidirectional dual voltage level translator without direction pin control. It can translate the memory card voltage to 1.8V or 3.0V signal levels from 1.2V to 1.8V of host side and supports SD 3.0 SDR104(208Mhz), SDR50(100Mhz), DDR50(50Mhz), SDR25(50Mhz), SDR12(25Mhz) and SD 2.0 High-Speed (50 MHz) and Default-Speed (25 MHz) modes.

To supply the memory card I/Os, the device has an integrated voltage selectable regulator and an auto-enable/disable function that connects to the VSD supply pin. The device also has built-in EMI filters and ESD protections.

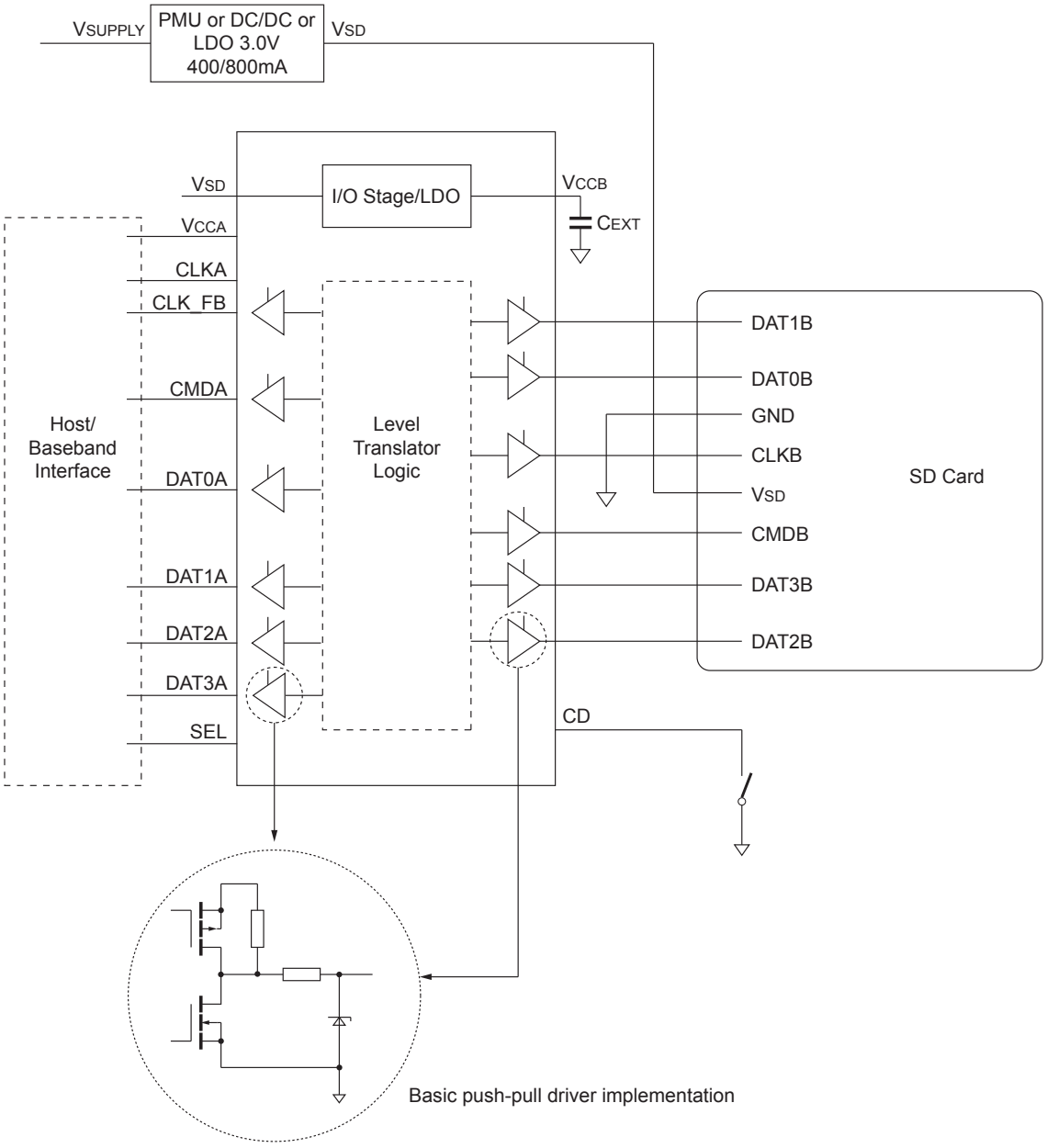
Applications

- Smart phones
- Mobile handsets
- Digital cameras
- Tablet PCs
- Laptop computers
- SD, MMC or microSD card readers

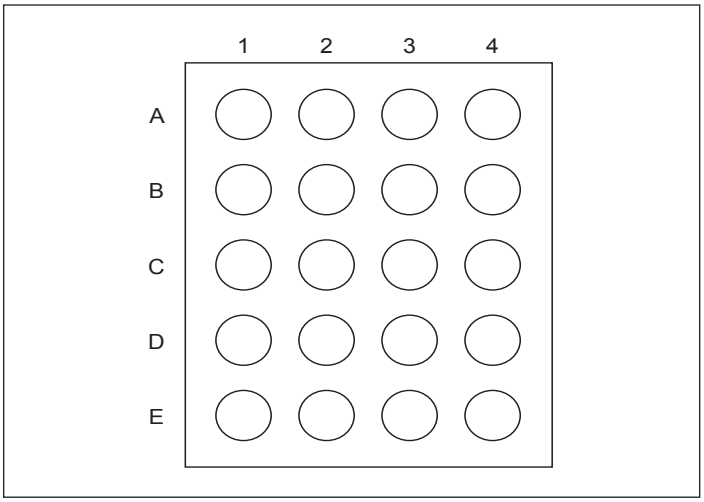
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Block Diagram



Pin Configuration (Top-Side View)



Pin Description

Pin #	Pin Name	Type	Description
A1	DAT2A	I/O	Data 2 input or output on host side
A2	V_{CCA}	Pwr	Supply voltage from host side
A3	V_{SD}	Pwr	Supply voltage
A4	DAT2B	I/O	Data 2 input or output on memory card side
B1	DAT3A	I/O	Data 3 input or output on host side
B2	CD	O	High voltage output (refer to V_{CCA})
B3	V_{CCB}	Pwr	Internal supply decoupling (V_{LDO})
B4	DAT3B	I/O	Data 3 input or output on memory card side
C1	CMDA	I/O	Command input or output on host side
C2	GND	Pwr	Supply ground
C3	GND	Pwr	Supply ground
C4	CMDB	I/O	Command input or output on memory card side
D1	DAT0A	I/O	Data 0 input or output on host side
D2	CLKA	I	Clock signal input on host side
D3	CLKB	O	Clock signal output on memory card side
D4	DAT0B	I/O	Data 0 input or output on memory card side
E1	DAT1A	I/O	Data 1 input or output on host side
E2	CLK_FB	O	Clock feedback output on host side
E3	SEL	I	Card side I/O voltage level select
E4	DAT1B	I/O	Data 1 input or output on memory card side

Note:

1. The pin names relate particularly to SD memory cards, but also apply to microSD and MMC memory cards.
2. I = input, O = output, I/O = input and output, S = power supply

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–55°C to +150°C
Junction Temperature	125°C max
Supply Voltage to Ground Potential	–0.5V to +4.6V
Host Side Input Voltage	–0.5V to +2.2V
Card Side Input Voltage	–0.5V to +4.6V
Power Dissipation Continuous	1000mW
I/O Latch-up Current	-100mA to +100mA
ESD, HBM	–2000V to +2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Limiting Values

Symbol	Parameter	Conditions		Min.	Max.	Units
V_{CC}	Supply voltage	4ms transient	On pin V_{SD}	-0.5	+4.6	V
			On pin V_{CCA}	-0.5	+2.2	V
V_I	Input voltage	4ms transient at I/O pins, port A max. = 2.2V		-0.5	+4.6	V
P_{tot}	Total power dissipation	T_{amb} = -40 °C to +85 °C			1000	mW
T_{stg}	Storage temperature			-55	150	°C
V_{ESD}	Electrostatic discharge voltage	IEC 61000-4-2, level 4, all memory card-side pins, V_{SD} and CD to ground(1)	Contact discharge	-8	8	kV
			Air discharge	-15	15	kV
			Human Body Model (HBM) JEDEC JESD22-A114F; all pins	-2000	2000	V
			Charge Device Model (CDM) JEDEC JESD22-C101E; all pins	-500	500	V
$I_{Iu(IO)}$	Input/output latch-up current	JESD 78B: -0.5 x V_{CC} < V_I < 1.5 x V_{CC}; T_j < 125 °C		-100	100	mA

Note: 1. All system level tests are performed with the application-specific capacitors connected to the supply pins V_{SUPPLY}, V_{LDO} and V_{CCA}.

Recommended Operating Conditions

Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage	On pin V_{SD}	2.9(1)		3.6	V
		On pin V_{CCA}	1.1		2.0	V
V_I	Input voltage	Host side	-0.3(2)		V_{CCA} + 0.3	V
		Memory card side	-0.3		$V_{O(LDO)}$ + 0.3	V
C_{ext}	External capacitance	Recommended capacitor at pin V_{CCB}		2.2		µF
ESR	Equivalent series resistance	At pin V_{LDO}	0		50	mΩ
C_{ext}	External capacitance	Recommended capacitor at pin V_{SD}		0.1		µF
		Recommended capacitor at pin V_{CCA}		0.1		µF

Note:
1. By minimum value the device is still fully functional, but the voltage on pin VLDO might drop below the recommended memory card supply voltage.
2. The voltage must not exceed 3.6 V.

Integrated Resistors

Tamb = 25°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{pd}	Pull-down resistance	R3; tolerance ±30 %	70	100	130	Ω
		R5	200	350	500	kΩ
R_{pu}	Pull-up resistance	All data lines and CMDx	21	30	39	kΩ
		R4	70	100	130	kΩ
R_s	Series resistance	Host side; R1; tolerance ±30 %	(1)	22.5		Ω
		Card side; R2; tolerance ±30 %	(1)	15		Ω

Note:
1. Guaranteed by design.

Static Characteristics

At recommended operating conditions; T_{amb} = 40°C to +85°C; voltages are referenced to GND (ground = 0 V); C_{ext} = 2.2 µF at pin V_{CCB}; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.(2)	Max.	Units
Automatic Enable Feature: V_{SD}						
V_{SDen}	Device enable voltage level	$V_{CCA} \geq 1.0V$, V_{SD} rising edge	2.05	2.25	2.45	V
$V_{SDdisable}$	Device disable voltage level	$V_{CCA} \geq 1.0V$, V_{SD} rising edge	2.0	2.2	2.4	V
ΔV_{SDen}	V_{SDen} hysteresis voltage			50		mV
Supply Voltage Regulator for Card-side I/O Pin: V_{CCB}						
$V_{O(LDO)}$	Regulator/switch output voltage	SEL = LOW; 3.0V ≤ V_{SD} ≤ 3.6V; I_O < 100mA	V_{SD}-0.2	V_{SD}-0.1	V_{SD}	V
		SEL = HIGH; V_{SD} ≥ 2.9V; I_O < 100mA	1.7	1.8	1.95	V
$I_{O(LDO)}$	Regulator/switch output current				100	mA
Host-side Input Signals: CMDA and DAT0A to DAT3A, CLKA; 1.1V ≤ V_{CCA} ≤ 2.0V						
V_{IH}	High level input voltage		0.75 x V_{CCA}		V_{CCA} + 0.3	V
V_{IL}	Low level input voltage		-0.3		0.25 x V_{CCA}	V
Host-side Control Signals; 1.1V ≤ V_{CCA} ≤ 2.0V — SEL						
V_{IH}	High level input voltage		0.75 x V_{CCA}		V_{CCA} + 0.3	V
V_{IL}	Low level input voltage		-0.3		0.25 x V_{CCA}	V
Host-side Output Signals: CLK_FB, CMDA and DAT0A to DAT3A; 1.1V ≤ V_{CCA} ≤ 2.0V						
V_{OH}	High level output voltage for CLK_FB	I_O = 2mA; V_I = V_{IH} (card side)	0.8 x V_{CCA}			V
	High level output voltage for CMDA, DATxA	IO = 2µA; V_I = V_{IH} (card side)	0.8 x V_{CCA}			V

Static Characteristics Cont.

Symbol	Parameter	Conditions		Min.	Typ.(2)	Max.	Units
V_{OL}	Low level output voltage	I_O = 2mA; V_I = V_{IL} (card side)				0.15 x V_{CCA}	V
Card-side Input Signals: CMDB and DAT0B to DAT3B							
V_{IH}	High level input voltage	SEL = LOW (3.0V card interface)		0.625 x $V_{O(LDO)}$		$V_{O(LDO)}$ + 0.3	V
		SEL = HIGH (1.8V card interface)		0.625 x $V_{O(LDO)}$		$V_{O(LDO)}$ + 0.3	V
V_{IL}	Low level input voltage	SEL = LOW (3.0V card interface)		-0.3		0.3 x $V_{O(LDO)}$	V
		SEL = HIGH (1.8V card interface)		-0.3		0.3 x $V_{O(LDO)}$	V
Card-side Output Signal — CMDB and DAT0B to DAT3B, CLKB							
V_{OH}	High level output voltage for CLKB only	I_O = 4mA; V_I = V_{IH} (host side); SEL = LOW (3.0V card interface)		0.85 x $V_{O(LDO)}$		$V_{O(LDO)}$ + 0.3	V
		I_O = 2mA; V_I = V_{IH} (host side); SEL = HIGH (1.8V card interface)		0.85 x $V_{O(LDO)}$		2.0	V
	High level output voltage for CMDB, DATxB	I_O = 2µA; V_I = V_{IH} (host side); SEL = HIGH (1.8V card interface)		0.85 x $V_{O(LDO)}$		2.0	V
V_{OL}	Low level output voltage	I_O = -4mA; V_I = V_{IL} (host side); SEL = LOW (2.9V card interface)		-0.3		0.125 x $V_{O(LDO)}$	V
		I_O = -2mA; V_I = $V_{I\ card\ L}$ (host side); SEL = HIGH (1.8V interface)		-0.3		0.125 x $V_{O(LDO)}$	V
Card-side Output Signal — Bus Signal Equivalent Capacitance							
C_{ch}	Channel capacitance	V_I = 0V; f_i = 1 MHz; V_{SD} = 3.0V; V_{CCA} = 1.8V	Host side	(3)	7		pF
			Card side		15		pF
Current Consumption							
$I_{CC(stat)}$	Static supply current	$V_{SD} \geq V_{SDen}$ (active mode); All inputs = HIGH	SEL = LOW (3.0V card interface)			100	µA
			SEL = HIGH (1.8V card interface)			100	µA
$I_{CC(stb)}$	Standby supply current	VSD ≤ VSDen and VCCA ≥ 1.0V (Inactive mode); All host side inputs = HIGH				7	µA

Note:
1. Guaranteed by design and characterization.
2. Typical values are measured at T_{amb} = 25°C.
3. EMI filter line capacitance per data channel from I/O driver to pin; C_{ch} is guaranteed by design.

Dynamic Characteristics

Voltage Regulator

(T_{amb} = 25°C; unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Regulator Output Pin: V_{CCB}						
$t_{startup(LDO)}$	Regulator start-up time	V_{CCA} = 1.8V; V_{SD} = 3.0V; C_{ext} = 2.2µF; see Figure 2			400	µs
$t_{f(o)}$	Output fall time	$V_{O(LDO)}$ = 3.0V to 1.8V; SEL = LOW to HIGH; see Figure 1			1	ms
$t_{r(o)}$	Output rise time	$V_{O(LDO)}$ = 1.8V to 3.0V; SEL = HIGH to LOW; see Figure 5			100	µs

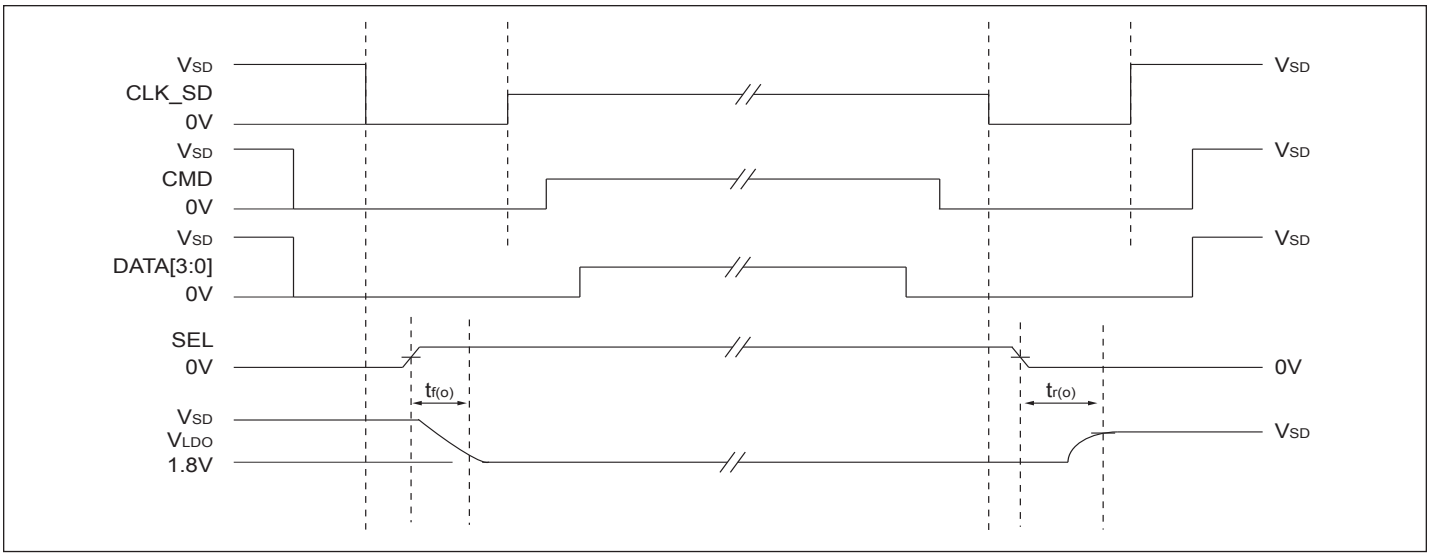


Figure 1. Regulator Mode Change Timing

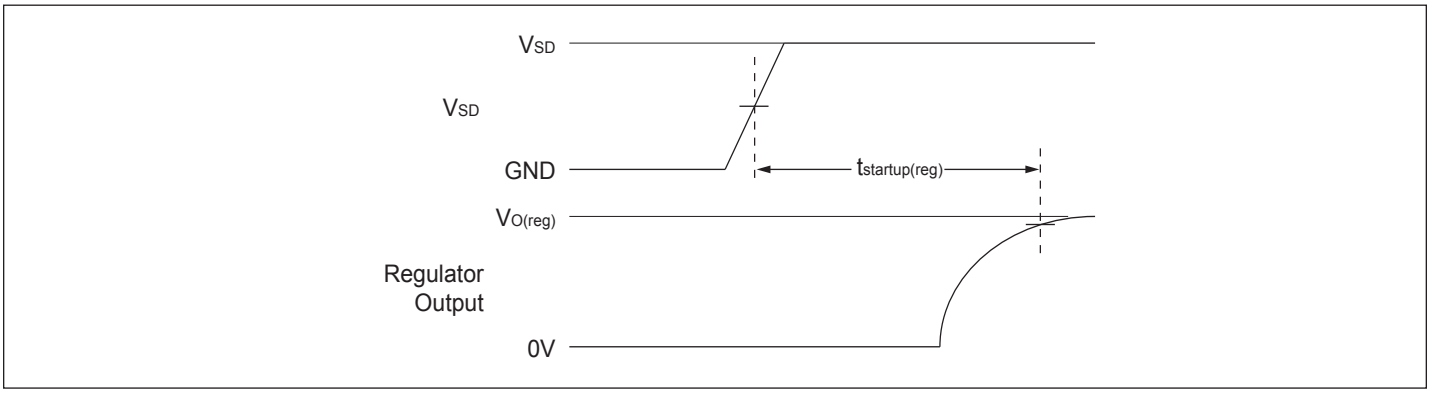


Figure 2. Regulator Start-up Time

Level Translator Dynamic Characteristics

At recommended operating conditions; V_{CCA} = 1.2V; T_{amb} = 25°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Host Side Transition Times						
t_r	Rise time	SEL = HIGH (1.8V card interface); V_{CCA} = 1.8V	(1)	0.4	1.0	ns
t_f	Fall time		(1)	0.4	1.0	ns
t_r	Rise time	SEL = HIGH (1.8V card interface); V_{CCA} = 1.2V	(1)	0.4	1.0	ns
t_f	Fall time		(1)	0.4	1.0	ns
Card Side Transition Times						
t_r	Rise time	SEL = HIGH (1.8V card interface); -40°C ≤ T_{amb} ≤ +85°C	0.4(2)	0.88	1.32	ns
t_f	Fall time		0.4(2)	0.88	1.32	ns
Card Input Transition Times						
t_r	Rise time	SEL = HIGH (1.8 V card interface); -40°C ≤ T_{amb} ≤ +85°C	0.2(3)	0.5	0.96	ns
t_f	Fall time		0.2(3)	0.45	0.96	ns
Host to Card Propagation Delay — DATxA to DATxB, CMDA to CMDB, CLKA to CLKB						
t_{pd}	Propagation delay	SEL = HIGH (1.8V card interface); V_{CCA} = 1.2V		3.0	5.5	ns
Host to Card Propagation Delay — CLKA to CLK_FB						
t_{pd}	Propagation delay	SEL = HIGH (1.8V card interface); V_{CCA} = 1.2V		5.5	10	ns
Card to Host Propagation Delay — DATxB to DATxA, CMDB to CMDA						
t_{pd}	Propagation delay	SEL = HIGH (1.8V card interface); V_{CCA} = 1.2V		2.5	4.5	ns

Note:
1. Transition between V_{OL} = 0.35 * V_{CCA} and V_{OH} = 0.65 * V_{CCA}
2. Transition between V_{OL} = 0.45V and V_{OH} = 1.4V
3. Guaranteed by design; transition between V_{IL} = 0.58V and V_{IH} = 1.27V with C_{trace} = 3.5 pF and $C_{card+CRADLE}$ = 12pF, trace length = 11mm

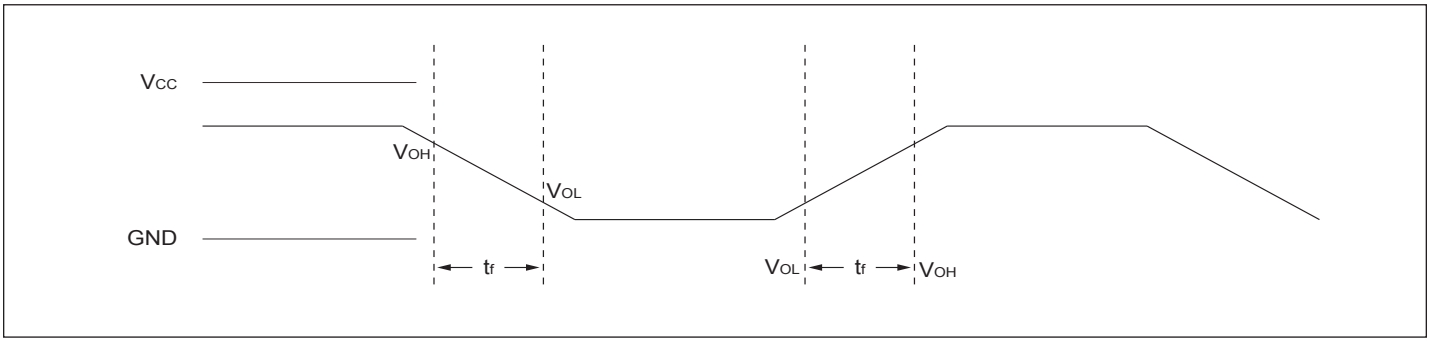


Figure 3. Output Rise and Fall Times

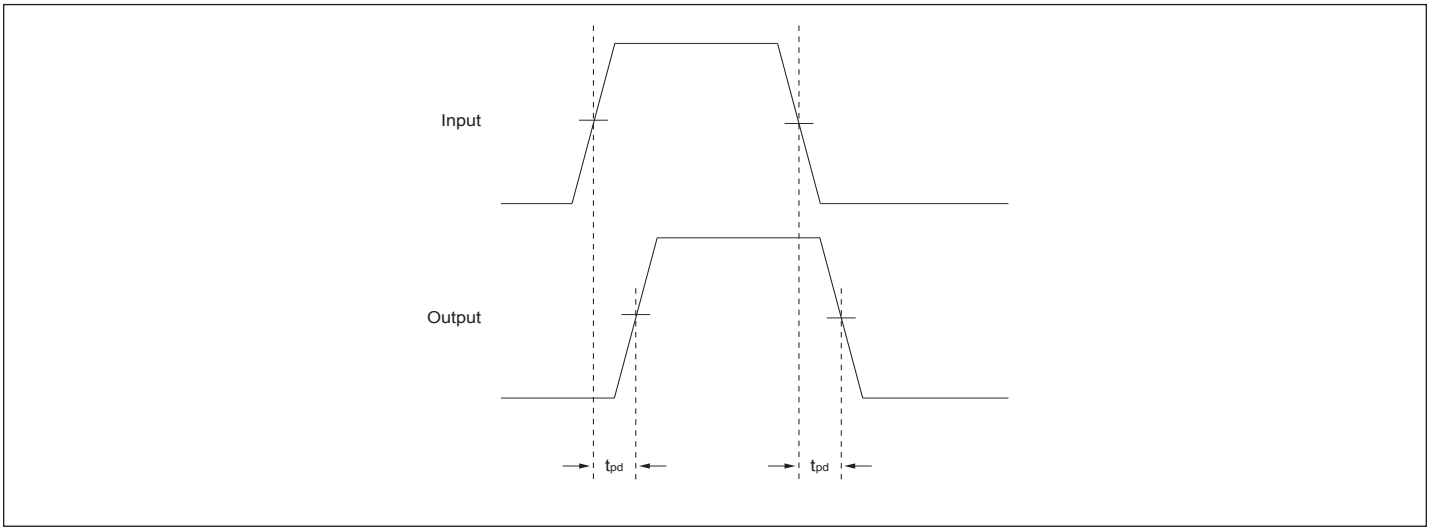
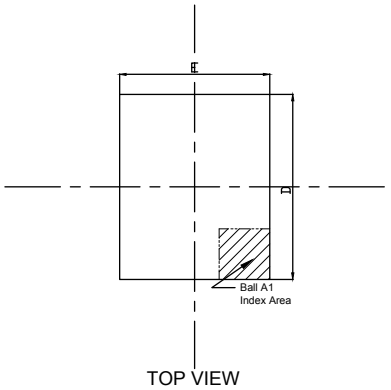


Figure 4. Output Delay Timing

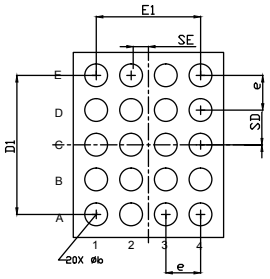
Part Marking

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

Package Mechanical: 20-WLCSP

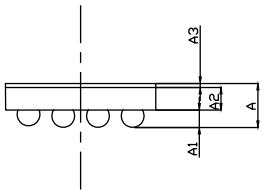


TOP VIEW

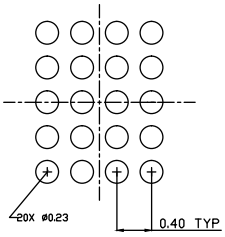


BOTTOM VIEW

PKG.	DIMENSIONS(MM)		
SYMBOL	Min.	Nom.	Max.
A	0.450	0490	0.530
A1	0.170	0.200	0.230
A2	0.245	0.265	0.285
A3	0.020	0.025	0.030
D	2.070	2.100	2.130
E	1.670	1.700	1.730
D1	1.550	1.600	1.650
E1	1.150	1.200	1.250
b	0.230	0.260	0.290
e	0.400BSC		
SD	0.000 BSC		
SE	0.200 BSC		



SIDE VIEW



RECOMMEND LAND PATTERN

Note:

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

20-1177

DIODES INCORPORATED | PERICOM ENABLING SERIAL CONNECTIVITY

DATE: 12/25/19

DESCRIPTION: 20-Ball, WLCSP, 2.10x1.70 (U-WLB2117-20)

PACKAGE CODE: GEA (GEA20)

DOCUMENT CONTROL #: PD-2248 **REVISION:A**

For latest package information:
See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Number	Package Code	Package Description
PI4ULS3V4857GEAEX	GEA	20-Ball, 2.10x1.70 (WLCSP) (U-WLB2117-20)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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