LITE-ON SEMICONDUCTOR

L09ESD3V3CE2

ESD PROTECTION DEVICE

STAND-OFF VOLTAGE – **3.3** Volts
POWER DISSIPATION – **90** WATTS

GENERAL DESCRIPTION

L09ESD3V3CE2 is designed to replace multilayer varistors (MLVs) in portable applications where low operating voltage is vital. They offer superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs. They are designed

to protect sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD), lightning, electrical fast transients (EFT), and cable discharge events (CDE).

FEATURES

- Protects one power or I/O line
- Max. peak pulse power : Ppp = 90W at tp = 8/20 us.
- Low clamping voltage
- IEC 61000-4-2, (ESD)> ±20KV (air) ; > ±10KV (contact)
- Qualified to AEC-Q101 Rev. C

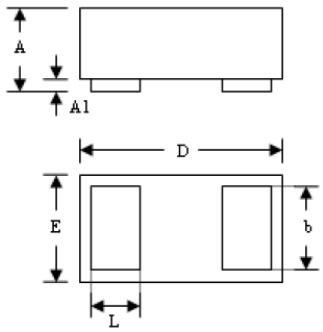
APPLICATION

- Cellular Handsets & Accessories
- Notebooks & Handhelds
- Portable Instrumentation
- Digital Cameras
- Peripherals
- MP3 Players

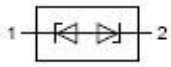
MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Moisture Sensitivity: Leve 1 per J-STD-020C
- Component in accordance to RoHs 2011/65/EU

SOD-882



SOD-882		
DIM.	MIN.	MAX.
A	0.47	0.53
A1	0.00	0.05
b	0.25	0.55
D	0.95	1.075
E	0.55	0.675
L	0.20	0.45
All Dimensions in millimeter		



PIN ASSIGNMENT	
1	Cathode
2	Cathode

MAXIMUM RATINGS (Tj= 25℃ unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20us)	P_{pk}	90	W
Peak Pulse Current (tp = 8/20us)	Ipp	5	A
Operating Junction Temperature Range	T_J	-55 to + 125	℃
Storage Temperature Range	Tstg	-55 to + 150	℃
Soldering Temperature, t max = 10s	T_L	260	℃

ELECTRICAL CHARACTERISTICS (Tj= 25℃ unless otherwise noticed)

Parameter	Symbol	Conditions	Mln	Typ	Max	Unit
Reverse standoff voltage	V_{RWM}		---	---	3.3	V
Punch Through Voltage	V_{PT}	I_{SB} = 2uA	3.5	---	---	V
Snap-Back Voltage	V_{SB}	I_{SB} = 50 mA	2.8	---	---	V
Reverse leakage current	I_{RM}	V_{DRM} = 3.3V	---	0.05	0.5	uA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20μs	---	6.0	8.0	V
Clamping Voltage	V_C	I_{PP} = 5 A, tp = 8/20μs	---	8.5	18	V
Junction capacitance	C_J	V_R = 0V, f = 1MHz	---	11	15	pF

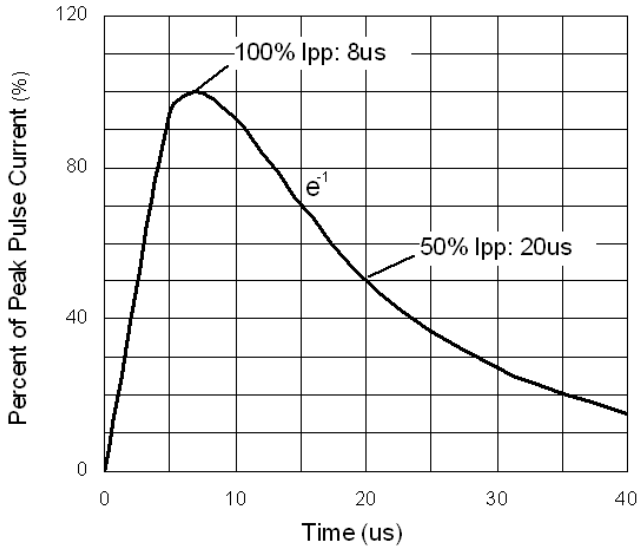


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

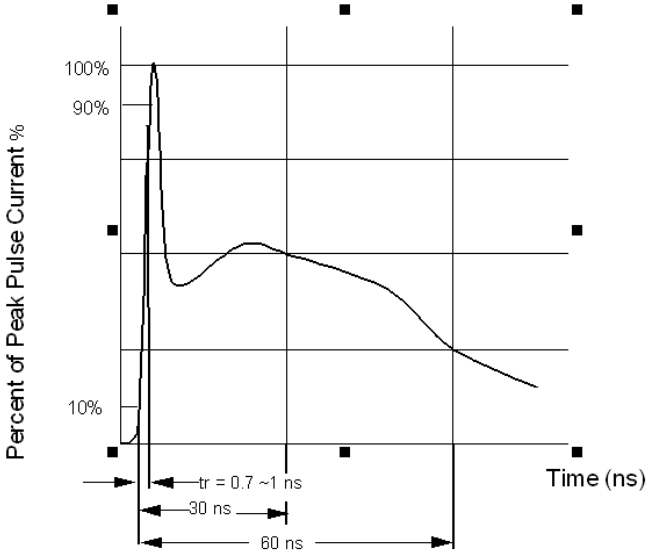


Figure 2. ESD pulse waveform according to IEC 61000-4-2

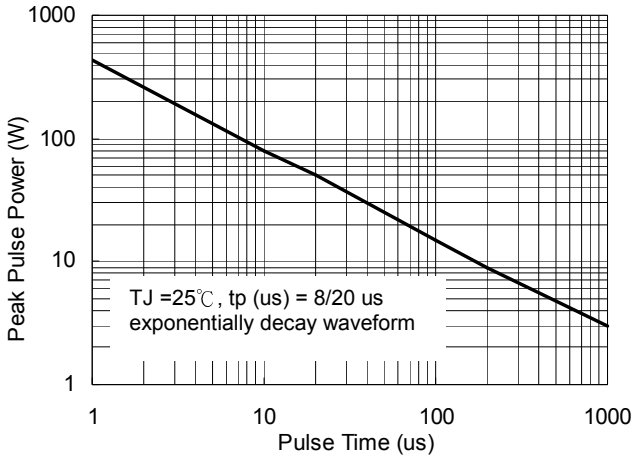


Figure 3. Power Dissipation versus Pulse Time

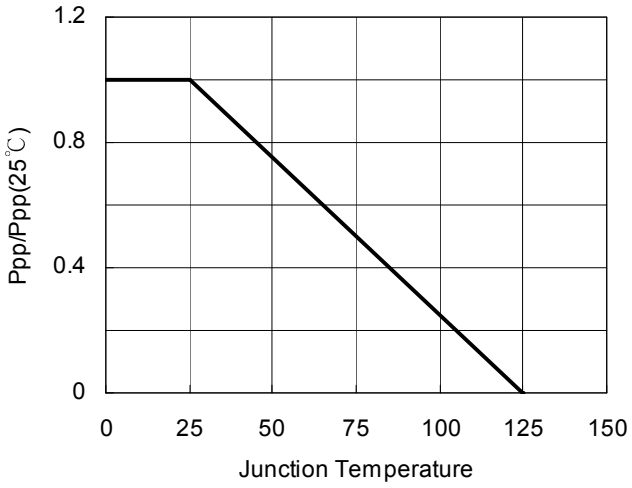


Figure 4. Peak pulse power versus TJ

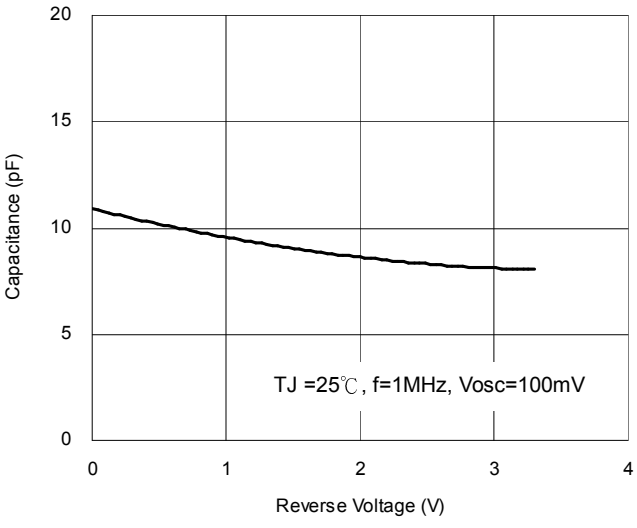


Figure 5. Typical Junction Capactiance

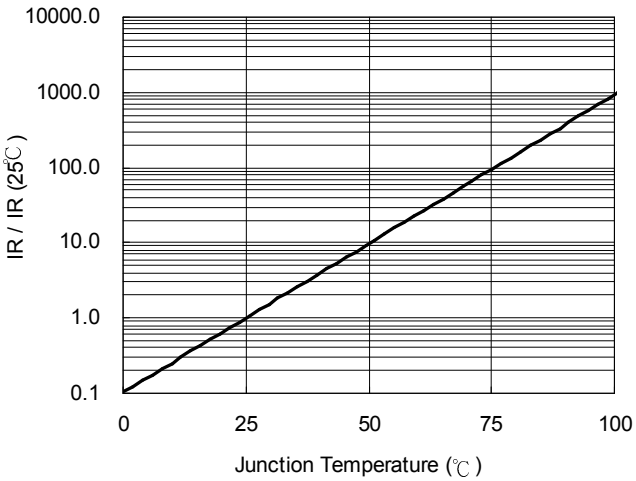


Figure 6. Reverse Leakage Current versus TJ

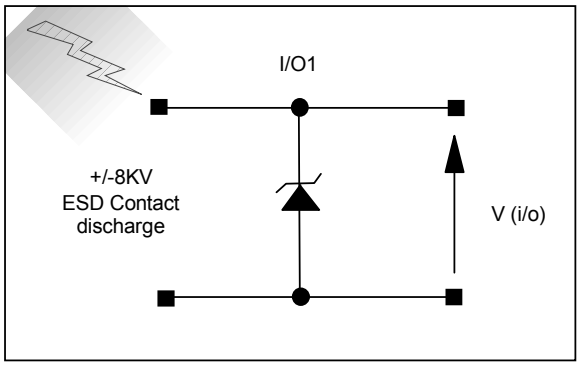


Figure 7. ESD Test Configuration

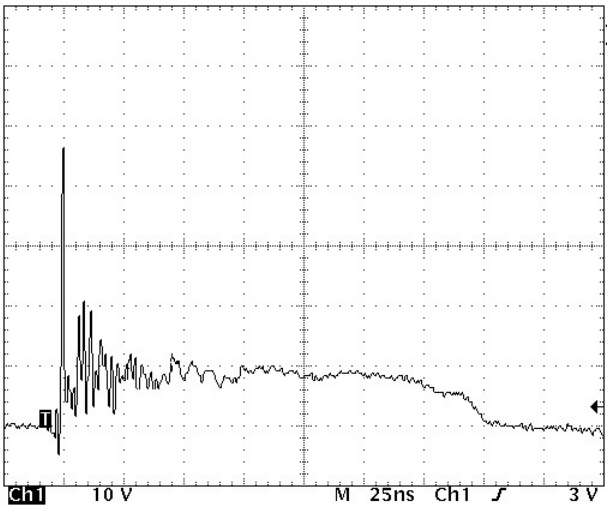


Figure 8. Clamped +8 kV ESD voltage waveform

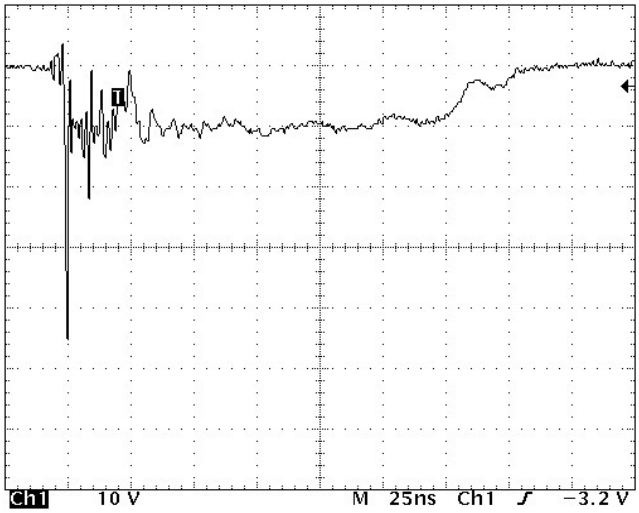
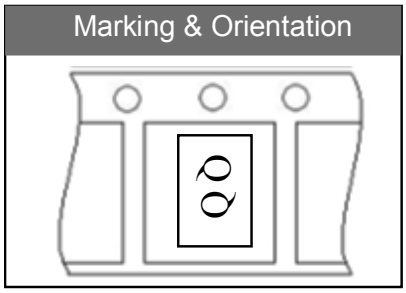


Figure 9. Clamped -8 kV ESD voltage waveform

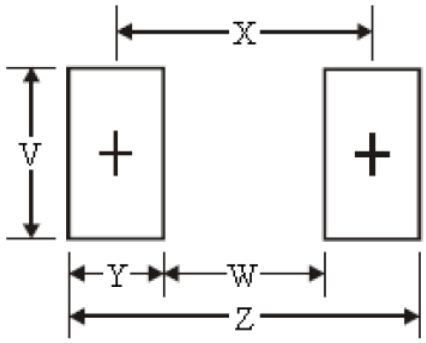
Marking & Orientation



Packaging Information

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L09ESD3V3CE2	10K	7	150K	300K

SOD-882 Soldering Pad Layout



Dim.	Millimeters	Inches
Z	1.30	0.051
X	0.75	0.029
W	0.20	0.007
Y	0.55	0.021
V	0.80	0.031

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