A Product Line of
Diodes Incorporated

PI6C4911504-01

High Performance LVPECL Fanout Buffer

Features

- 4 LVPECL Outputs
- Up to 1.5GHz Output Frequency
- Ultra Low Additive Phase Jitter: < 0.04 ps (typ)
- Two Selectable Inputs
- Low Delay from Input to Output (Tpd typ. < 1.0ns)
- 2.5V / 3.3V Power Supply
- Industrial Temperature Support
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 20-Pin, TSSOP (L)

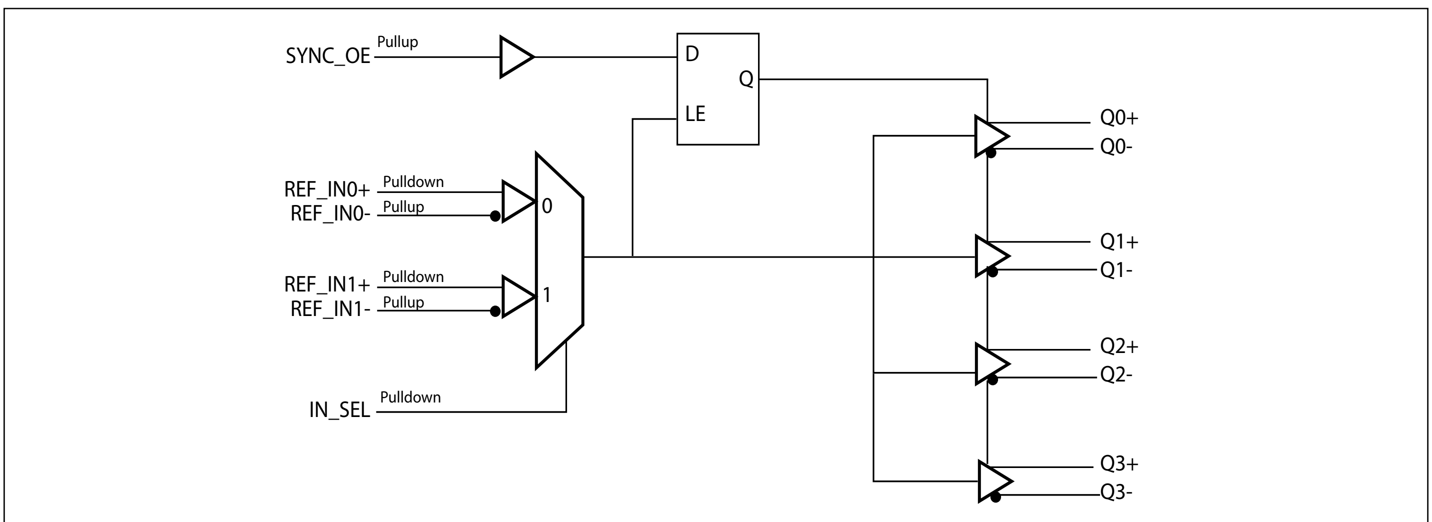
Description

The PI6C4911504-01 is a high performance fanout buffer device which supports up to 1.5GHz frequency. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

Applications

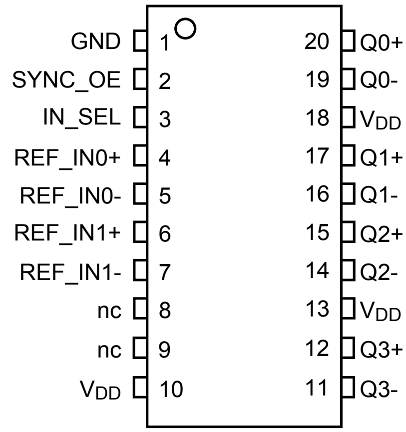
- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin #	Pin Name	Type		Description
1	GND	Power		Ground
2	SYNC_OE	Input	Pullup	Synchronous clock enable. When High, clock outputs follow REF_IN. When low, Q+ outputs are forced low, Q- are forced high
3	IN_SEL	Input	Pulldown	Clock input source selection pin
4, 5	REF_IN0+, REF_IN0-	Input	Pulldown Pullup	Differential clock input 0
6, 7	REF_IN1+, REF_IN1-	Input	Pulldown Pullup	Differential clock input 1
8, 9	NC	-		No connect
10, 13, 18	V_{DD}	Power		Power supply
11, 12	Q3-, Q3+	Output		LVPECL output clock 3
14, 15	Q2-, Q2+	Output		LVPECL output clock 2
16, 17	Q1-, Q1+	Output		LVPECL output clock 1
19, 20	Q0-, Q0+	Output		LVPECL output clock 0

Function Table

Table 1: Clock source input select function

IN_SEL	Function
0	REF_IN0 is the selected reference input
1	REF_IN1 is the selected reference input

Table 2: SYNC_OE select function

SYNC_OE	Function
0	All outputs disabled. Q+ disabled low, Q- disabled High.
1	All outputs enabled.

Pin Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
R_{PULLUP}	Input Pullup Resistor		50		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor		75		kΩ

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested)

Storage Temperature	-55 to +150°C
Supply Voltage to Ground Potential (V_{DD})	-0.5 to +4.65V
Inputs (Referenced to GND)	-0.5 to V_{DD}+0.5V
Clock Output (Referenced to GND)	-0.5 to V_{DD}+0.5V
Latch Up	200mA
ESD Protection (Input)	2000 V min (HBM)
Junction Temperature	125°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage		3.135		3.465	V
			2.375		2.625	V
I_{DD}	Power Supply Current	Outputs unloaded			90	mA
T_A	Ambient Operating Temperature		-40		85	°C

LVCMOS/ LVTTL DC Characteristics

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		$V_{DD} = V_{IN} = 3.465V$	2		V_{DD}+0.3	V
			$V_{DD} = V_{IN} = 2.625V$	1.6		V_{DD}+0.3	V
V_{IL}	Input Low Voltage		$V_{DD} = V_{IN} = 3.465V$	-0.3		0.8	V
			$V_{DD} = V_{IN} = 2.625V$	-0.3		0.6	V
I_{IH}	Input High Current	SYNC_OE	$V_{DD} = V_{IN} = 3.465V$			5	µA
			$V_{DD} = V_{IN} = 2.625V$			5	
		IN_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
			$V_{DD} = V_{IN} = 2.625V$			150	
I_{IL}	Input Low Current	SYNC_OE	$V_{DD} = V_{IN} = 3.465V$	-150			µA
			$V_{DD} = V_{IN} = 2.625V$	-150			
		IN_SEL	$V_{DD} = V_{IN} = 3.465V$	-5			µA
			$V_{DD} = V_{IN} = 2.625V$	-5			

DC Electrical Specifications - Differential Inputs

Symbol	Parameter			Min.	Typ.	Max.	Units
I_{IH}	Input High current	REF_IN-	Input = V_{DD}			5	µA
		REF_IN+	Input = V_{DD}			150	µA
I_{IL}	Input Low current	REF_IN-	Input = GND	-150			µA
		REF_IN+	Input = GND	-5			µA
V_{ID}	Input Differential Amplitude (Vp-p)			0.15		V_{DD}-2.0	V
V_{CM}	Common mode input voltage		REF_IN0	0.5		V_{DD}-0.85	V
			REF_IN1	1.5		V_{DD}	

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage	V_{DD} = 3.3V ± 5%	V_{DD}-1.4		V_{DD}-0.9	V
		V_{DD} = 2.5V ± 5%	V_{DD}-1.6		V_{DD}-0.8	V
V_{OL}	Output Low voltage	V_{DD} = 3.3V ± 5%	V_{DD}-2.0		V_{DD}-1.6	V
		V_{DD} = 2.5V ± 5%	V_{DD}-2.0		V_{DD}-1.5	V
V_{SWING}	Peak to Peak Output Voltage Swing		0.6		1.0	V

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency	LVPECL			1500	MHz
T_r	Output rise time	From 20% to 80%	300	400	600	ps
T_f	Output fall time	From 80% to 20%	300	400	600	ps
T_{ODC}	Output duty cycle	Frequency<650MHz	48		52	%
V_{PP}	Output swing Single-ended	Frequency<650MHz	400			
$T_{addjitter}$	Buffer additive jitter RMS	Using 156.25MHz XO, 0.17ps jitter as source @3.3V		0.05		ps
$T_{Phasejitter}$	Total output jitter RMS	Using 156.25MHz XO, 0.17ps jitter as source @3.3V		0.23		ps
T_{SK}	Output Skew	4 outputs devices, outputs in same tank, with same load, at DUT.		40		ps
T_{PD}	Propagation Delay			1000		ps
T_{OD}	Valid to HiZ				100	ns
T_{OE}	HiZ to valid				100	ns

Notes:

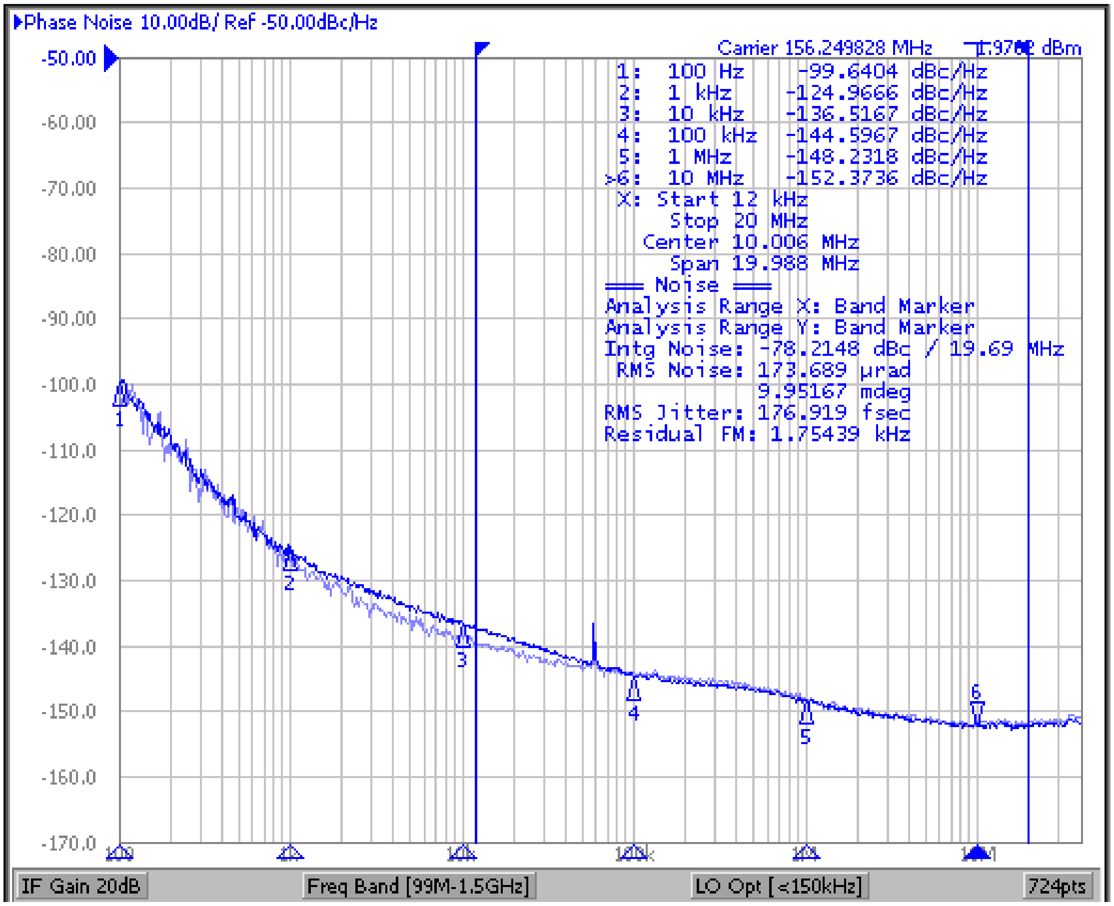
1. This parameter is guaranteed by design

Phase Noise Plots

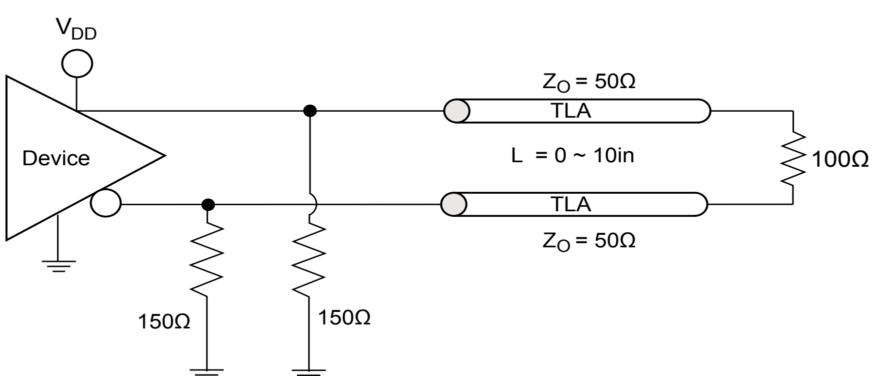
f_{OUT} = 156.25MHz

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

Additive jitter is calculated at 156.25MHz~40fs RMS (12kHz to 20MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$



Configuration Test Load Board Termination for LVPECL



Application Information

Suggest for Unused Inputs and Outputs

LVCMOS Input Control Pins

It is suggested to add pull-up=4.7k and pull-down=1k for LVCMOS pins even though they have internal pull-up/down but with much higher value (>=50k) for higher reliability design.

Differential +IN/-IN Input Pins

They can be left floating if not used. Connect them 1k to GND is optional for the additional protection.

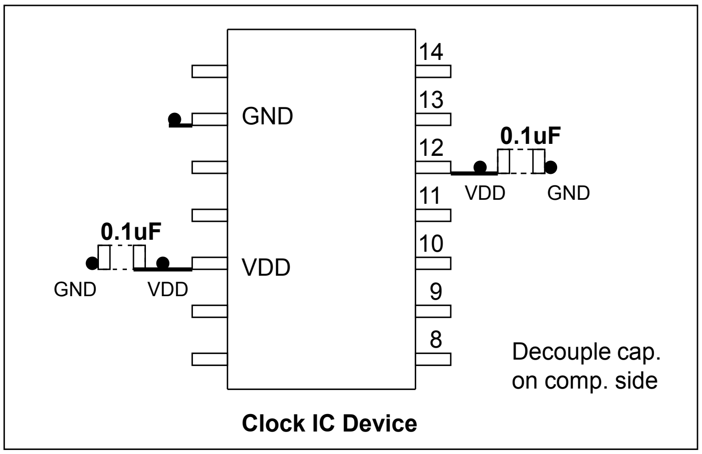
Outputs

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power supply power.

Power Decoupling & Routing

VDD Pin Decoupling

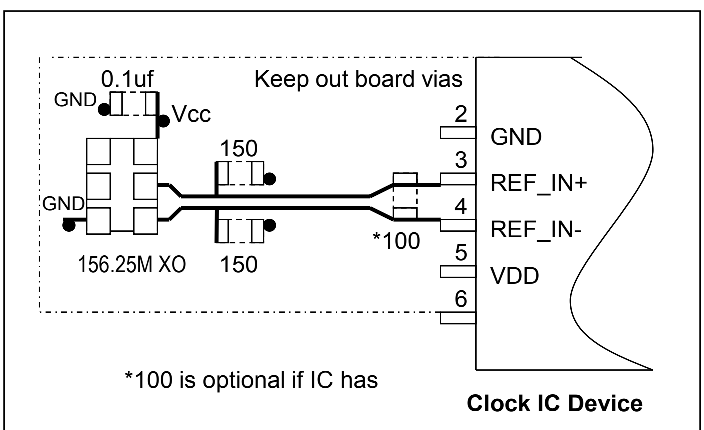
As general design rule, each VDD pin must have a 0.1uF decoupling capacitor. For better decoupling, 1uF can be used. Locating the decoupling capacitor on the component side has better decoupling filter result as shown below.



Placement of Decoupling Caps

Differential Clock Trace Routing

Always route differential signals symmetrically, make sure there is enough keep-out space to the adjacent trace (>20mil.). In 156.25MHz XO drives IC example, it is better routing differential trace on component side as the following.



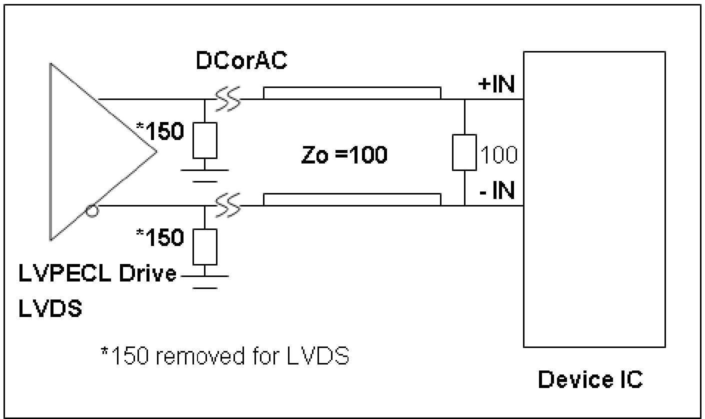
IC Routing for XO Drive

Clock timing is the most important component in PCB design, so its trace routing must be planned and routed as a first priority in manual routing. Some good practices are to use minimum vias (total trace vias count <4), use independent layers with good reference plane and keep other signal traces away from clock traces (>20mil.) etc.

LVPECL and LVDS Input Interface

LVPECL and LVDS DC/ AC Input

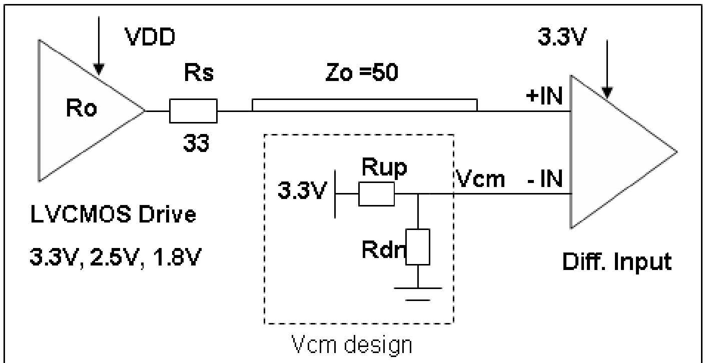
LVPECL and LVDS clock input to this IC is connected as shown below.



LVPECL/ LVDS Input

CMOS Clock DC Drive Input

LVCMOS clock has voltage Voh levels such as 3.3V, 2.5V, 1.8V. CMOS drive requires a Vcm design at the input: Vcm= ½ (CMOS V) as shown below 7. Rs =22 ~33Ω typically.



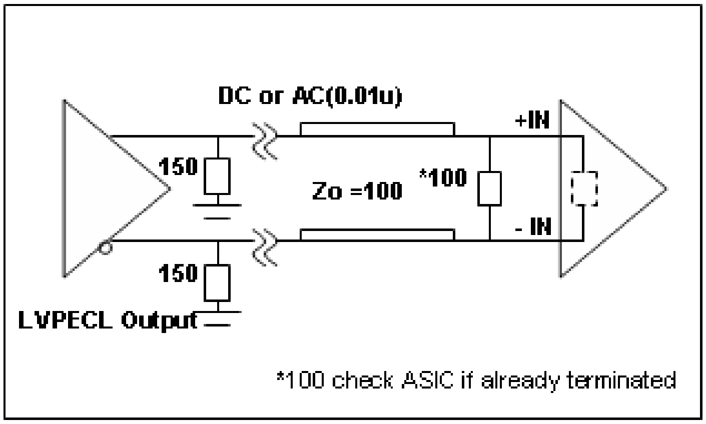
VDD V	Rup	Rdn	Vcm
3.3V	1k	1k	1.65V
2.5V	1k	610	1.25V
1.8V	1k	380	0.9V

CMOS DC Input Vcm Design

Device LVPECL Output Terminations

LVPECL Output Popular Termination

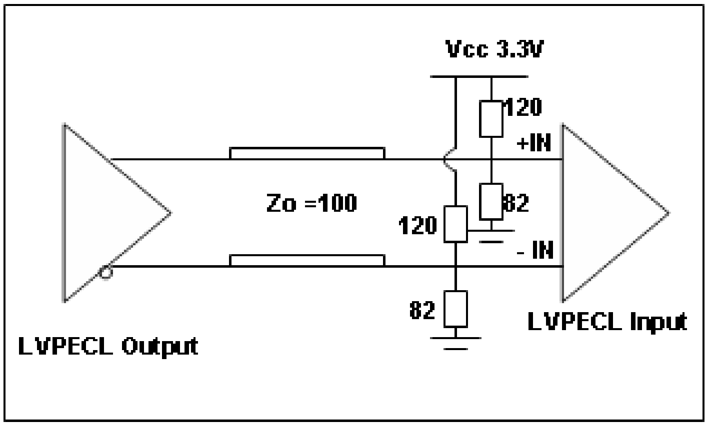
The most popular LVPECL termination is 150Ω pull-down bias and 100Ω across at RX side. Please consult ASIC datasheet if it already has 100Ω or equivalent internal termination. If so, do not connect external 100Ω across as shown in below. This popular termination's advantage is that it does not allow any bias through from Vcc. This prevents Vcc system noise coupling onto clock trace.



LVPECL Output Popular Termination

LVPECL Output Thevenin Termination

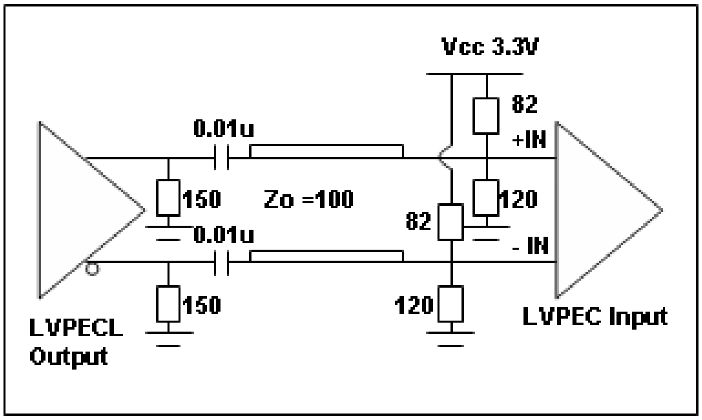
Figure below shows LVPECL output Thevenin termination which is used for shorter trace drive (<5in.), but it takes Vcc bias current and Vcc noise can get onto clock trace. It also requires more component count. So it is seldom used today.



LVPECL Thevenin Output Termination

LVPECL Output AC Thevenin Termination

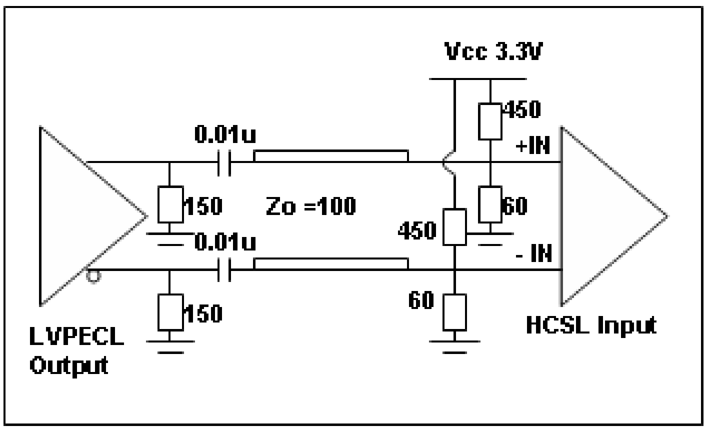
LVPECL AC Thevenin terminations require a 150Ω pull-down before the AC coupling capacitor at the source as shown below. Note that pull-up/down resistor value is swapped compared to previous figure. This circuit is good for short trace (<5in.) application only.



LVPECL Output AC Thenvenin Termination

LVPECL Output Drive HCSL Input

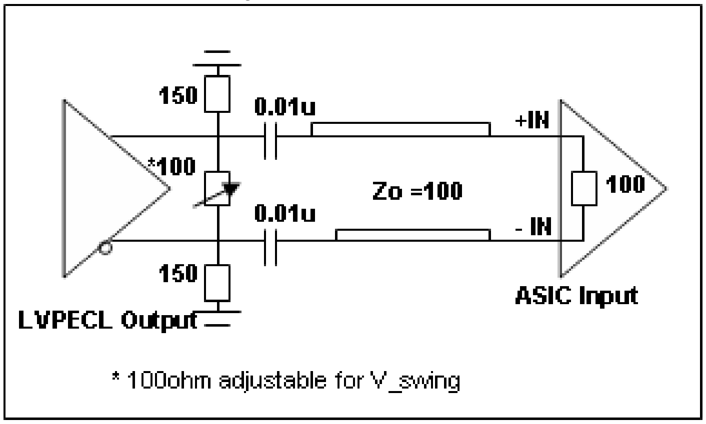
Using the LVPECL output to drive a HCSL input can be done using a typical LVPECL AC Thenvenin termination scheme. Use pull-up/down 450/60Ω to generate Vcm=0.4V for the HCSL input clock. This termination is equivalent to 50Ω load as shown.



LVPECL Output Drive HCSL Termination

LVPECL Output V_swing Adjustment

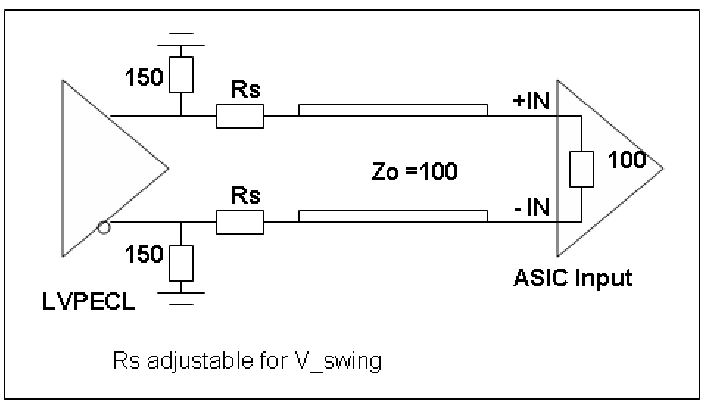
It is suggested to add another cross 100Ω at TX side to tune the LVPECL output V_swing without changing the optimal 150Ω pull-down bias. This form of double termination can reduce the V_swing in ½ of the original at the RX side. By fine tuning the 100Ω resistor at the TX side with larger values like 150 to 200Ω, one can increase the V_swing by > 1/2 ratio.



LVPECL Output V_swing Adjustment

LVPECL V_Swing Adjustment using Rs

Another way to control V_swing is by adding serial Rs. Rs value is tunable between 22 to 33Ω depending on application. This method may reduce the clock drive PCB trace in slower Tr/Tf .



LVPECL V_swing Adjustment using Rs

Clock Jitter Definitions

Total jitter= RJ + DJ

Random Jitter (RJ) is unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related with how long or how many test samples are available. Deterministic Jitter (DJ) is timing jitter that is predictable and periodic in fixed interference frequency. Total Jitter (TJ) is the combination of random jitter and deterministic jitter: , where is a factor based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

Phase Jitter

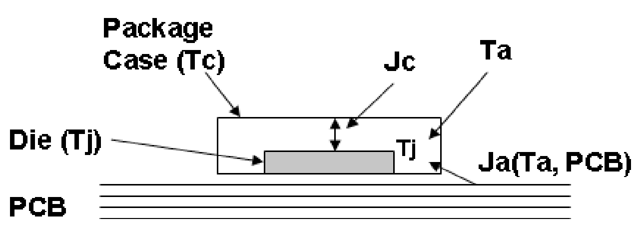
Phase noise is short-term random noise attached on the clock carrier and it is a function of the clock offset from the carrier, for example dBc/Hz@10kHz which is phase noise power in 1-Hz normalized bandwidth vs. the carrier power @10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter, for example, to specify phase jitter <=1ps at 12k to 20MHz offset band as SONET standard specification.

PCIe Ref_CLK Jitter

PCIe reference clock jitter specification requires testing via the PCI-SIG jitter tool, which is regulated by US PCI-SIG organization. The jitter tool has PCIe Serdes embedded filter to calculate the equivalent jitter that relates to data link eye closure. Direct peak-peak jitter or phase jitter test data, normally is higher than jitter measure using PCI-SIG jitter tool. It has high-frequency jitter and low-frequency jitter spec. limit. For more information, please refer to the PCI-SIG website: http://www.pcisig.com/specifications/pciexpress/

Device Thermal Calculation

Figure below shows the JEDEC thermal model in a 4-layer PCB.



JEDEC 4-layer PCB Thermal Model

JEDEC IC Thermal Model

Important factors to influence device operating temperature are:

1) The power dissipation from the chip (P_chip) is after subtracting power dissipation from external loads. Generally it can be the no-load device Idd

2) Package type and PCB stack-up structure, for example, 1oz 4 layer board. PCB with more layers and are thicker has better heat dissipation

3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature Tj

The individual device thermal calculation formula:

Tj =Ta + Pchip x Ja

Tc = Tj - Pchip x Jc

Ja ___ Package thermal resistance from die to the ambient air in C/W unit; This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce Ja (still air) by 20~30%

Jc ___ Package thermal resistance from die to the package case in C/W unit

Tj ___ Die junction temperature in C (industry limit <125C max.)

Ta ___ Ambiant air température in C

Tc ___ Package case temperature in C

Pchip___ IC actually consumes power through Iee/GND current

Thermal calculation example

To calculate Tj and Tc of PI6CV304 in an SOIC-8 package:

Step 1: Go to Diodes web to find Ja=157 C/W, Jc=42 C/W

https://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Step 2: Go to device datasheet to find Idd=40mA max.

I_{DD}	Supply Current	C_L = 33pF/33MHz		20		mA
		C_L = 33pF/66MHz		40		
		C_L = 22pF/80MHz		35		
		C_L = 15pF/100MHz		32		
		C_L = 10pF/125MHz		28		
		C_L = 10pF/155MHz		41		

Step 3: P_total= 3.3Vx40mA=0.132W

Step 4: If Ta=85C

Tj= 85 + Ja xP_total= 85+25.9 = 105.7C

Tc= Tj + Jc xP_total= 105.7- 5.54 = 100.1C

Note:

The above calculation is directly using Idd current without subtracting the load power, so it is a conservative estimation. For more precise thermal calculation, use P_unload or P_chip from device Iee or GND current to calculate Tj, especially for LVPECL buffer ICs that have a 150Ω pull-down and equivalent 100Ω differential RX load.

Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	84.0 ^{O}C/W
Θ_{JC}	Junction-to-case thermal resistance		17.0 ^{O}C/W

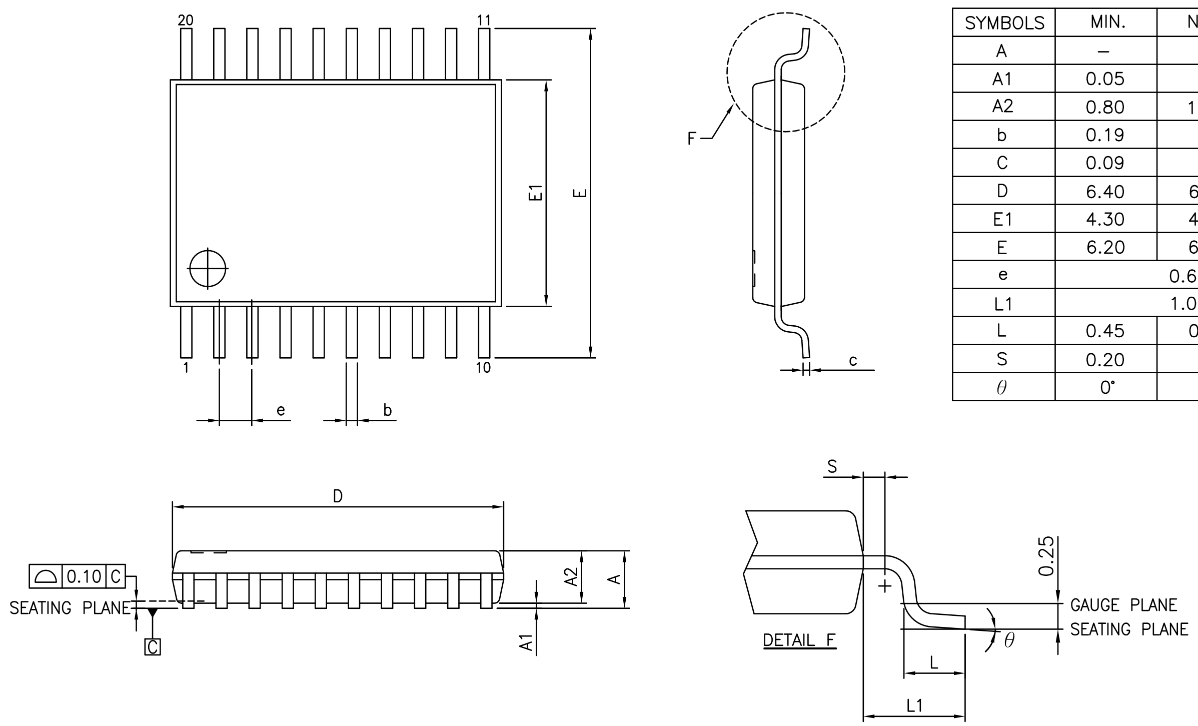
Part Marking

PI6C4911
504-01LIE
YYWWX$\overline{X}$

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical

20-TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 03/31/16

DESCRIPTION: 20-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L20)

DOCUMENT CONTROL #: PD-1311 REVISION: G

16-0074

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description	Operating Temperature
PI6C4911504-01LIEX	L	20-Pin, 173mil Wide (TSSOP)	-40 to 85 °C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

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