

3.3V Very Low Power 8-Output PCIe Clock Generator With On-chip Termination

Features

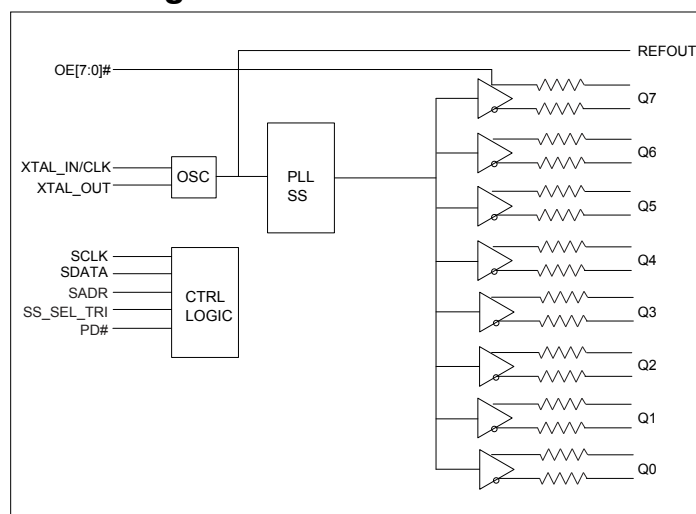
- 3.3V Supply Voltage
- Crystal/CMOS input: 25 MHz
- 8 differential low power HCSL outputs with on-chip termination
- Default $Z_{OUT} = 100\Omega$
- Individual output enable
- Reference CMOS output
- Programmable slew rate and output amplitude for each output
- Differential outputs blocked until PLL is locked
- Selectable 0%, -0.25% or -0.5% spread on differential outputs
- Strapping pins or SMBus for configuration
- Differential Output-To-Output Skew <60ps
- Very-Low Jitter Outputs
 - Differential Cycle-To-Cycle Jitter <50ps
 - PCIe Gen1/Gen2/Gen3/Gen4/Gen5 Compliant
 - CMOS REFOUT Phase Jitter
 - < 0.3ps RMS, SSC off
 - <1.5ps RMS, SSC on
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green): 48-lead 6×6mm TQFN

Description

The PI6CG33801C is an 8-output very low power PCIe Gen1/Gen2/Gen3/Gen4/Gen5 clock generator. It uses 25MHz crystal or CMOS reference as an input to generate the 100MHz low power differential HCSL outputs with on-chip terminations. The on-chip termination can save 32 external resistors and make layout easier. An additional buffered reference output is provided to serve as a low noise reference for other circuitry.

It uses Diodes' proprietary PLL design to achieve very low jitter that meets PCIe Gen1/Gen2/Gen3/Gen4/Gen 5 requirements. It also provides various options such as different slew rate and amplitude through SMBUS so that users can configure the device easily to get the optimized performance for their individual boards. The device also supports selectable spread-spectrum options to reduce EMI for various applications.

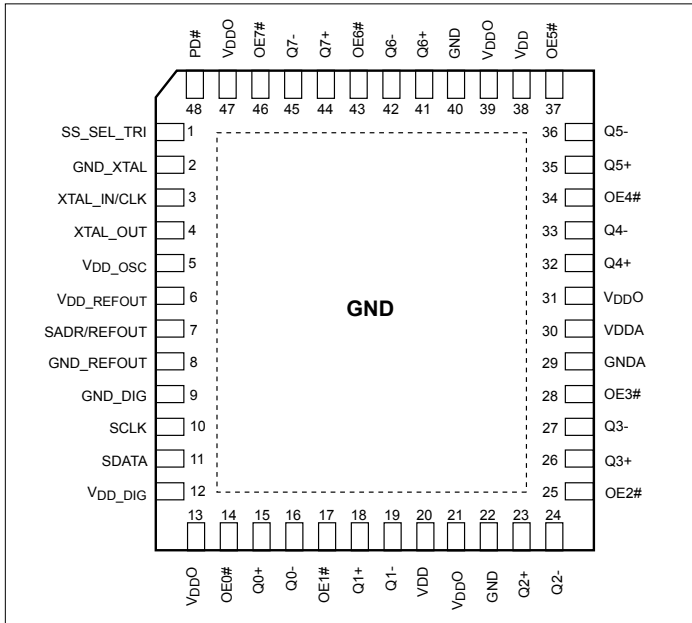
Block Diagram



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

| Pin # | Pin Name | Type | | Description |
|--------------------|-------------|------------------|-----------|--|
| 1 | SS_SEL_TRI | Input | Tri-level | Latched select input to select spread spectrum amount at initial power up. 1 = -0.5% spread, M = Spread Off, 0 = Spread Off. This pin has both internal pull-up and pull-down. Refer to SMBUS byte_1 bit 4, 3 = '01' to get -0.25% spread. |
| 2 | GND_XTAL | Power | | Ground for oscillator circuit |
| 3 | XTAL_IN/CLK | Input | | Crystal input or CMOS reference input |
| 4 | XTAL_OUT | Output | | Crystal output |
| 5 | VDD_OSC | Power | | Power supply for oscillator circuitry, nominal 3.3V |
| 6 | VDD_REFOUT | Power | | Power supply for buffered CMOS output |
| 7 | SADR/REFOUT | Input/ Output | CMOS | Latch to select SMBus Address or LVC MOS REFOUT. This pin has an internal pull-down |
| 8 | GND_REFOUT | Power | | Ground for REFOUT |
| 9 | GND_DIG | Power | | Ground for digital circuitry |
| 10 | SCLK | Input | CMOS | SMBUS clock input, 3.3V tolerant |
| 11 | SDATA | Input/ Output | CMOS | SMBUS Data line, 3.3V tolerant |
| 12 | VDD_DIG | Power | | Power supply for digital circuitry, nominal 3.3V |
| 13, 21, 31, 39, 47 | VDDO | Power | | Power supply for differential outputs |
| 14 | OE0# | Input | CMOS | Active low input for enabling Q0 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 15 | Q0+ | Output | HCSL | Differential true clock output |

Pin Description Cont.

| Pin # | Pin Name | Type | | Description |
|--------|------------------|--------|------|---|
| 16 | Q0- | Output | HCSL | Differential complementary clock output |
| 17 | OE1# | Input | CMOS | Active low input for enabling Q1 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 18 | Q1+ | Output | HCSL | Differential true clock output |
| 19 | Q1- | Output | HCSL | Differential complementary clock output |
| 20, 38 | V _{DD} | Power | | Power supply, nominal 3.3V |
| 22, 40 | GND | Power | | Ground |
| 23 | Q2+ | Output | HCSL | Differential true clock output |
| 24 | Q2- | Output | HCSL | Differential complementary clock output |
| 25 | OE2# | Input | CMOS | Active low input for enabling Q2 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 26 | Q3+ | Output | HCSL | Differential true clock output |
| 27 | Q3- | Output | HCSL | Differential complementary clock output |
| 28 | OE3# | Input | CMOS | Active low input for enabling Q3 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 29 | GNDA | Power | | Ground for analog circuitry |
| 30 | V _{DDA} | Power | | Power supply for analog circuitry |
| 32 | Q4+ | Output | HCSL | Differential true clock output |
| 33 | Q4- | Output | HCSL | Differential complementary clock output |
| 34 | OE4# | Input | CMOS | Active low input for enabling Q4 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 35 | Q5+ | Output | HCSL | Differential true clock output |
| 36 | Q5- | Output | HCSL | Differential complementary clock output |
| 37 | OE5# | Input | CMOS | Active low input for enabling Q5 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 41 | Q6+ | Output | HCSL | Differential true clock output |
| 42 | Q6- | Output | HCSL | Differential complementary clock output |
| 43 | OE6# | Input | CMOS | Active low input for enabling Q6 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 44 | Q7+ | Output | HCSL | Differential true clock output |
| 45 | Q7- | Output | HCSL | Differential complementary clock output |
| 46 | OE7# | Input | CMOS | Active low input for enabling Q7 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 48 | PD# | Input | CMOS | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |

SMBus Address Selection Table

| | SADR | Address | +Read/Write Bit |
|---|------|---------|-----------------|
| State of SADR on first application of PD# | 0 | 1101000 | X |
| | 1 | 1101010 | X |

Power Management Table⁽³⁾

| PD# | SMBus OE bit | OEn# | Qn+ | Qn- | REFOUT |
|-----|--------------|------|-------------------------|-------------------------|-------------------------|
| 0 | X | X | Low ⁽¹⁾ | Low ⁽¹⁾ | HiZ ⁽²⁾ |
| 1 | 1 | 0 | Running | Running | Running |
| 1 | 1 | 1 | Disabled ⁽¹⁾ | Disabled ⁽¹⁾ | Running |
| 1 | 0 | X | Disabled ⁽¹⁾ | Disabled ⁽¹⁾ | Disabled ⁽⁴⁾ |

Note:

1. The output state is set by B11[1:0] (Low/Low default)
2. REF is Hi-Z until the 1st assertion of PD# high. After this, when PD# is low, REF is disabled. If Byte3, bit 5 = 1, then REF is running
3. Input High/ Low defined at default values for device
4. See SMBUs Byte 3, bit 4

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| | |
|--|--|
| Storage Temperature..... | -65°C to +150°C |
| Supply Voltage to Ground Potential, V_{DDxx} | -0.5V to +4.6V |
| Input Voltage | -0.5V to $V_{DD}+0.5V$, not exceed 4.6V |
| SMBus, Input High Voltage | 3.6V |
| ESD Protection (HBM) | 2000 V |
| Max Junction Temperature | +125°C |

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A ; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|--|---|---|-------|------|-------|-------|
| $V_{DD}, V_{DDA}, V_{DD_OSC}, V_{DD_DIG},$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Power Supply Voltage | | 1.0 | 3.3 | 3.465 | V |
| $V_{DD_RE-FOUT}$ | Reference Output Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DDA} | Analog Power Supply Current | All outputs active @100MHz | | 22 | 25 | mA |
| I_{DD} | Power Supply Current | All V_{DD} , except V_{DDA} and V_{DDO} , All outputs active @100MHz | | 20 | 25 | mA |
| I_{DDO} | Power Supply Current for Outputs ⁽³⁾ | All outputs active @100MHz | | 29 | 34 | mA |
| I_{DDA_WL} | Analog Power Supply Wake-on-LAN ⁽¹⁾ Current | Q outputs off, REF output running | | 0.5 | 1 | mA |
| I_{DD_WL} | Power Supply Wake-on-LAN ⁽¹⁾ Current | All V_{DD} , except V_{DDA} and V_{DDO} , Q outputs off, REF output running | | 3 | 6 | mA |
| I_{DDO_WL} | Power Supply Wake-on-LAN ⁽¹⁾ Current for Outputs | Q outputs off, REF output running | | 0.04 | 0.1 | mA |
| I_{DDA_PD} | Analog Power Supply Power Down ⁽²⁾ Current | All outputs off | | 0.5 | 1 | mA |
| I_{DD_PD} | Power Supply Power Down ⁽²⁾ Current | All outputs off | | 1 | 2 | mA |
| I_{DDO_PD} | Power Supply Current Power Down ⁽²⁾ for Outputs | All outputs off | | 0.05 | 0.1 | mA |
| T_A | Ambient Temperature | Industrial grade | -40 | | 85 | °C |

Note:

1. Wake-on-LAN mode: PD# = '0' Byte 3, bit 5 = '1'
2. Power down mode: PD# = '0' Byte 3, bit 5 = '0'
3. Output drive 5 inch trace.

Input Electrical Characteristics

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|-------------------|---|------------|------|------|------|-------|
| R _{pu} | Internal pull up resistance | | | 120 | | KΩ |
| R _{dn} | Internal pull down resistance | | | 120 | | KΩ |
| C _{XTAL} | Internal capacitance on X_IN and X_OUT pins | | | 8 | | pF |
| L _{PIN} | Pin inductance | | | | 7 | nH |

Crystal Characteristic

| Parameters | Description | Min. | Typ | Max. | Units |
|--------------------|------------------------------|-------------|-----|------|-------|
| OSCmode | Mode of Oscillation | Fundamental | | | |
| FREQ | Frequency | | 25 | | MHz |
| ESR ⁽¹⁾ | Equivalent Series Resistance | | | 50 | Ω |
| C _{load} | Load Capacitance | | 8 | | pF |
| C _{shunt} | Shunt Capacitance | | | 7 | pF |
| | Drive Level | | | 200 | uW |

Note:

1. ESR value is dependent upon frequency of oscillation

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|----------------------|---------------------------|--|----------------------------|------|------|-------|
| V _{DDSMB} | Nominal bus voltage | | 2.7 | | 3.6 | V |
| V _{IHSMB} | SMBus Input High Voltage | SMBus, V _{DDSMB} = 3.3V | 2.1 | | 3.6 | V |
| | | SMBus, V _{DDSMB} < 3.3V | 0.65 V _{DDSMB} | | | |
| V _{ILSMB} | SMBus Input Low Voltage | SMBus, V _{DDSMB} = 3.3V | | | 0.8 | V |
| | | SMBus, V _{DDSMB} < 3.3V | | | 0.8 | |
| I _{SMBSINK} | SMBus sink current | SMBus, at V _{OLSMB} | 4 | | | mA |
| V _{OLSMB} | SMBus Output Low Voltage | SMBus, at I _{SMBSINK} | | | 0.4 | V |
| f _{MAXSMB} | SMBus operating frequency | Maximum frequency | | | 500 | kHz |
| t _{RMSB} | SMBus rise time | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | | 1000 | ns |
| t _{FMSB} | SMBus fall time | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | | 300 | ns |

Spread Spectrum Characteristic

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|------------------|-------------------------|-----------------------|------|------|------|-------|
| f _{MOD} | SS Modulation Frequency | Triangular modulation | 30 | 31.8 | 33 | kHz |

LVC MOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|------------------|-----------------------|--|-------------------------------------|--------------------|-------------------------------------|-------|
| V _{IH} | Input High Voltage | Single-ended inputs, except SMBus | 0.75 V _{DD} | | V _{DD} +0.3 | V |
| V _{IM} | Input Mid Voltage | SS_SEL_TRI | 0.4V _{DD} | 0.5V _{DD} | 0.6V _{DD} | V |
| V _{IL} | Input Low Voltage | Single-ended inputs, except SMBus | -0.3 | | 0.25 V _{DD} | V |
| I _{IH} | Input High Current | Single-ended inputs, V _{IN} = V _{DD} | | | 5 | μA |
| I _{IL} | Input Low Current | Single-ended inputs, V _{IN} = 0V | -5 | | | μA |
| I _{IH} | Input High Current | Single-ended inputs with pull up / pull down resistor, V _{IN} = V _{DD} | | | 50 | μA |
| I _{IL} | Input Low Current | Single-ended inputs with pull up / pull down resistor, V _{IN} = 0V | -50 | | | μA |
| V _{OH} | Output High Voltage | REFOUT, except SMBus; I _{OH} = -2mA | 0.8 x V _{DD_} REFOUT | | | V |
| V _{OL} | Output Low Voltage | REFOUT, except SMBus; I _{OL} = 2mA | | | 0.2 x V _{DD_} REFOUT | V |
| R _{OUT} | CMOS Output impedance | | | 20 | | Ω |
| C _{IN} | Input Capacitance | | 1.5 | | 5 | pF |

LVCMOS AC Characteristics

Temperature = T_A ; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---------------------|--|---|------|------|------|--------|
| f_{INPUT} | Input Frequency | XTAL_IN/CLK | | 25 | | MHz |
| t_{RIN} | Input rise time | Single-ended inputs | | | 5 | ns |
| t_{FIN} | Input fall time | Single-ended inputs | | | 5 | ns |
| t_{STAB} | Clock stabilization | From Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.75 | 1 | ms |
| t_{OELAT} | Output enable latency | Q start after OE# assertion Q stop after OE# deassertion | 1 | | 3 | clocks |
| t_{PDLAT} | PD# de-assertion | Differential outputs enable after PD# de-assertion | | 25 | 300 | us |
| t_{PERIOD} | REFOUT clock period | REFOUT, assume input is at 25MHz | | 40 | | ns |
| f_{ACC} | REFOUT frequency accuracy ⁽¹⁾ | REFOUT, long term accuracy to input | | 0 | | ppm |
| t_{SLEW} | REFOUT slew rate ⁽¹⁾ | Byte 3 = 1F, 20% to 80% of V_{DDREF} | 0.9 | 1.4 | 2 | V/ns |
| | | Byte 3 = 5F, 20% to 80% of V_{DDREF} | 1.5 | 2.4 | 3.2 | V/ns |
| | | Byte 3 = 9F, 20% to 80% of V_{DDREF} | 2 | 3 | 3.8 | V/ns |
| | | Byte 3 = DF, 20% to 80% of V_{DDREF} | 2.3 | 3.2 | 4 | V/ns |
| t_{DC} | REFOUT Duty Cycle ⁽¹⁾ | $V_T = V_{\text{DD}} / 2$ V, driven by a Xtal | 45 | 50 | 55 | % |
| t_{DCDIS} | REFOUT Duty Cycle Distortion | $V_T = V_{\text{DD}} / 2$ V, driven by an external source | -2 | 0 | +2 | % |
| t_{JITCC} | REFOUT cycle-cycle jitter | $V_T = V_{\text{DD}} / 2$ V, driven by a Xtal | | 70 | 150 | ps |
| t_{JITPH} | REFOUT Phase Jitter, RMS | 12kHz to 5MHz, SSC off, driven by a Xtal | | 0.16 | 0.3 | ps |
| | | 12kHz to 5MHz, SSC on, driven by a Xtal | | 0.9 | 1.5 | ps |
| t_{JITN} | Noise floor | 1kHz offset, driven by a Xtal | | -149 | -135 | dBc/Hz |
| | | 10kHz offset to Nyquist, driven by a Xtal | | -158 | -140 | dBc/Hz |

Note:

1. Guaranteed by design and characterization, not 100% tested in production

HCSL Output Characteristics

Temperature = T_A ; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|------------|--|---|------|------|------|-------|
| V_{OH} | Output Voltage High ⁽¹⁾ | Statistical measurement on single-ended signal using oscilloscope math function | 660 | 784 | 850 | mV |
| V_{OL} | Output Voltage Low ⁽¹⁾ | | -150 | | 150 | mV |
| V_{OMAX} | Output Voltage Maximum ⁽¹⁾ | Measurement on single ended signal using absolute value | | 816 | 1150 | mV |
| V_{OMIN} | Output Voltage Minimum ⁽¹⁾ | | -300 | -42 | | mV |
| V_{OC} | Output Cross Voltage ^(1,2,4) | | 250 | 430 | 550 | mV |
| DV_{OC} | V_{OC} Magnitude Change ^(1,2,5) | | | 30 | 140 | mV |

Note:

1. At default SMBUS amplitude settings
2. Guaranteed by design and characterization, not 100% tested in production
3. Measured from differential waveform
4. This one is defined as voltage where $Q+ = Q-$ measured on a component test board and only applied to the differential rising edge
5. The total variation of all V_{cross} measurements in any particular system. This is a subset of $V_{cross_min/max}$ allowed.

HCSL Output AC Characteristics

Temperature = T_A ; Supply voltages per normal operation conditions; See test circuits for the load conditions

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|-------------|--|-----------------------------------|------|------|------|-------|
| f_{OUT} | Output Frequency | | | 100 | | MHz |
| t_{RF} | Slew rate ^(1,2,3) | Scope averaging on fast setting | 2.5 | 3.2 | 4 | V/ns |
| | | Scope averaging on slow setting | 2.2 | 3 | 3.7 | V/ns |
| D_{tRF} | Slew rate matching ^(1,2,4) | Scope averaging on | | 7 | 15 | % |
| t_{DC} | Duty Cycle ^(1,2) | Measured differentially, PLL Mode | 45 | 50 | 55 | % |
| t_{SKEW} | Output Skew ^(1,2) | Averaging on, $V_T = 50\%$ | | 20 | 60 | ps |
| t_{j_c-c} | Cycle to cycle jitter ^(1,2) | | | 20 | 50 | ps |

HC SL Output AC Characteristics Cont.

| Symbol | Parameters | Condition | Min. | Typ. | Max | Spec Limit | Units |
|-------------------------|--|---|------|------|------|------------|---------|
| t _{JPHASE} | Integrated Phase Jitter (RMS) ^(1,5) | PCIe Gen 1 ⁽⁶⁾ | | 20 | 30 | 86 | ps(p-p) |
| | | PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz | | 0.08 | 0.1 | 3.0 | ps |
| | | PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz) | | 0.99 | 1.3 | 3.1 | ps |
| | | PCIe Gen3 Common Clock Architecture (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | | 0.32 | 0.42 | 1.0 | ps |
| | | PCIe Gen3 Separate Reference No Spread (PLL BW of 2-4 or 2-5MHz, CDR =10 MHz) | | 0.16 | 0.21 | 0.7 | ps |
| | | PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | | 0.32 | 0.4 | 0.5 | ps |
| | | PCIe Gen 5 ⁽⁷⁾ (PLL BW of 500k to 1.8MHz. CDR = 20MHz) | | 0.02 | 0.05 | 0.15 | ps |
| t _{JPH-SRISG2} | Integrated Phase Jitter (RMS), -0.25% Spread | PCIe Gen 2, Separate Reference Independent Spread (PLL BW of 16MHz, CDR=5MHz) | | 0.6 | 0.92 | 2 | ps |
| t _{JPH-SRISG3} | Integrated Phase Jitter (RMS), -0.25% Spread | PCIe Gen 3, Separate Reference Independent Spread (PLL BW of 2-4MHz or 2-5MHz, CDR=10MHz) | | 0.32 | 0.4 | 0.7 | ps |
| t _{JPH-SRISG2} | Integrated Phase Jitter (RMS), -0.5% Spread | PCIe Gen 2, Separate Reference Independent Spread (PLL BW of 16MHz, CDR=5MHz) | | 0.8 | 1.1 | 2 | ps |
| t _{JPH-SRISG3} | Integrated Phase Jitter (RMS), -0.5% Spread | PCIe Gen 3, Separate Reference Independent Spread (PLL BW of 2-4MHz or 2-5MHz, CDR=10MHz) | | 0.35 | 0.6 | 0.7 | ps |

Note:

1. Guaranteed by design and characterization—not 100% tested in production.
2. Measured from differential waveform.
3. Slew rate is measured through the V_{swing} voltage range centered around differential 0V, within ±150mV window.
4. It is measured using a ±75mV window centered on the average cross point.
5. See <http://www.pcisig.com> for complete specs.
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10⁻¹².
7. PCIe Gen 5 v0.9 specification.

Differential Output Clock Periods - Spread Spectrum Disabled

| Center Freq. MHz | Measurement Window | | | | | | | Units |
|------------------|------------------------|---------------------------|-------------------------|----------------------|-------------------------|---------------------------|------------------------|-------|
| | 1 clock | 1 us | 0.1 s | 0.1 s | 0.1 s | 1 us | 1 clock | |
| | -c2c jitter AbsPer Min | - SSC Short-term Avg. Min | -ppm Long-term Avg. min | 0 ppm Period Nominal | +ppm Long-term Avg. max | + SSC Short-term Avg. Max | -c2c jitter AbsPer Max | |
| 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns |

Differential Output Clock Periods - Spread Spectrum Enabled

| Center Freq. MHz | Measurement Window | | | | | | | Units |
|------------------|------------------------|---------------------------|-------------------------|----------------------|-------------------------|---------------------------|------------------------|-------|
| | 1 clock | 1 us | 0.1 s | 0.1 s | 0.1 s | 1 us | 1 clock | |
| | -c2c jitter AbsPer Min | - SSC Short-term Avg. Min | -ppm Long-term Avg. min | 0 ppm Period Nominal | +ppm Long-term Avg. max | + SSC Short-term Avg. Max | -c2c jitter AbsPer Max | |
| 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns |

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. All long term accuracy and clock period specifications are guaranteed assuming REF is trimmed to 25.00MHz

SMBus Serial Data Interface

PI6CG33801C is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|----|------|----|-----|
| 1 | 1 | 0 | 1 | 0 | SADR | 0 | 1/0 |

Note: SMBus address is latched on SADR pin

How to Write

| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | | 8 bits | 1 bit | 1 bit |
|-----------|--------|-------|-------|-----------------------------|-------|---------------------|-------|-------------------------|-------|-------|-------------------|-------|----------|
| Start bit | Add. | W(0) | Ack | Beginning Byte location = N | Ack | Data Byte count = X | Ack | Beginning Data Byte (N) | Ack | | Data Byte (N+X-1) | Ack | Stop bit |

How to Read

| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit |
|-----------|---------|-------|-------|-----------------------------|-------|------------------|---------|-------|-------|---------------------|-------|-------------------------|-------|
| Start bit | Address | W(0) | Ack | Beginning Byte location = N | Ack | Repeat Start bit | Address | R(1) | Ack | Data Byte count = X | Ack | Beginning Data Byte (N) | Ack |

| | 8 bits | 1 bit | 1 bit |
|-------|-------------------|-------|----------|
| | Data Byte (N+X-1) | NAck | Stop bit |

Byte 0: Output Enable Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|------------------|------|--------------------|--------------|-------------|
| 7 | Q7_OE | Q7 output enable | RW | 1 | See B11[1:0] | Pin Control |
| 6 | Q6_OE | Q6 output enable | RW | 1 | | Pin Control |
| 5 | Q5_OE | Q5 output enable | RW | 1 | | Pin Control |
| 4 | Q4_OE | Q4 output enable | RW | 1 | | Pin Control |
| 3 | Q3_OE | Q3 output enable | RW | 1 | | Pin Control |
| 2 | Q2_OE | Q2 output enable | RW | 1 | | Pin Control |
| 1 | Q1_OE | Q1 output enable | RW | 1 | | Pin Control |
| 0 | Q0_OE | Q0 output enable | RW | 1 | | Pin Control |

Note:

1. A low on these bits will override the OE# pins and force the differential outputs to the state indicated by B11[1:0] (Low/ Low default)

Byte 1: SS Spread Spectrum and Control Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|---------------------------|-------------------|--------------------|--|-------------------------------------|
| 7 | SSENRB1 | SS Enable Readback Bit1 | R | Latch | '00' for SS_SEL_TRI = '0', '10' for SS_SEL_TRI = 'M' '11' for SS_SEL_TRI = '1' | |
| 6 | SSENRB0 | SS Enable Readback Bit0 | R | Latch | | |
| 5 | SSEN_SWCTR | Enable SW control of SS | RW | 0 | Values in B1[7:6] control SS amount | Values in B1[4:3] control SS amount |
| 4 | SSENSW1 | SS enable SW control Bit1 | RW ⁽¹⁾ | 0 | '00' = SS off, '01' = -0.25% SS, '10' = SS off, '11' = -0.5% SS | |
| 3 | SSENSW0 | SS enable SW control Bit0 | RW ⁽¹⁾ | 0 | | |
| 2 | Reserved | | | 1 | | |
| 1 | Amplitude1 | Control output amplitude | RW | 1 | '00' = 0.6V, '01' = 0.68V, '10' = 0.75V, '11' = 0.85V | |
| 0 | Amplitude0 | | RW | 0 | | |

Note:
1. Spread must be selected OFF or ON with the hardware latch pin. These bits should not be used to turn spread ON or OFF after power up. These bits can be used to change the spread amount, and B1[5] must be set to a 1 for these bits to have any effect on the part. If These bits are used to turn spread OFF or ON, the system will need to be reset.

Byte 2: Differential Output Slew Rate Control Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|-------------------------|------|--------------------|--------------|--------------|
| 7 | SLEWRATECTR_Q7 | Control slew rate of Q7 | RW | 1 | Slow setting | Fast setting |
| 6 | SLEWRATECTR_Q6 | Control slew rate of Q6 | RW | 1 | Slow setting | Fast setting |
| 5 | SLEWRATECTR_Q5 | Control slew rate of Q5 | RW | 1 | Slow setting | Fast setting |
| 4 | SLEWRATECTR_Q4 | Control slew rate of Q4 | RW | 1 | Slow setting | Fast setting |
| 3 | SLEWRATECTR_Q3 | Control slew rate of Q3 | RW | 1 | Slow setting | Fast setting |
| 2 | SLEWRATECTR_Q2 | Control slew rate of Q2 | RW | 1 | Slow setting | Fast setting |
| 1 | SLEWRATECTR_Q1 | Control slew rate of Q1 | RW | 1 | Slow setting | Fast setting |
| 0 | SLEWRATECTR_Q0 | Control slew rate of Q0 | RW | 1 | Slow setting | Fast setting |

Byte 3: REF Control Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|----------------------------|------|--------------------|--|---------------------------|
| 7 | REFSLEWRATE | Slew rate control for REF | RW | 0 | '00' = 1.4V/ns '01' = 2.4V/ns, '10' = 3V/ns, '11' = 3.2V/ns | |
| 6 | | | RW | 1 | | |
| 5 | REF_PDSTATE | Wake-on-Lan enable for REF | RW | 0 | REF = Disabled in PD state ⁽¹⁾ | REF = running in PD state |
| 4 | REF_OE | Output enable for REF | RW | 1 | REF = Disabled ⁽¹⁾ | REF = running |
| 3 | Reserved | | | 1 | | |
| 2 | Reserved | | | 1 | | |
| 1 | Reserved | | | 1 | | |
| 0 | Reserved | | | 1 | | |

Note:

1. The disabled state depends on Byte11[1:0]. '00' = Low, '01'=HiZ, '10'=Low, '11'=High

Byte 4: Reserved

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|-------------|------|--------------------|---|---|
| 7:0 | Reserved | | | 0x40 | | |

Byte 5: Revision and Vendor ID Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|-------------|------|--------------------|---------------|---|
| 7 | RID3 | Revision ID | R | 0 | rev = 0000 | |
| 6 | RID2 | | R | 0 | | |
| 5 | RID1 | | R | 0 | | |
| 4 | RID0 | | R | 0 | | |
| 3 | PVID3 | Vendor ID | R | 0 | Diodes = 0011 | |
| 2 | PVID2 | | R | 0 | | |
| 1 | PVID1 | | R | 1 | | |
| 0 | PVID0 | | R | 1 | | |

Byte 6: Device Type/Device ID Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|-------------|------|--------------------|---|---|
| 7 | DTYPE1 | Device type | R | 0 | '00' = CG, '01' = ZDB, '10' = Reserve, '11' = NZDB | |
| 6 | DTYPE0 | | R | 0 | | |
| 5 | DID5 | Device ID | R | 0 | 001000 binary, 08Hex | |
| 4 | DID4 | | R | 0 | | |
| 3 | DID3 | | R | 1 | | |
| 2 | DID2 | | R | 0 | | |
| 1 | DID1 | | R | 0 | | |
| 0 | DID0 | | R | 0 | | |

Byte 7: Byte Count Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|------------------------|------|--------------------|--|---|
| 7 | Reserved | | | 0 | | |
| 6 | Reserved | | | 0 | | |
| 5 | Reserved | | | 0 | | |
| 4 | BC4 | Byte count programming | RW | 0 | Writing to this register will configure how many bytes will be read back, default is 8 bytes | |
| 3 | BC3 | | RW | 1 | | |
| 2 | BC2 | | RW | 0 | | |
| 1 | BC1 | | RW | 0 | | |
| 0 | BC0 | | RW | 0 | | |

Byte 8 and 9: Reserved

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|-------------|------|------------------------|---|---|
| 7:0 | Reserved | | | B8 = 0x36 B9 = 0x00 | | |

Byte 10: PD Restore

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|-------------------------------------|------|--------------------|-----------------|----------------|
| 7 | Reserved | | | 0 | | |
| 6 | PD Restore | PD Restore to default configuration | RW | 1 | Clear PD Config | Keep PD Config |
| 5:0 | Reserved | | | 0 | | |

Byte 11: Stop Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|--|------|--------------------|-------------|--------------|
| 7:2 | Reserved | | | 0 | | |
| 1 | STP1 | True/ Compliment DIF Output Disable Sate | RW | 0 | 00= Low/Low | 10= High/Low |
| 0 | STP0 | | RW | 0 | 01= HiZ/HiZ | 11= Low/High |

Byte 12: Impedance Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|-------------|------|--------------------|---|---|
| 7 | Q3_Zout1 | Q3 Zout | RW | 10 | 00 = Reserved 01 = 85Ω 10 = 100Ω 11 = Reserved | |
| 6 | Q3_Zout0 | Q3 Zout | RW | | | |
| 5 | Q2_Zout1 | Q2 Zout | RW | | | |
| 4 | Q2_Zout0 | Q2 Zout | RW | | | |
| 3 | Q1_Zout1 | Q1 Zout | RW | | | |
| 2 | Q1_Zout0 | Q1 Zout | RW | | | |
| 1 | Q0_Zout1 | Q0 Zout | RW | | | |
| 0 | Q0_Zout0 | Q0 Zout | RW | | | |

Byte 13: Impedance Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|-------------|------|--------------------|---|---|
| 7 | Q7_Zout1 | Q7 Zout | RW | 10 | 00 = Reserved 01 = 85Ω 10 = 100Ω 11 = Reserved | |
| 6 | Q7_Zout0 | Q7 Zout | RW | | | |
| 5 | Q6_Zout1 | Q6 Zout | RW | | | |
| 4 | Q6_Zout0 | Q6 Zout | RW | | | |
| 3 | Q5_Zout1 | Q5 Zout | RW | | | |
| 2 | Q5_Zout0 | Q5 Zout | RW | | | |
| 1 | Q4_Zout1 | Q4 Zout | RW | | | |
| 0 | Q4_Zout0 | Q4 Zout | RW | | | |

Byte 14: OE Termination Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|---------------------|------|--------------------|-------------|--------------------|
| 7 | OE3_term1 | OE3 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 6 | OE3_term0 | OE3 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |
| 5 | OE2_term1 | OE2 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 4 | OE2_term0 | OE2 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |
| 3 | OE1_term1 | OE1 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 2 | OE1_term0 | OE1 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |
| 1 | OE0_term1 | OE0 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 0 | OE0_term0 | OE0 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |

Byte 15: OE Termination Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|---------------------|------|--------------------|-------------|--------------------|
| 7 | OE7_term1 | OE7 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 6 | OE7_term0 | OE7 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |
| 5 | OE6_term1 | OE6 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 4 | OE6_term0 | OE6 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |
| 3 | OE5_term1 | OE5 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 2 | OE5_term0 | OE5 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |
| 1 | OE4_term1 | OE4 Pull up or down | RW | 0 | 00=None | 10= Pullup |
| 0 | OE4_term0 | OE4 Pull up or down | RW | 1 | 01=Pulldown | 11=Pullup and Down |

Byte 16: Power Good Termination Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|--|------|--------------------|-------------|--------------------|
| 7:2 | Reserved | | | 0x09 | | |
| 1 | PWRGD_PD1 | Clock Power Good and Power Down Pull up or Pull down | RW | 1 | 00=None | 10= Pullup |
| 0 | PWRGD_PD0 | | RW | 0 | 01=Pulldown | 11=Pullup and Down |

Byte 17: Reserved

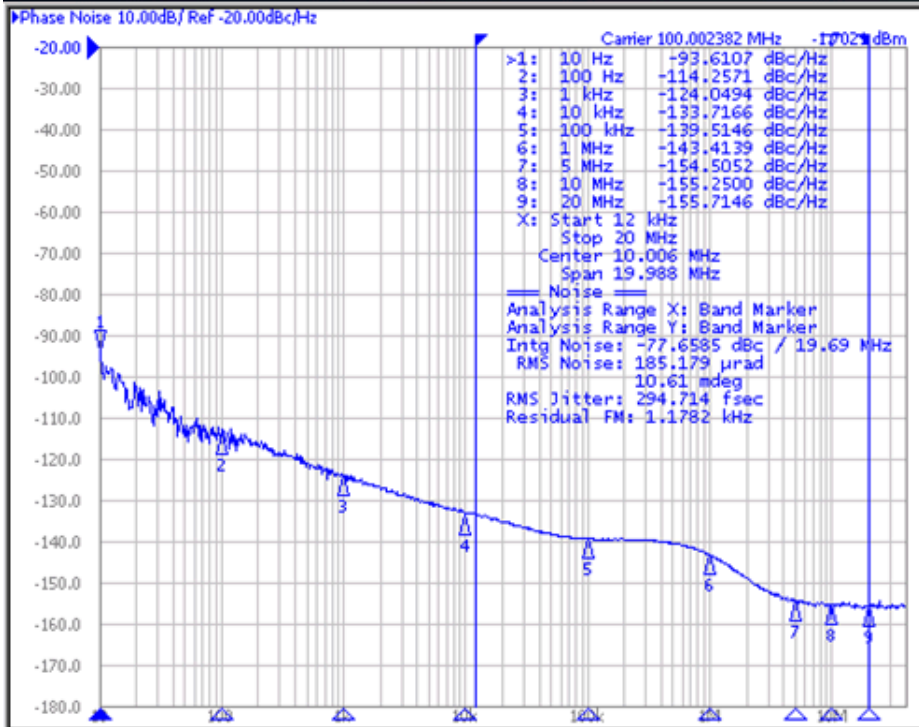
Byte 18: Enable Pin Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|-------------------------|------|--------------------|--------------|---------------|
| 7 | OE7_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 6 | OE6_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 5 | OE5_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 4 | OE4_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 3 | OE3_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 2 | OE2_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 1 | OE1_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |
| 0 | OE0_Enable | Sets Enable High or Low | RW | 0 | Enable = Low | Enable = High |

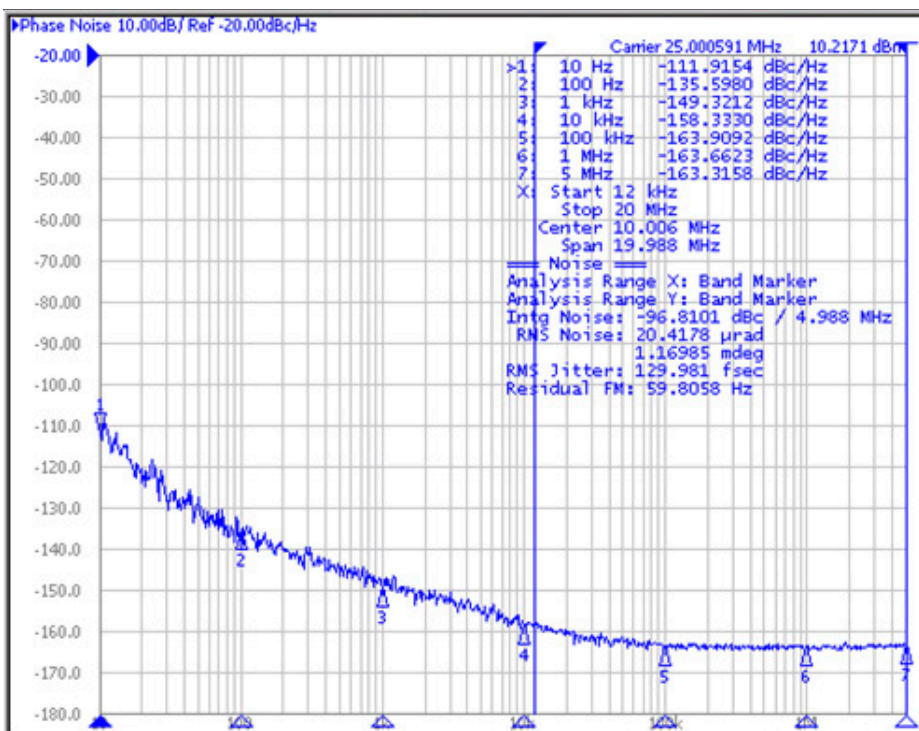
Byte 19: Power Down Pin Control

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|-----|------------------|--|------|--------------------|------------------|-------------------|
| 7:1 | Reserved | | | 0 | | |
| 0 | PWRGD_PD | PWRGD_PD Active via Pull up or Pull down | RW | 0 | Power Down = Low | Power Down = High |

Phase Noise Plots
100MHz HCSL Clock (12k to 20MHz)



25MHz CMOS Clock



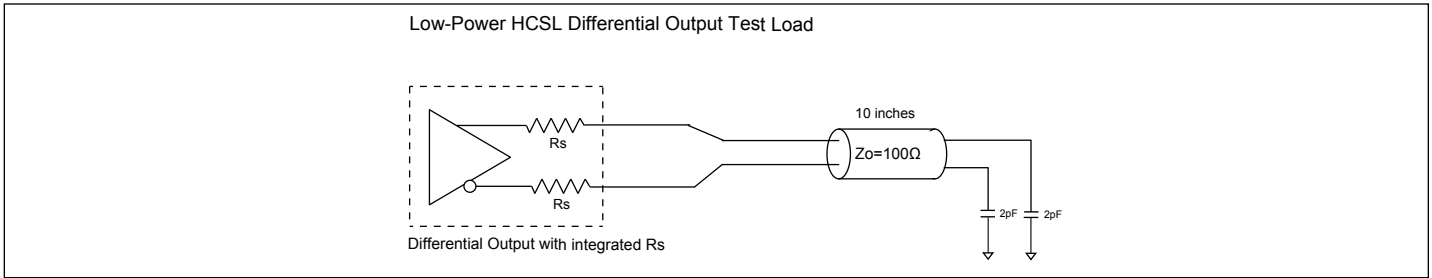


Figure 1. Low Power HCSL Test Circuit

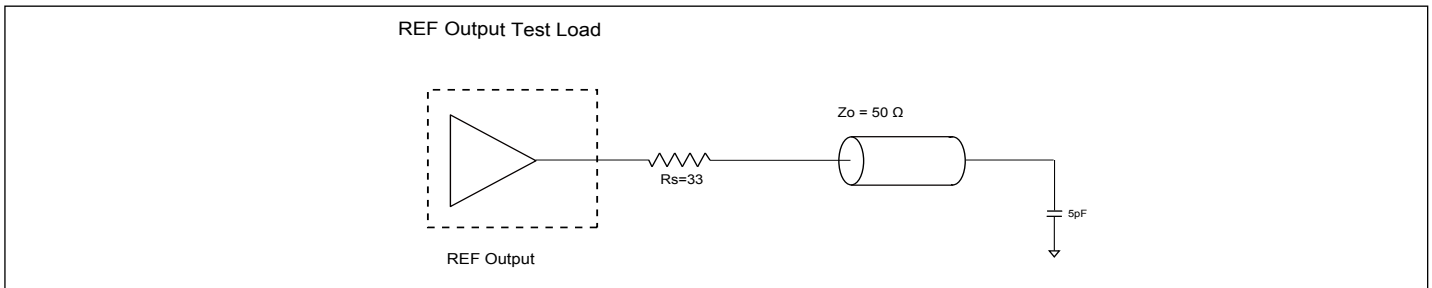


Figure 2. CMOS REF Test Circuit

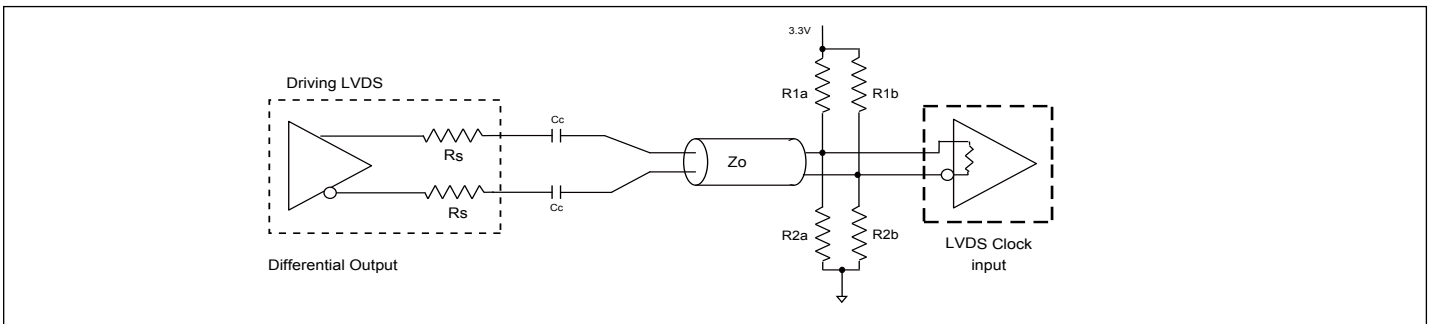


Figure 3. Differential Output driving LVDS

Alternate Differential Output Terminations

| Component | Receiver with termination | Receiver without termination | Unit |
|-----------------------------------|---------------------------|------------------------------|------|
| R _{1a} , R _{1b} | 10,000 | 140 | Ω |
| R _{2a} , R _{2b} | 5,600 | 75 | Ω |
| C _C | 0.1 | 0.1 | μF |
| V _{CM} | 1.2 | 1.2 | V |

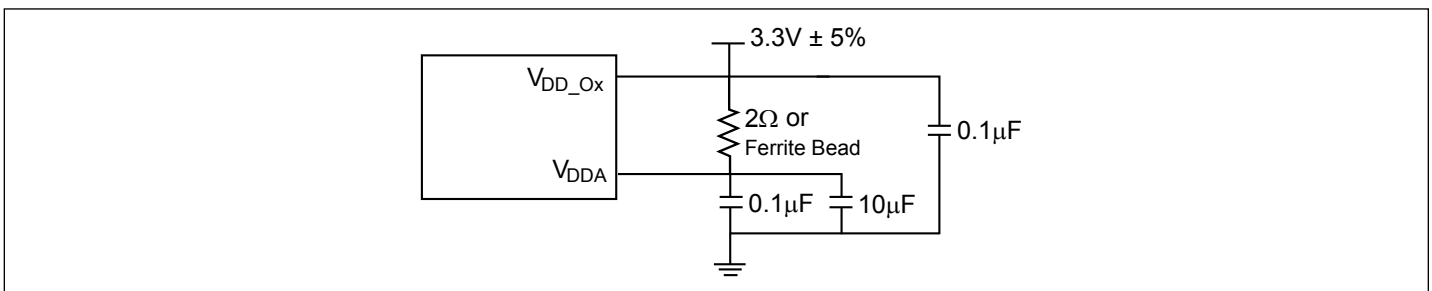
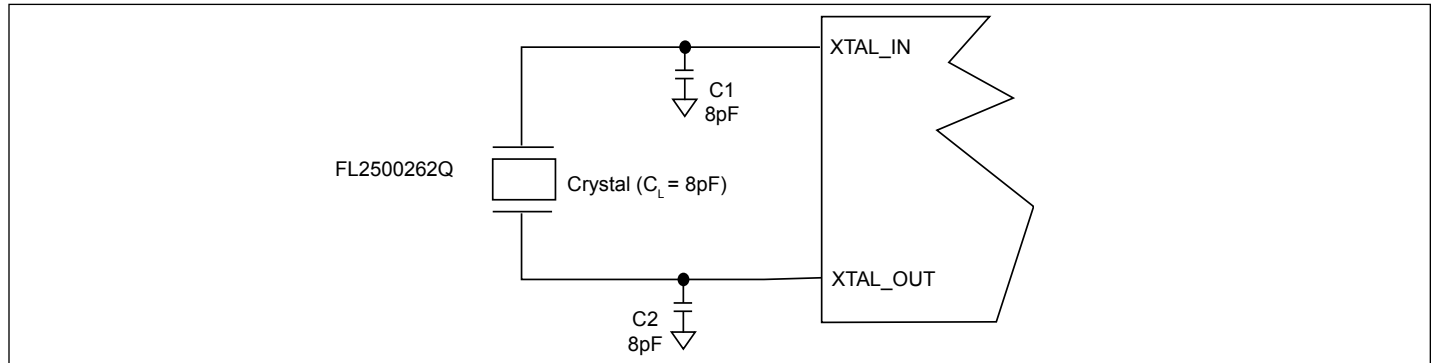


Figure 4. Power Supply Filter

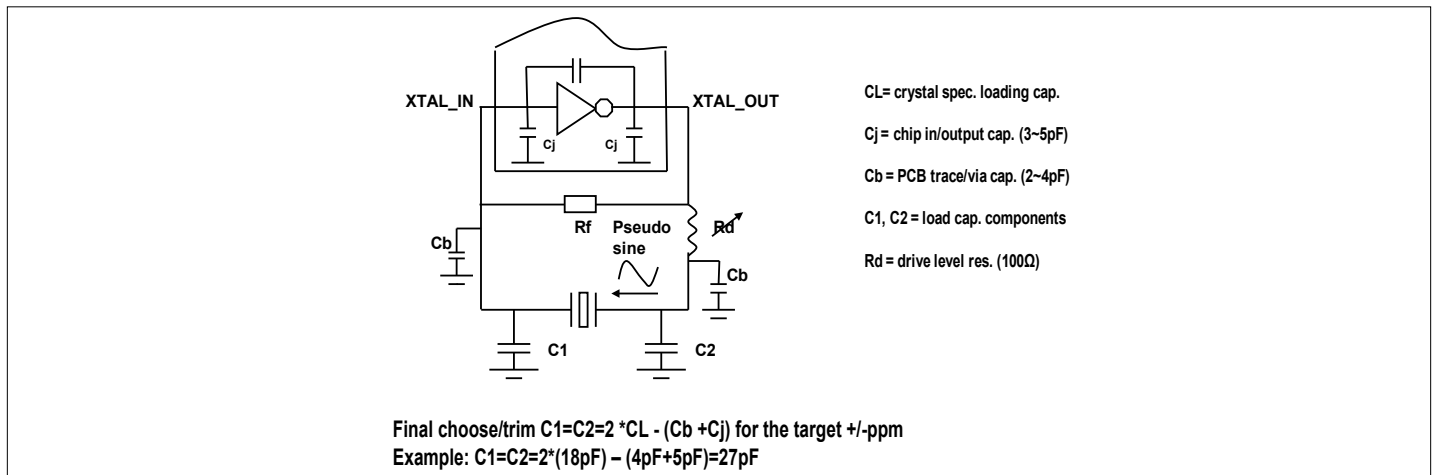
Crystal circuit connection

The following diagram shows PI6CG33801C crystal circuit connection with a parallel crystal. For the $CL=8\text{pF}$ crystal, it is suggested to use $C1=8\text{pF}$, $C2=8\text{pF}$. $C1$ and $C2$ can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts based on the following formular in the Crystal Capacitor Calculation diagram.

Crystal Oscillator Circuit



Crystal Capacitor Calculation



Recommended Crystal Specification

Diodes recommends:

- FL2500217, SMD 3.2x2.5(4P), 25MHz, $CL=8\text{pF}$, +/-20ppm, <https://www.diodes.com/assets/Datasheets/FL.pdf>
- FH2500016, SMD 2.5x2.0(4P), 25MHz, $CL=8\text{pF}$, +/-30ppm, <https://www.diodes.com/assets/Datasheets/FH.pdf>
- FW2500031, SMD 2.0x1.6(4P), 25MHz, $CL=8\text{pF}$, +/-30ppm, <https://www.diodes.com/assets/Datasheets/FW.pdf>
- US2500003, SMD 1.6x1.2(4P), 25MHz, $CL=12\text{pF}$, +/-30ppm, <https://www.diodes.com/assets/Datasheets/US.pdf>

PI6CG33801C

Thermal Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------|--|------------|------|------|-------|------|
| θ_{JA} | Thermal Resistance Junction to Ambient | Still air | | | 38.15 | °C/W |
| θ_{JC} | Thermal Resistance Junction to Case | | | | 24.66 | °C/W |

Part Marking



YY: Year

WW: Workweek

1st X: Assembly Code

2nd X: Fab Code

Packaging Mechanical: 48-TQFN (ZL)

| SYMBOLS | MIN. | NOM. | MAX. |
|---------|------------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.203 REF. | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 5.90 | 6.00 | 6.10 |
| E | 5.90 | 6.00 | 6.10 |
| e | 0.40 BSC | | |
| K | 0.35 REF. | | |
| D2 | 4.45 | 4.50 | 4.55 |
| E2 | 4.45 | 4.50 | 4.55 |
| L | 0.35 | 0.40 | 0.45 |

NOTE :
 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
 2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
 3. REFER JEDEC MO-220
 4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
 5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

| | | |
|---|--|----------------|
| | | DATE: 10/26/15 |
| DESCRIPTION: 48-Contact, Very Thin Quad Flat No-Lead (TQFN) | | |
| PACKAGE CODE: ZL (ZL48) | | |
| DOCUMENT CONTROL #: PD-2201 | | REVISION: A |

15-0244

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

| Ordering Code | Package Code | Package Description | Pin 1 Location |
|----------------------|--------------|--|------------------|
| PI6CG33801CZLIEX | ZL | 48-Contact, Very Thin Quad Flat No-Lead (TQFN) | Top Right Corner |
| PI6CG33801CZLIEX-13R | ZL | 48-Contact, Very Thin Quad Flat No-Lead (TQFN) | Top Left Corner |

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- E = Pb-free and Green
- X suffix = Tape/Reel
- For packaging details, go to our website at: <https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf>

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