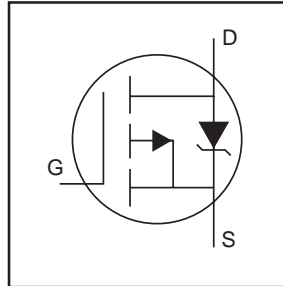


IRFR/U5410

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- P-Channel
- Surface Mount (IRFR5410)
- Straight Lead (IRFU5410)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

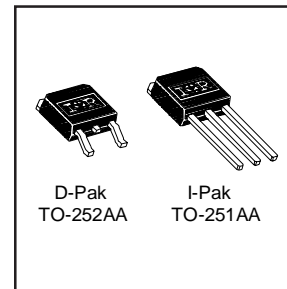


$V_{DSS} = -100V$
$R_{DS(on)} = 0.205\Omega$
$I_D = -13A$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



D-Pak
TO-252AA

I-Pak
TO-251AA

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-13	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-8.2	
I_{DM}	Pulsed Drain Current ①	-52	
$P_D @ T_C = 25^\circ C$	Power Dissipation	66	W
	Linear Derating Factor	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	194	mJ
I_{AR}	Avalanche Current③	-8.4	A
E_{AR}	Repetitive Avalanche Energy④	6.3	mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	-5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

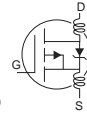
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	1.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	---	50	
$R_{\theta JA}$	Junction-to-Ambient	---	110	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	-0.12	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.205	Ω	V _{GS} = -10V, I _D = -7.8A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	3.2	—	—	S	V _{DS} = -50V, I _D = -7.8A
I _{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V _{DS} = -100V, V _{GS} = 0V
		—	—	-250		V _{DS} = -80V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	58	nC	I _D = -8.4A
Q _{gs}	Gate-to-Source Charge	—	—	8.3		V _{DS} = -80V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	32		V _{GS} = -10V, See Fig. 6 and 13 ④ ⑥
t _{d(on)}	Turn-On Delay Time	—	15	—	ns	V _{DD} = 50V
t _r	Rise Time	—	58	—		I _D = -8.4A
t _{d(off)}	Turn-Off Delay Time	—	45	—		R _G = 9.1Ω
t _f	Fall Time	—	46	—		R _D = 6.2Ω, See Fig. 10 ④ ⑥
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑤
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	760	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	260	—		V _{DS} = -25V
C _{rss}	Reverse Transfer Capacitance	—	170	—		f = 1.0MHz, See Fig. 5⑥



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-13	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-52		
V _{SD}	Diode Forward Voltage	—	—	-1.6	V	T _J = 25°C, I _S = -7.8A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	130	190	ns	T _J = 25°C, I _F = -8.4A
Q _{rr}	Reverse Recovery Charge	—	650	970	nC	di/dt = 100A/μs ④ ⑥
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 6.4mH
R_G = 25Ω, I_{AS} = -7.8A. (See Figure 12)
- ③ I_{SD} ≤ -7.8A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact
- ⑥ Uses IRF9530N data and test conditions.

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

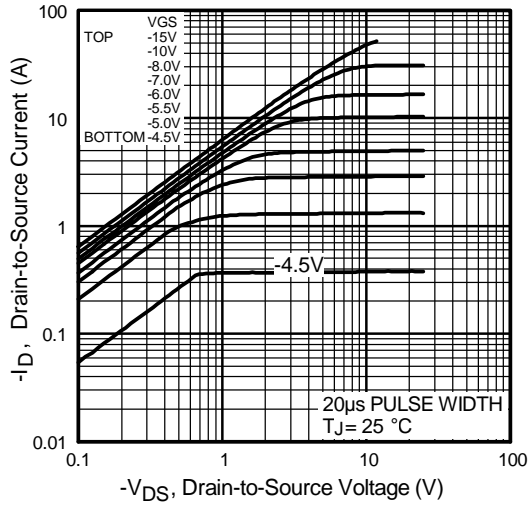


Fig 1. Typical Output Characteristics

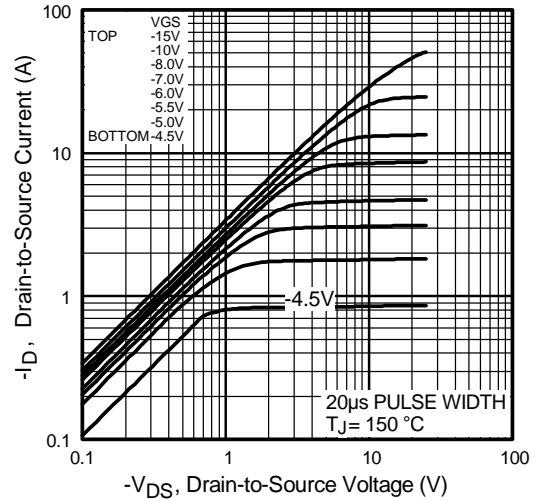


Fig 2. Typical Output Characteristics

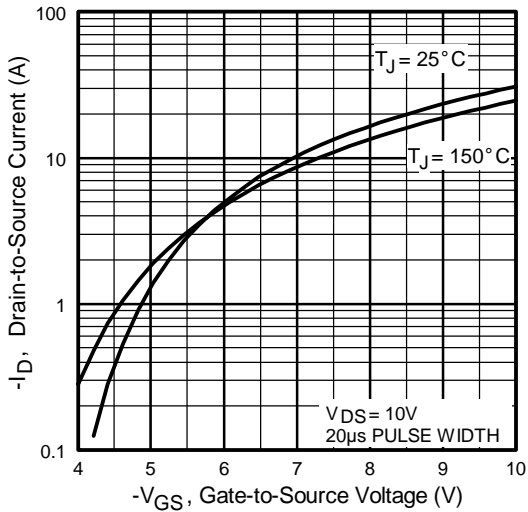


Fig 3. Typical Transfer Characteristics

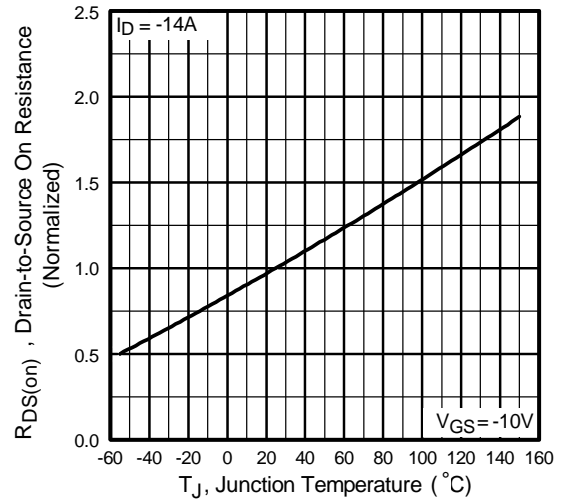


Fig 4. Normalized On-Resistance Vs. Temperature

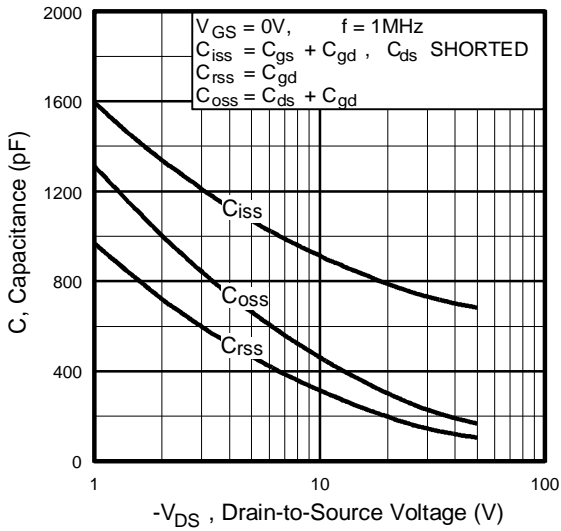


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

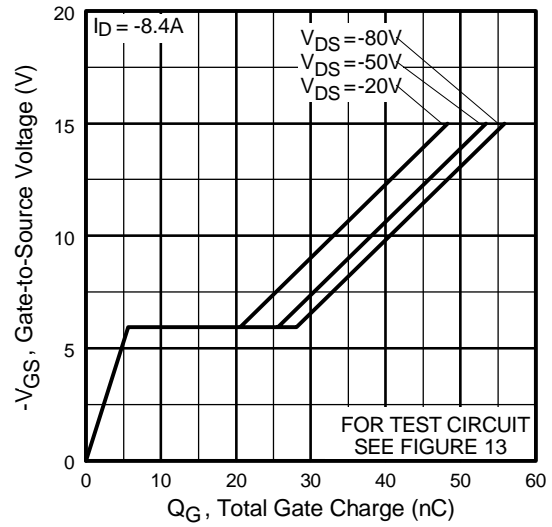


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

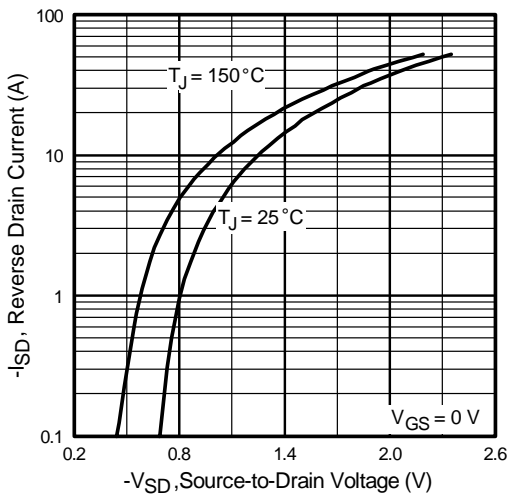


Fig 7. Typical Source-Drain Diode Forward Voltage

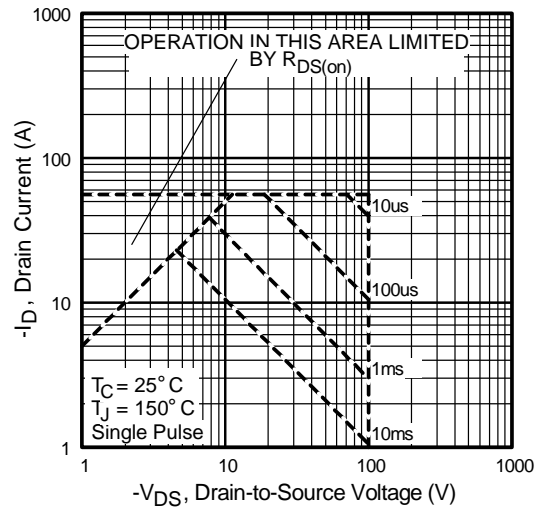


Fig 8. Maximum Safe Operating Area

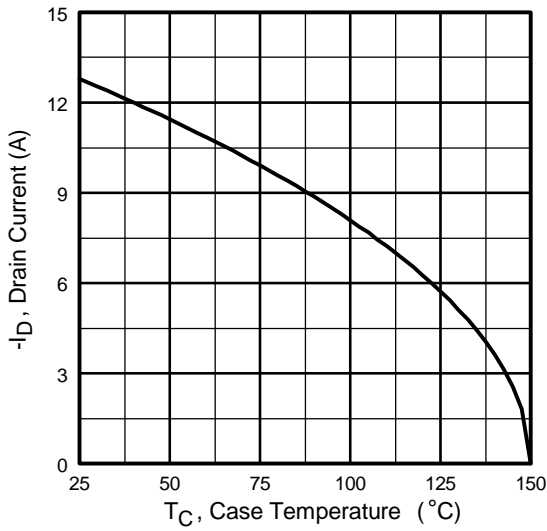


Fig 9. Maximum Drain Current Vs. Case Temperature

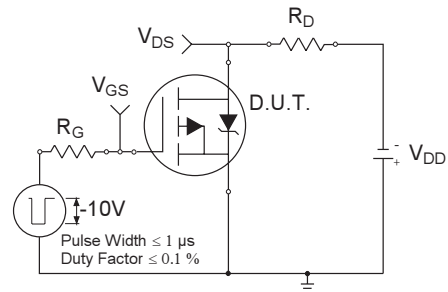


Fig 10a. Switching Time Test Circuit

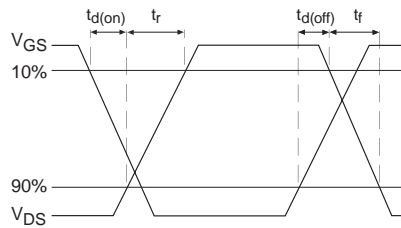


Fig 10b. Switching Time Waveforms

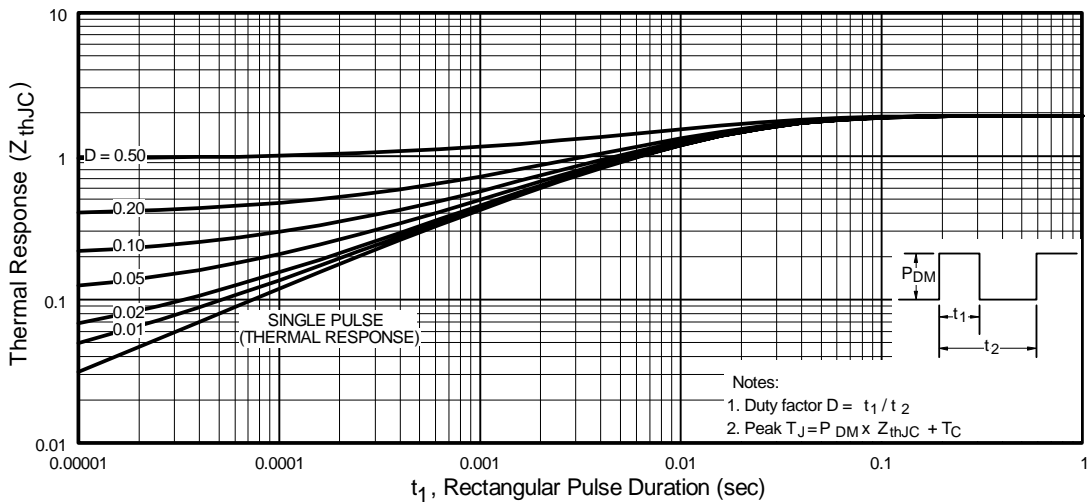


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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IR Rectifier

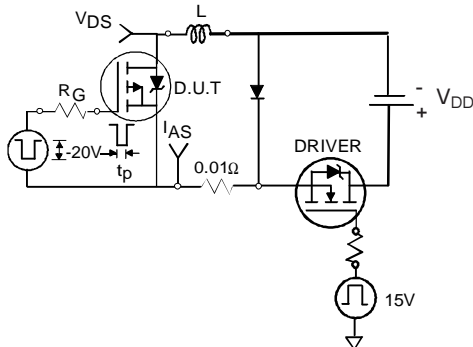


Fig 12a. Unclamped Inductive Test Circuit

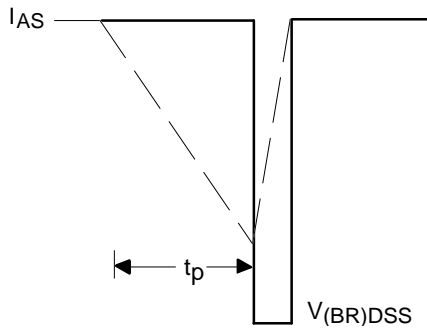


Fig 12b. Unclamped Inductive Waveforms

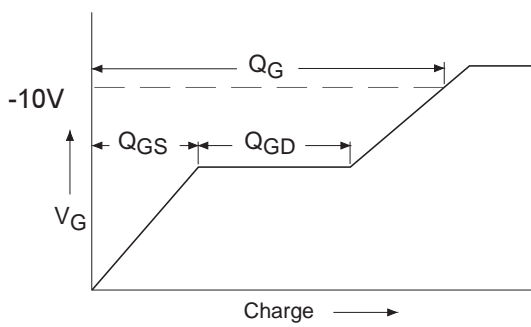


Fig 13a. Basic Gate Charge Waveform

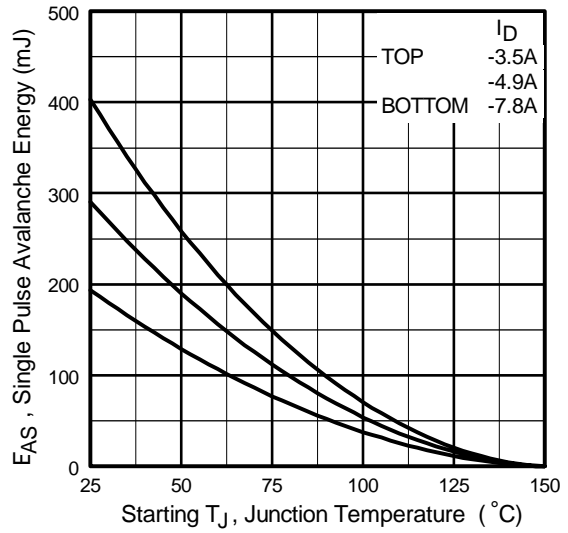


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

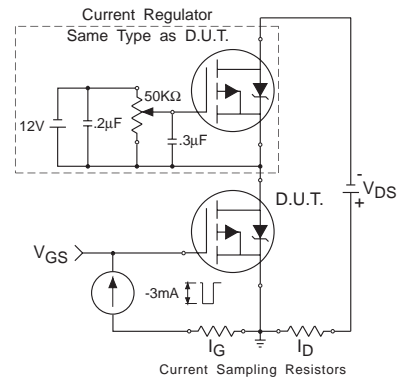
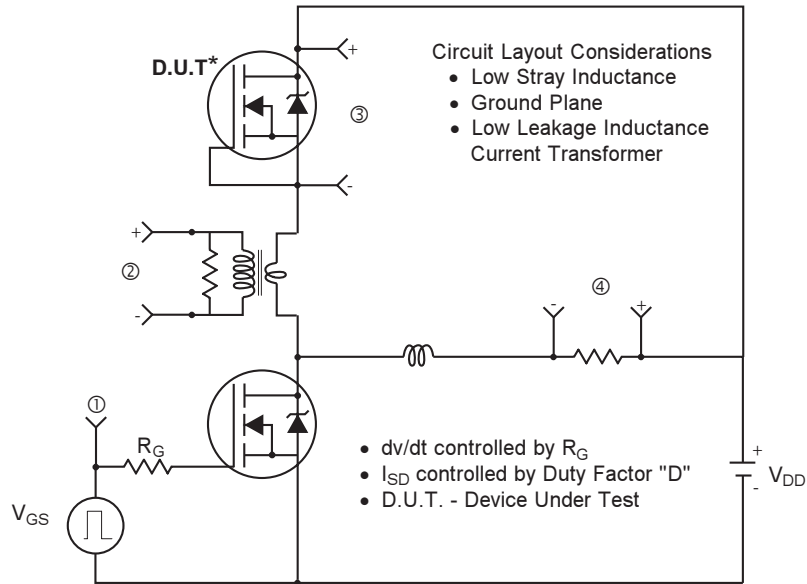
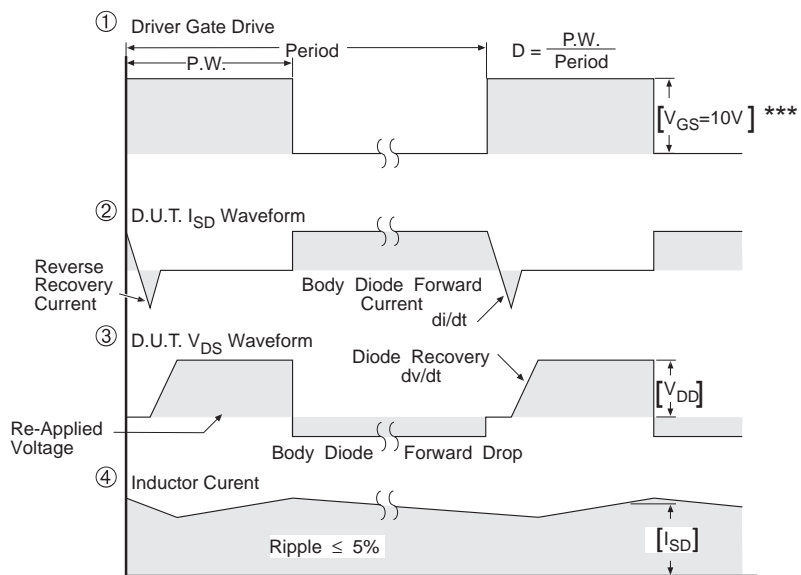


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

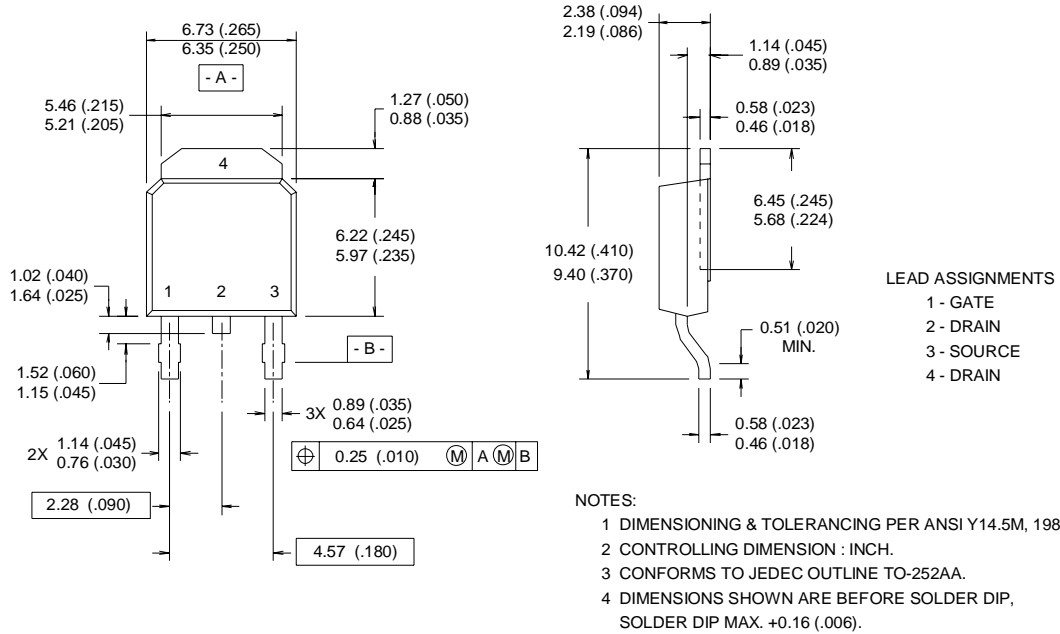
Fig 14. For P-Channel HEXFETS

IRFR/U5410

Package Outline

TO-252AA Outline

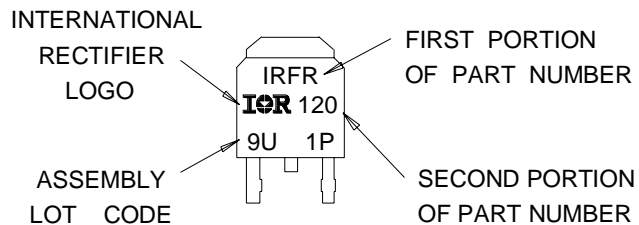
Dimensions are shown in millimeters (inches)



Part Marking Information

TO-252AA (D-Pak)

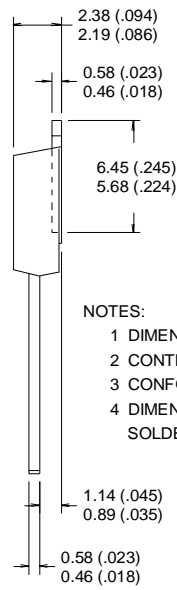
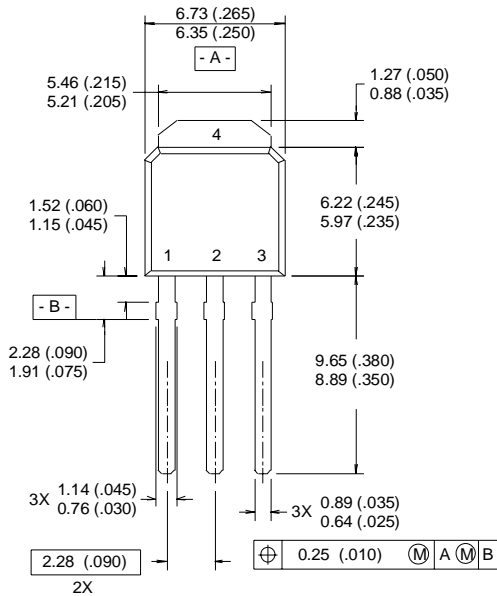
EXAMPLE : THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



Package Outline

TO-251AA Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

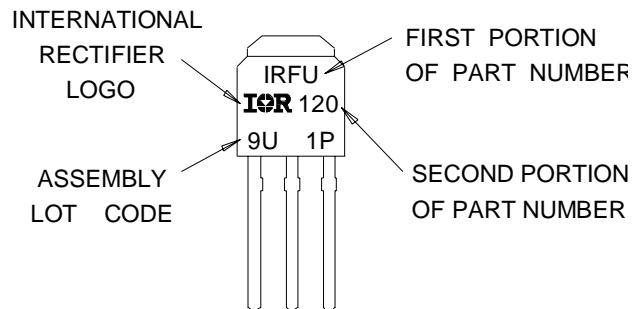
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 CONFORMS TO JEDEC OUTLINE TO-252AA.
- 4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

TO-251AA (I-Pak)

EXAMPLE : THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 9U1P



Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>