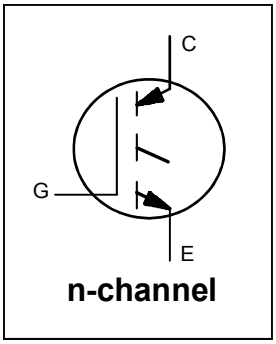
IRG8CH184K10F

INSULATED GATE BIPOLAR TRANSISTOR

V_{CES} = 1200V
$I_{C(Nominal)}$ = 200A
$T_{J(max)}$ = 175°C
$V_{CE(on)}$ typ = 1.7V @ I_C = 200A



n-channel

Applications
- Industrial Motor Drives
- UPS
- HEV Inverter
- Welding

G	C	E
Gate	Collector	Emitter

Features	→	Benefits
Low $V_{CE(on)}$ Trench IGBT Technology		High Efficiency in a Wide Range of Applications
Low Switching Losses		Suitable for a Wide Range of Switching Frequencies
Very Soft Turn-off Characteristics		Reduced EMI and Overvoltage in Motor Drive Applications
10µs Short Circuit SOA		Rugged Transient Performance for Increased Reliability
Square RBSOA		
Tight Parameter Distribution		Excellent Current Sharing in Parallel Operation
Positive $V_{CE(on)}$ Temperature Coefficient		
Integrated Gate Resistor		Easier Paralleling with Integrated Gate Resistor
$T_{j(max)}$ = 175°C		Increased Reliability

Base part number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRG8CH184K10F	Die on Film	Wafer	1	IRG8CH184K10F

Mechanical Parameter

Die Size	15.3 x 12.0	mm^2
Minimum Street Width	95	µm
Emitter Pad Size	See Die Drawing	mm^2
Gate Pad Size	1.0 x 1.6	
Area Total / Active	184 / 142.8	
Thickness	140	µm
Wafer Size	200	mm
Notch Position	0	Degrees
Maximum-Possible Chips per Wafer	134 pcs.	
Passivation Front side	Silicon Nitride, Polyimide	
Front Metal	Al, Si (5.6µm)	
Backside Metal	Al, Ti, Ni, Ag	
Die Bond	Electrically conductive epoxy or solder	
Reject Ink Dot Size	0.25 mm diameter minimum	

Maximum Ratings

	Parameter	Max.	Units
V_{CE}	Collector-Emitter Voltage, T_J = 25°C	1200	V
I_C	DC Collector Current	①	A
I_{LM}	Clamped Inductive Load Current ②	600	A
V_{GE}	Gate Emitter Voltage	± 30	V
T_J, T_{STG}	Operating Junction and Storage Temperature	-40 to +175	°C

Static Characteristics (Tested on wafers) @ T_J=25°C

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA ③
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	—	2.0		V_{GE} = 15V, I_C = 200A, T_J = 25°C ④
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	5.0	—	6.5		I_C = 8.0mA , V_{GE} = V_{CE}
I_{CES}	Zero Gate Voltage Collector Current	—	1.0	70	µA	V_{CE} = 1200V, V_{GE} = 0V
I_{GES}	Gate Emitter Leakage Current	—	—	± 600	nA	V_{CE} = 0V, V_{GE} = ±30V
$R_{G\ INTERNAL}$	Internal Gate Resistance	0.95	1.2	1.45	Ω	

Electrical Characteristics (Not subject to production test- Verified by design/characterization)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.7	—	V	V_{GE} = 15V, I_C = 200A , T_J = 25°C ⑤
		—	2.1	—		V_{GE} = 15V, I_C = 200A , T_J = 175°C⑤
SCSOA	Short Circuit Safe Operating Area	10	—	—	µs	V_{GE} = 15V, V_{CC} = 600V V_P ≤ 1200V,T_J = 150°C
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T_J = 175°C, I_C = 600A V_{CC} = 960V, Vp ≤ 1200V V_{GE} = +20V to 0V
C_{iss}	Input Capacitance	—	20230	—	pF	V_{GE} = 0V
C_{oss}	Output Capacitance	—	800	—		V_{CE} = 30V
C_{rss}	Reverse Transfer Capacitance	—	570	—		f = 1.0MHz
Q_g	Total Gate Charge (turn-on)	—	1110	—	nC	I_C = 200A ⑤
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	67	—		V_{GE} = 15V
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	710	—		V_{CC} = 600V

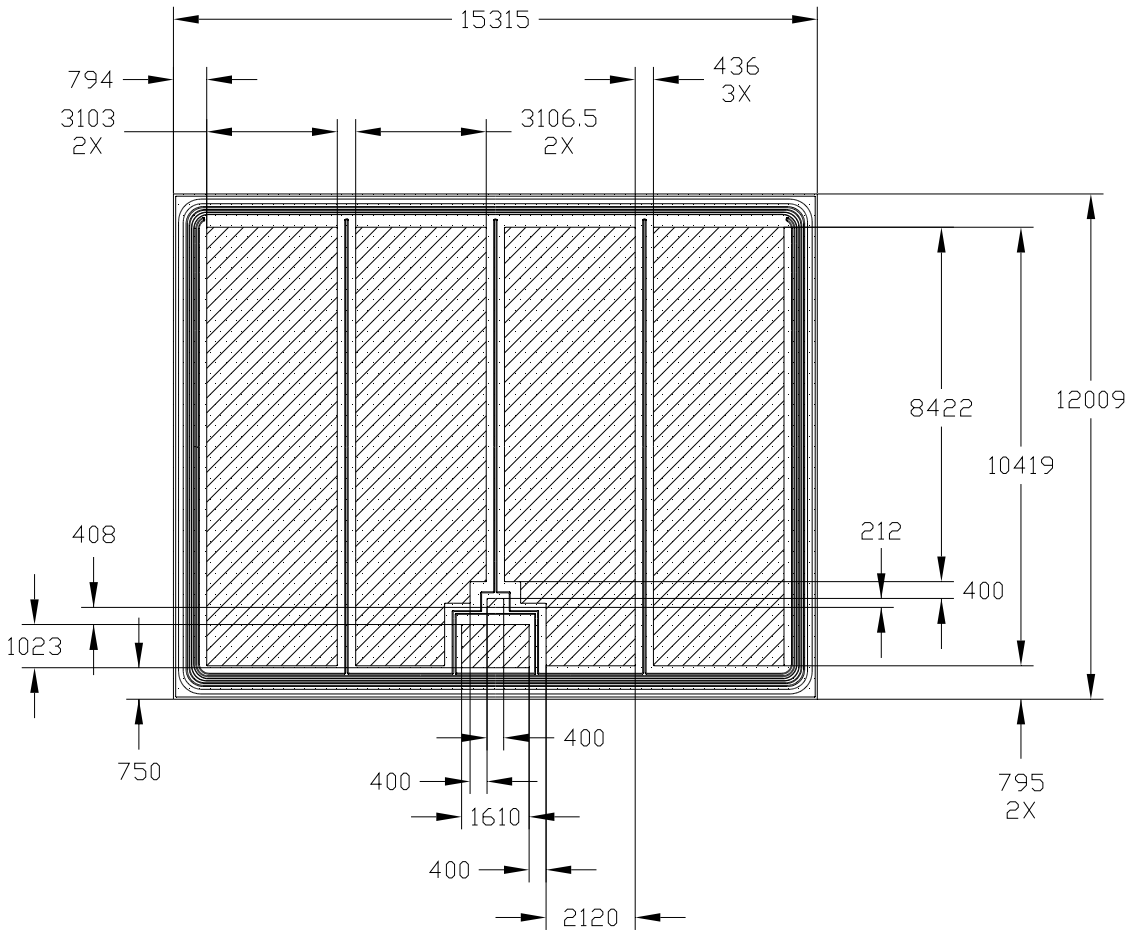
Switching Characteristics (Inductive Load-Not subject to production test-Verified by design/characterization)

	Parameter	Min.	Typ.	Max.	Units	Conditions ⑥
$t_{d(on)}$	Turn-On delay time	—	135	—	ns	I_C = 200A, V_{CC} = 600V
t_r	Rise time	—	40	—		R_G = 2.0Ω, V_{GE}=15V
$t_{d(off)}$	Turn-Off delay time	—	640	—		T_J = 25°C
t_f	Fall time	—	170	—		
$t_{d(on)}$	Turn-On delay time	—	130	—		I_C = 200A, V_{CC} = 600V
t_r	Rise time	—	45	—		R_G = 2.0Ω, V_{GE} = 15V
$t_{d(off)}$	Turn-Off delay time	—	780	—		T_J = 150°C
t_f	Fall time	—	235	—		

Notes:

① The current in the application is limited by T_{JMax} and the thermal properties of the assembly.
② V_{CC} = 80%$V_{(BR)CES}$, V_{GE} = 20V. Die is probed at I_L = 25A, V_{GE} = 15V at elevated temperature.
③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.
④ Actual test limits take into account additional losses in the measurement setup.
⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.
⑥ Values influenced by parasitic L and C in measurement.

Die Drawing



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MICRO-METER
2. CONTROLLING DIMENSION: MICRO-METER
3. DIE WIDTH AND LENGTH TOLERANCE: -50µm
4. DIE THICKNESS = 140 MICRO-METER

Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales

Shipping

Sawn Wafer on Film. Please contact your local IR sales office for non-standard shipping options

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

Further Information

For further information please contact your local IR Sales office.

Revision History

Date	Comments
06/04/2015	• Updated IFX logo on page 1 & 4.

International
IOR Rectifier
AN INFINEON TECHNOLOGIES COMPANY

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
To contact International Rectifier, please visit http://www.irf.com/whoto-call/

