

IGBT

TRENCHSTOP™ IGBT3 Chip IGC114T170S8RM

Data Sheet

Industrial Power Control



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TRENCHSTOP[™] IGBT3 Chip

Features:

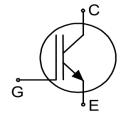
- 1700V trench & field stop technology
- Low switching losses
- Soft turn off
- Positive temperature coefficient
- Easy paralleling

Recommended for:

Power modules

Applications:

• Drives



Chip Type	V _{CE}	<i>I</i> _{Cn} ¹	Die Size	Package
IGC114T170S8RM	1700V	100A	9.47mm x 12.08mm	Sawn on foil

Mechanical Parameters

Die size		9.47 x 12.08		
Emitter pad size		See chip drawing	mm ²	
Gate pad size		1.674 x 0.899		
Area total		114.4		
Thickness		190	μm	
Wafer size		200	mm	
Maximum possible ch	ips per wafer	225		
Passivation frontside	Passivation frontside Photoimide			
Pad metal 3200nm AlSiCu				
Backside metal		Ni Ag – system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process		
Die bond	Die bond Electrically conductive epoxy glue and soft solder			
Wire bond	Al, ≤500μm			
Reject ink dot size		Ø 0.65mm; max. 1.2mm		
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C, <6 months		
	for open MBB bags	Acc. to IEC62258-3: atmosphere >99% Nitrogen or inchange humidity <25%RH, temperature 17°C – 25°C, <6 mg		

¹ Nominal collector current at T_C =100°C for chip packaged in power modules, see application example cited on page 5.



Maximum Ratings

Parameter	Symbol	Value	Unit	
Collector-emitter voltage, T _{vj} =25°C	V _{CE}	1700	V	
DC collector current, limited by $T_{\rm vjmax}^{\ \ 2}$	I _C	-	Α	
Pulsed collector current, t_p limited by $T_{vj \max}^{3}$	I _{C,puls}	300	Α	
Gate-emitter voltage	V_{GE}	±20	V	
Junction temperature range	$T_{\rm vj}$	-40 +175	°C	
Operating junction temperature	$T_{\rm vj}$	-40 +150	°C	
Short circuit data $^{3/4}$ V_{GE} =15V, V_{CC} =1000V, T_{vj} =150°C	t _{sc}	10	μs	
Reverse bias safe operating area ³ (RBSOA)	<i>I</i> _{C,max} =200A, <i>V</i> _{CE,max} =1700V, <i>T</i> _{vj} ≤150°C			

Static Characteristics (tested on wafer), T_{vi}=25°C

Parameter	Symbol	Conditions	Value			Unit
rai ametei	Symbol	Conditions	min.	typ.	max.	•
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE} =0V, I_{C} =2mA	1700	1	-	
Collector-emitter saturation voltage	V _{CEsat}	V _{GE} =15V, I _C =100A	1.6	1.9	2.2	V
Gate-emitter threshold voltage	$V_{\rm GE(th)}$	$I_{\rm C}$ =4mA, $V_{\rm GE}$ = $V_{\rm CE}$	5.2	5.8	6.4	
Zero gate voltage collector current	I _{CES}	$V_{\text{CE}} = 1700 \text{V}, \ V_{\text{GE}} = 0 \text{V}$	-	1	5.6	μA
Gate-emitter leakage current	I _{GES}	$V_{CE} = 0V, V_{GE} = 20V$		1	300	nA
Integrated gate resistor	r _G			7.5		Ω

Electrical Characteristics ³

Parameter	Symbol	Conditions	Value			Unit
raiailletei			min.	typ.	max.	Onit
Collector-emitter saturation voltage	V_{CEsat}	V_{GE} =15V, I_{C} =100A, T_{vj} =150°C	-	2.45	-	V
Input capacitance	C _{ies}	V _{CE} =25V,	-	9000	-	nE
Reverse transfer capacitance	C _{res}	V_{GE} =0V, f =1MHz T_{vj} =25°C	-	290	-	pF

² Depending on thermal properties of assembly.

³ Not subject to production test - verified by design/characterization.

⁴ Allowed number of short circuits: <1000; time between short circuits: >1s.

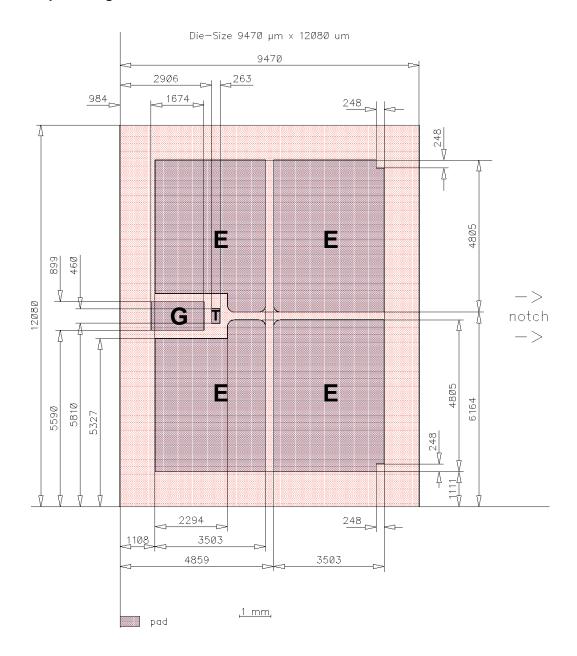


Further Electrical Characteristics

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.



Chip Drawing



E = Emitter

G = Gate

T = Test pad do not contact



Bare Die Product Specifics

Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

Description

AQL 0.65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Revision History

Revision	Subjects (major changes since last revision)	Date
2.0	Final data sheet	06.02.2015
2.1	Update disclaimer	19.08.2015

Relevant Application Notes					



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