PD-91438D

IRHM9064
JANSR2N7424

RADIATION HARDENED POWER MOSFET THRU-HOLE (TO-254AA)

60V, P-CHANNEL
REF: MIL-PRF-19500/660
RAD-Hard HEXFET TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHM9064	100 kRads(Si)	0.05Ω	-35A*	JANSR2N7424
IRHM93064	300 kRads(Si)	0.05Ω	-35A*	JANSF2N7424

TO-254AA

Description

IR HiRel RAD-Hard HEXFET technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low Rdson and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low $R_{DS(on)}$
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Light Weight
- ESD Rating: Class 3A per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = -12V, T_C = 25°C	Continuous Drain Current	-35*	A
I_D @ V_{GS} = -12V, T_C = 100°C	Continuous Drain Current	-30	
I_{DM}	Pulsed Drain Current ①	-140	
P_D @T_C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	500	mJ
I_{AR}	Avalanche Current ①	-35	A
E_{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	9.3 (Typical)	g

*Current is limited by package

For Footnotes refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.056	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.050	Ω	V_{GS} = -12V, I_D = -30A ④
		—	—	0.053		V_{GS} = -12V, I_D = -35A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -1.0mA
Gfs	Forward Transconductance	18	—	—	S	V_{DS} = -15V, I_D = -30A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V_{DS} = -48V, V_{GS} = 0V
		—	—	-250		V_{DS} = -48V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_G	Total Gate Charge	—	—	300	nC	I_D = -35A
Q_{GS}	Gate-to-Source Charge	—	—	70		V_{DS} = -30V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	91		V_{GS} = -12V
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = -30V
tr	Rise Time	—	—	150		I_D = -35A
$t_{d(off)}$	Turn-Off Delay Time	—	—	200		R_G = 2.35Ω
t_f	Fall Time	—	—	200		V_{GS} = -12V
$L_S + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	6700	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	2800	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	920	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-35*	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-140		
V_{SD}	Diode Forward Voltage	—	—	-3.0	V	T_J = 25°C, I_S = -35A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	—	270	ns	T_J = 25°C, I_F = -35A, V_{DD} ≤ -50V
Q_{rr}	Reverse Recovery Charge	—	—	2.5	μC	di/dt = -100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

* Current is limited by package

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.50	°C/W
$R_{\theta CS}$	Case -to-Sink	—	0.21	—	
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	48	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = -25V, starting T_J = 25°C, L =0.82mH, Peak I_L = -35A, V_{GS} = -12V

③ I_{SD} ≤ -35A, di/dt ≤ -150A/μs, V_{DD} ≤ -60V, T_J ≤ 150°C

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** -12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** -48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100 kRads (Si)[1]		300 kRads (Si)[2]		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	——	-60	——	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	-2.0	-5.0	V	V_{DS} = V_{GS}, I_D = -1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	-100	——	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	100	——	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	——	-25	——	-25	µA	V_{DS} = -48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	0.05	——	0.05	Ω	V_{GS} = -12V, I_D = -30A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-254AA)	——	0.05	——	0.05	Ω	V_{GS} = -12V, I_D = -30A
V_{SD}	Diode Forward Voltage ④	——	-3.0	——	-3.0	V	V_{GS} = 0V, I_D = -35A

1. Part numbers IRHM9064 (JANSR2N7424)
2. Part number IRHM93064 (JANSF2N7424)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	V_{DS} (V)				
				@V_{GS}=0V	@V_{GS}=5V	@V_{GS}=10V	@V_{GS}=15V	@V_{GS}=20V
Cu	28	285	43	-60	-60	-50	-35	——
Br	36.8	305	39	-55	-45	-35	-30	——
I	59.9	345	32.8	-40	-35	——	——	——

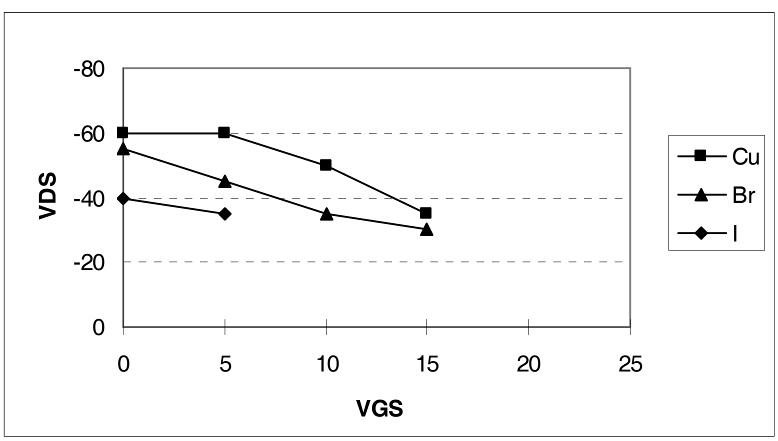


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

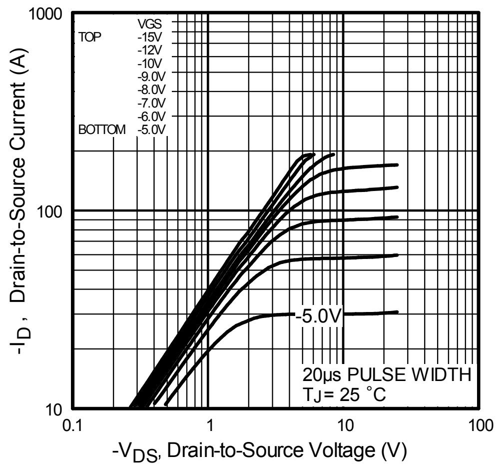


Fig 1. Typical Output Characteristics

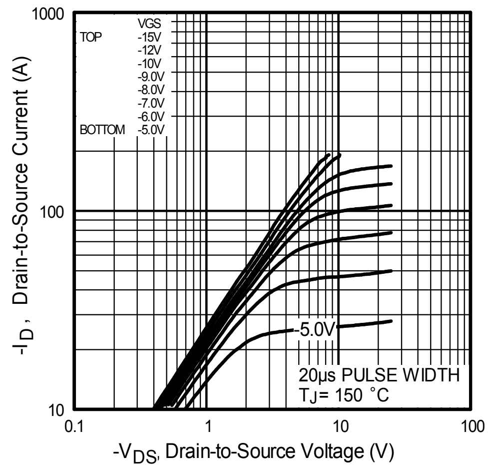


Fig 2. Typical Output Characteristics

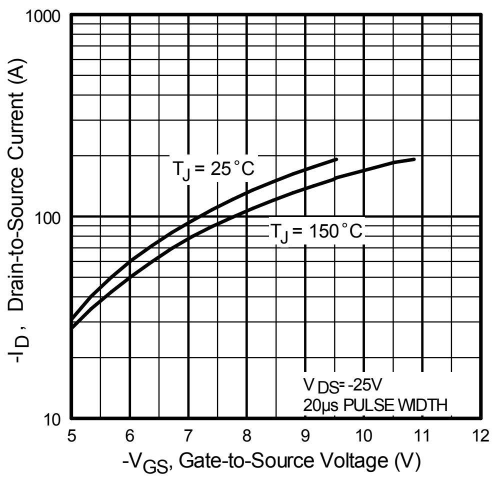


Fig 3. Typical Transfer Characteristics

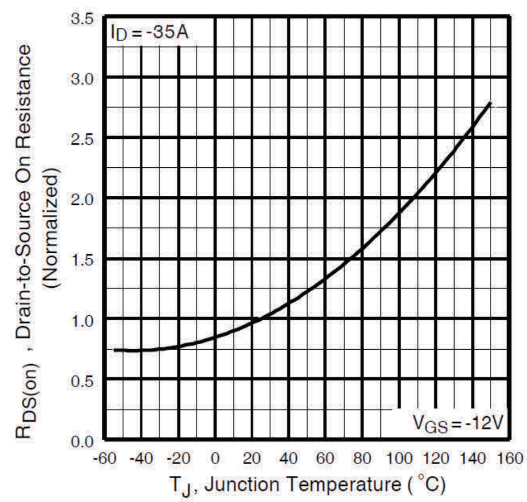


Fig 4. Normalized On-Resistance Vs. Temperature

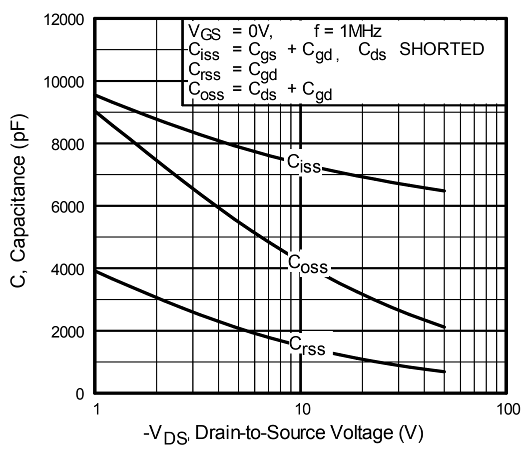


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

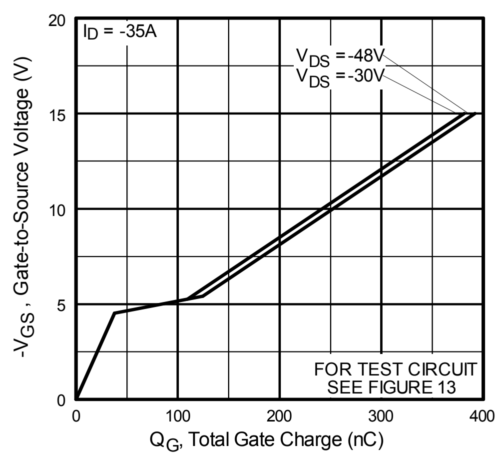


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

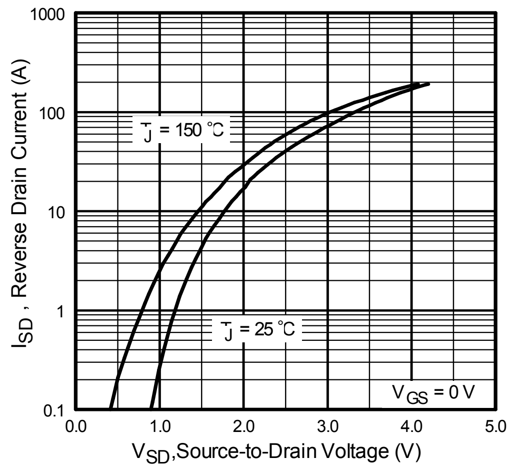


Fig 7. Typical Source-Drain Diode Forward Voltage

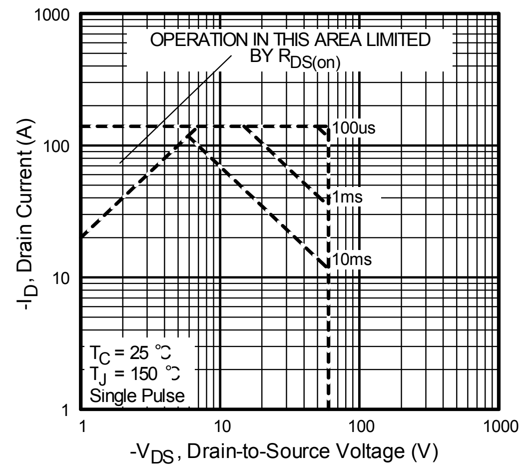


Fig 8. Maximum Safe Operating Area

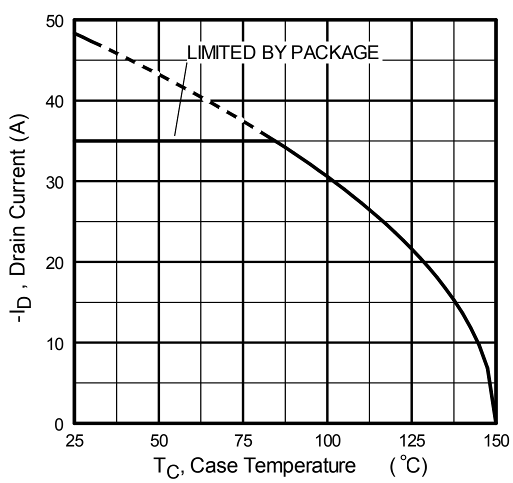


Fig 9. Maximum Drain Current Vs. Case Temperature

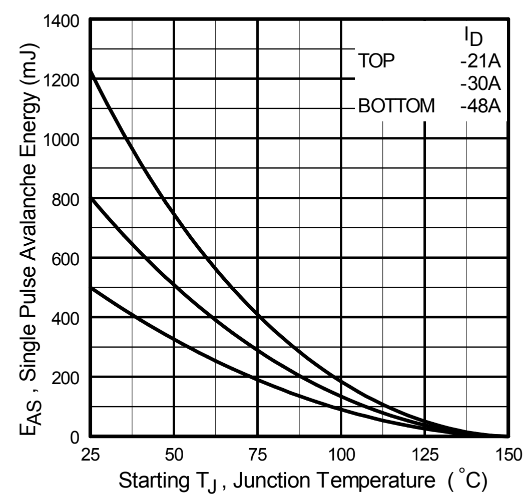


Fig 10. Maximum Avalanche Energy Vs. Drain Current

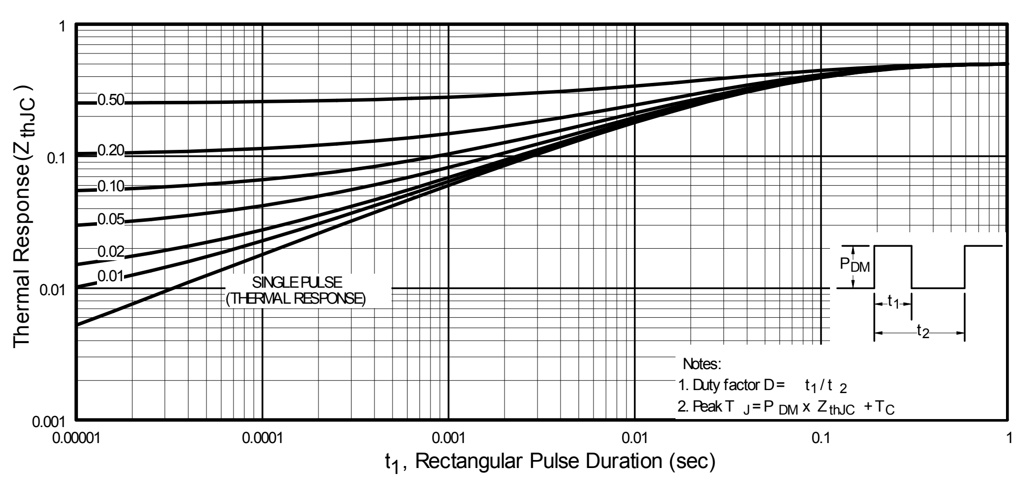


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

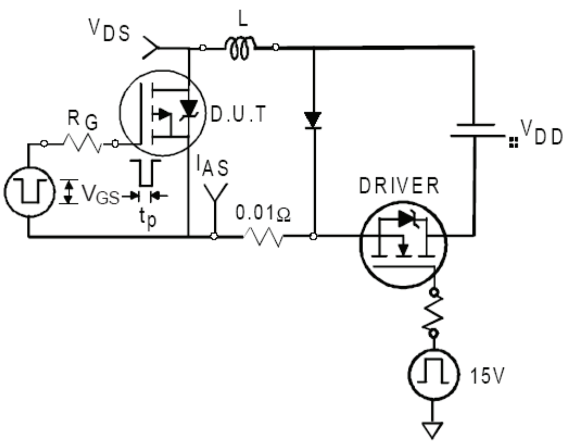


Fig 12a. Unclamped Inductive Test Circuit

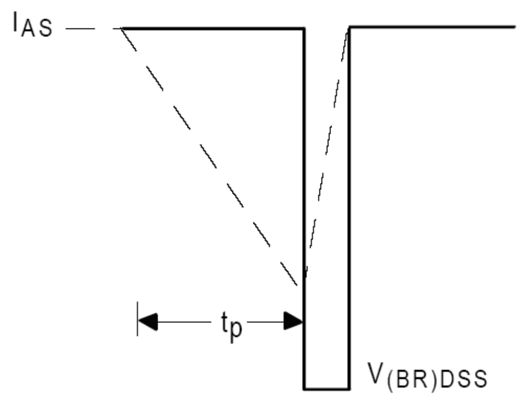


Fig 12b. Unclamped Inductive Waveforms

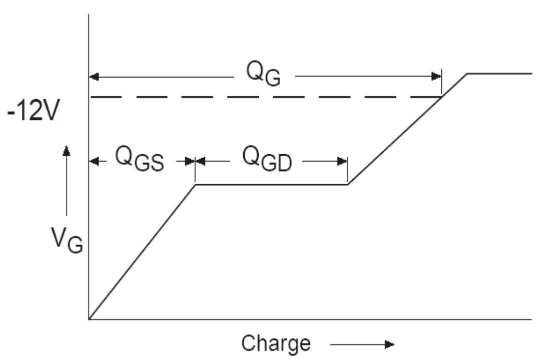


Fig 13a. Gate Charge Waveform

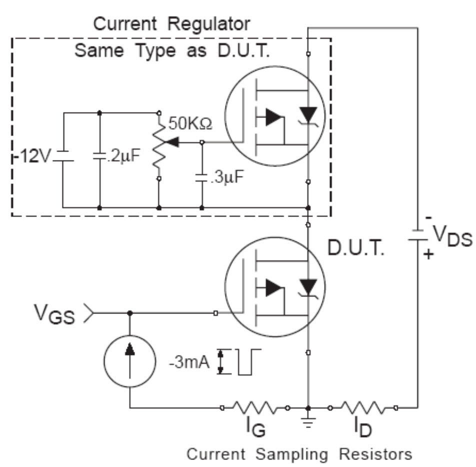


Fig 13b. Gate Charge Test Circuit

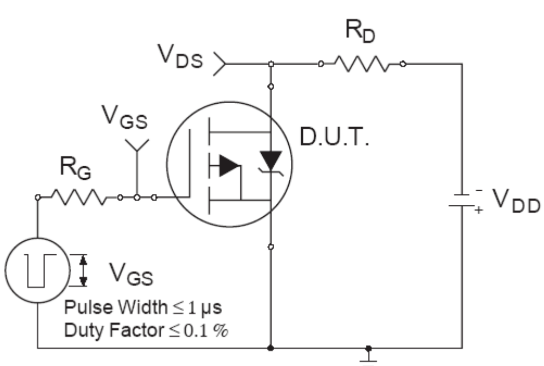


Fig 14a. Switching Time Test Circuit

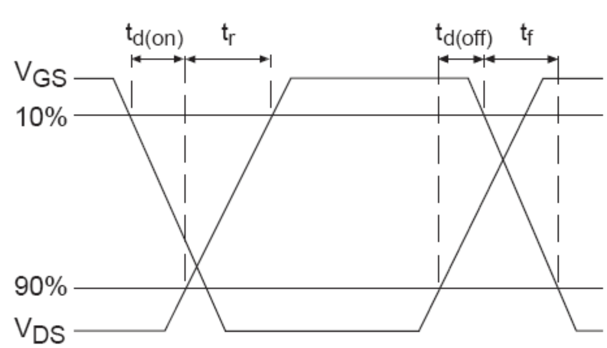
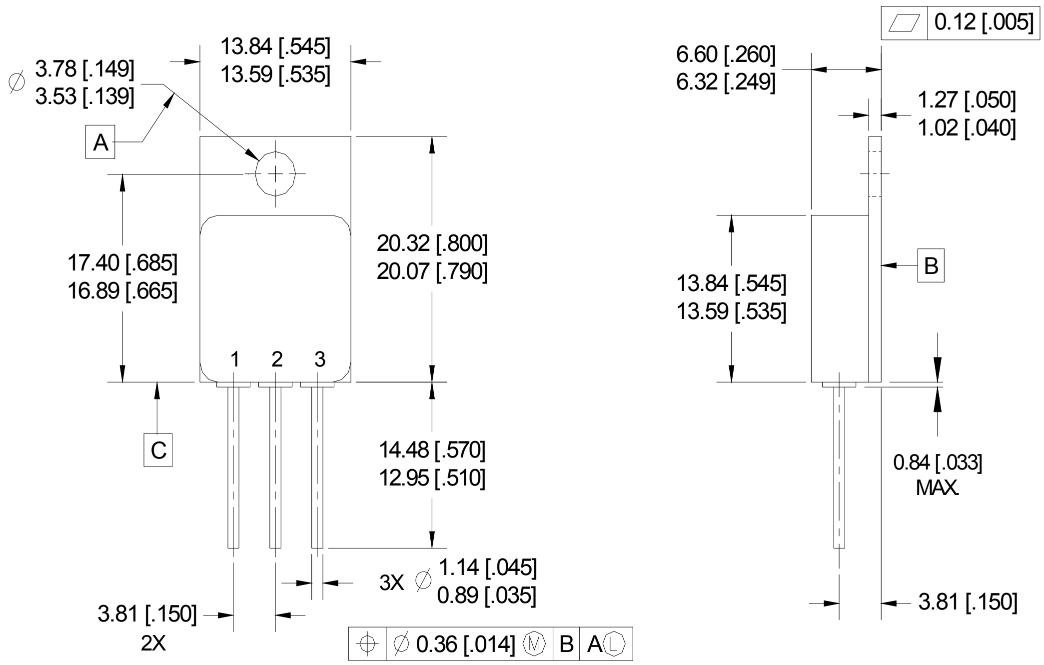


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions — TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

1 = DRAIN
2 = SOURCE
3 = GATE

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

An Infineon Technologies Company

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