International
IOR Rectifier

PD - 97636A

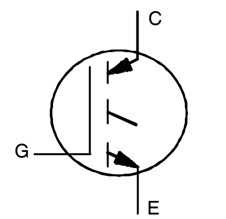
IRG7IA13UPbF

PDP TRENCH IGBT

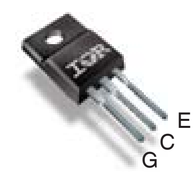
Features

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low $V_{CE(on)}$ and Energy per Pulse (E_{PULSE}™) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters		
V_{CE} min	360	V
$V_{CE(ON)}$ typ. @ I_C = 20A	1.42	V
I_{RP} max @ T_C= 25°C	160	A
T_J max	150	°C



n-channel



TO-220 Full-Pak
IRG7IA13UPbF

G	C	E
Gate	Collector	Emitter

Description

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low $V_{CE(on)}$ and low E_{PULSE}™ rating per silicon area which improve panel efficiency. Additional features are 150°C operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GE}	Gate-to-Emitter Voltage	±30	V
I_C @ T_C = 25°C	Continuous Collector Current, V_{GE} @ 15V	20	A
I_C @ T_C = 100°C	Continuous Collector, V_{GE} @ 15V	10	
I_{RP} @ T_C = 25°C	Repetitive Peak Current ①	160	
P_D @T_C = 25°C	Power Dissipation	34	W
P_D @T_C = 100°C	Power Dissipation	14	
	Linear Derating Factor	0.27	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	°C
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	3.7	°C/W
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	65	
Wt	Weight	2.0	—	g

08/02/12

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{CES}	Collector-to-Emitter Breakdown Voltage	360	–––	–––	V	V_{GE} = 0V, I_{CE} = 250µA
$\Delta BV_{CES}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.4	–––	V/°C	Reference to 25°C, I_{CE} = 1mA
$V_{CE(on)}$	Static Collector-to-Emitter Voltage	–––	1.26	1.52	V	V_{GE} = 15V, I_{CE} = 12A ③
		–––	1.42	–––		V_{GE} = 15V, I_{CE} = 20A ③
			1.84	–––		V_{GE} = 15V, I_{CE} = 40A ③
		–––	2.25	–––		V_{GE} = 15V, I_{CE} = 60A ③
		–––	1.48	–––		V_{GE} = 15V, I_{CE} = 20A, T_J = 150°C ③
$V_{GE(th)}$	Gate Threshold Voltage	2.2	–––	4.7	V	V_{CE} = V_{GE}, I_{CE} = 1.0mA
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	–––	-10	–––	mV/°C	
I_{CES}	Collector-to-Emitter Leakage Current	–––	1.0	10	µA	V_{CE} = 360V, V_{GE} = 0V
			25	150		V_{CE} = 360V, V_{GE} = 0V, T_J = 125°C
		–––	75	–––		V_{CE} = 360V, V_{GE} = 0V, T_J = 150°C
I_{GES}	Gate-to-Emitter Forward Leakage	–––	–––	100	nA	V_{GE} = 30V
	Gate-to-Emitter Reverse Leakage	–––	–––	-100		V_{GE} = -30V
g_{fe}	Forward Transconductance	–––	47	–––	S	V_{CE} = 25V, I_{CE} = 12A
Q_g	Total Gate Charge	–––	33	–––	nC	V_{CE} = 240V, I_C = 12A, V_{GE} = 15V③
Q_{gc}	Gate-to-Collector Charge	–––	12	–––		
$t_{d(on)}$	Turn-On delay time	–––	11	–––	ns	I_C = 12A, V_{CC} = 196V
t_r	Rise time	–––	13	–––		R_G = 10Ω, L=210µH
$t_{d(off)}$	Turn-Off delay time	–––	75	–––		T_J = 25°C
t_f	Fall time	–––	120	–––		
$t_{d(on)}$	Turn-On delay time	–––	11	–––	ns	I_C = 12A, V_{CC} = 196V
t_r	Rise time	–––	14	–––		R_G = 10Ω, L=200µH, L_S= 150nH
$t_{d(off)}$	Turn-Off delay time	–––	86	–––		T_J = 150°C
t_f	Fall time	–––	190	–––		
t_{st}	Shoot Through Blocking Time	100	–––	–––	ns	V_{CC} = 240V, V_{GE} = 15V, R_G= 5.1Ω
E_{PULSE}	Energy per Pulse	–––	480	–––	µJ	L = 220nH, C= 0.20µF, V_{GE} = 15V V_{CC} = 240V, R_G= 5.1Ω, T_J = 25°C
		–––	570	–––		L = 220nH, C= 0.20µF, V_{GE} = 15V V_{CC} = 240V, R_G= 5.1Ω, T_J = 100°C
ESD	Human Body Model	Class 1C (Per JEDEC standard JESD22-A114)				
	Machine Model	Class B (Per EIA/JEDEC standard EIA/JESD22-A115)				
C_{ies}	Input Capacitance	–––	880	–––	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	–––	47	–––		V_{CE} = 30V
C_{res}	Reverse Transfer Capacitance	–––	26	–––		f = 1.0MHz
L_C	Internal Collector Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.)
L_E	Internal Emitter Inductance	–––	7.5	–––		from package and center of die contact

Notes:

① Half sine wave with duty cycle = 0.05, ton=2µsec.

② R_θ is measured at T_J of approximately 90°C.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

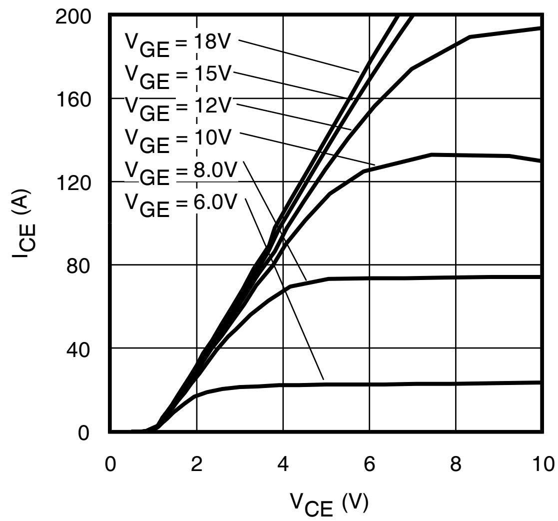


Fig 1. Typical Output Characteristics @ 25°C

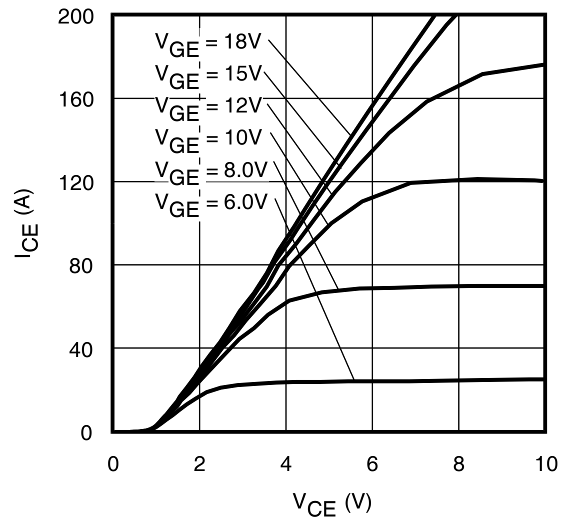


Fig 2. Typical Output Characteristics @ 75°C

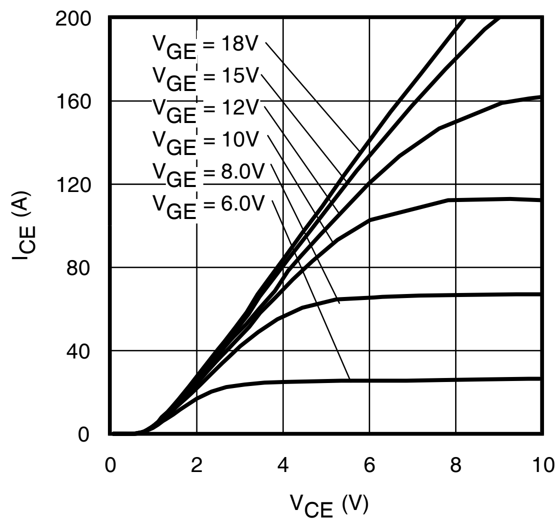


Fig 3. Typical Output Characteristics @ 125°C

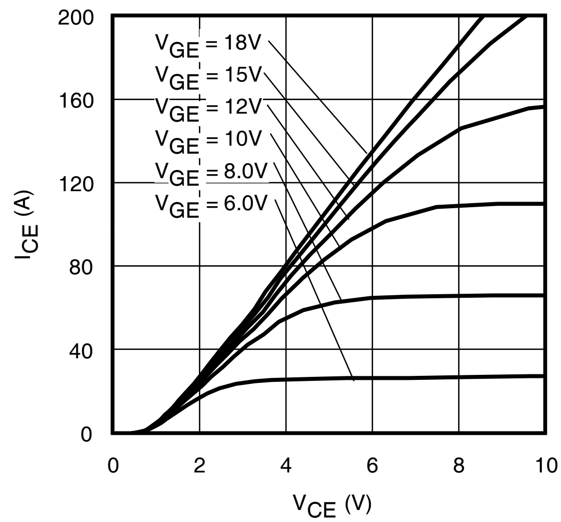


Fig 4. Typical Output Characteristics @ 150°C

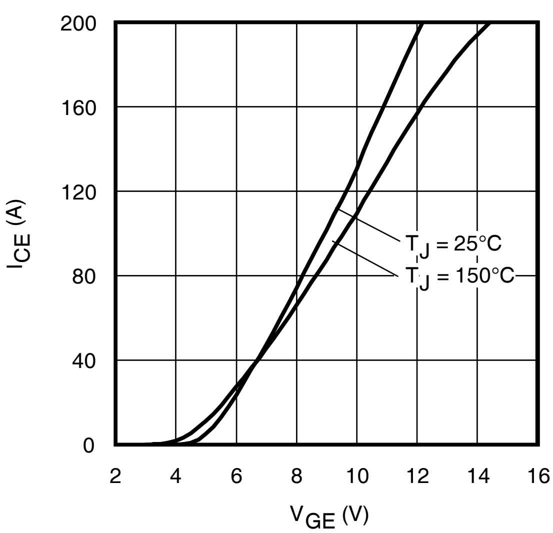


Fig 5. Typical Transfer Characteristics

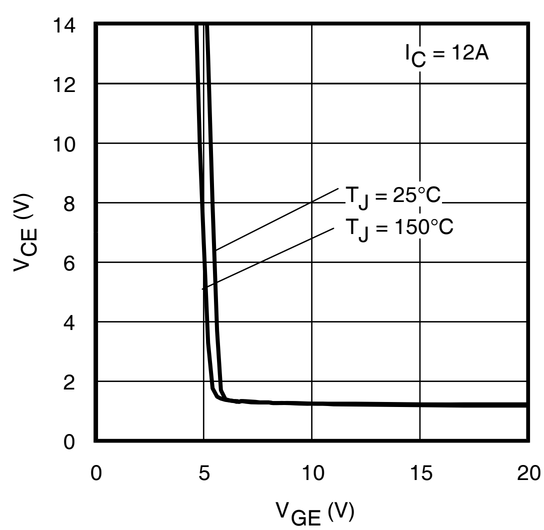


Fig 6. $V_{CE(ON)}$ vs. Gate Voltage

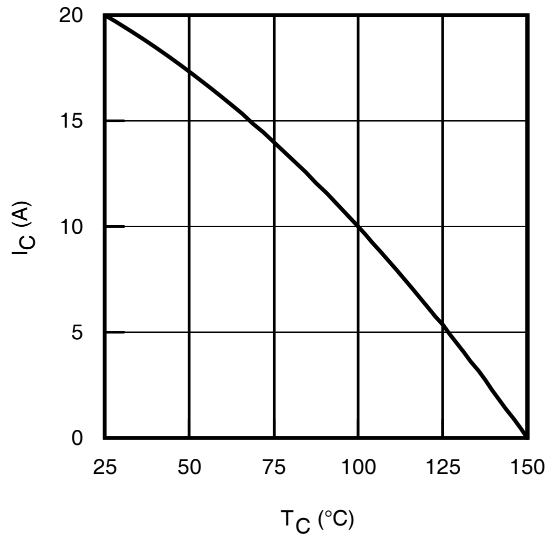


Fig 7. Maximum Collector Current vs. Case Temperature

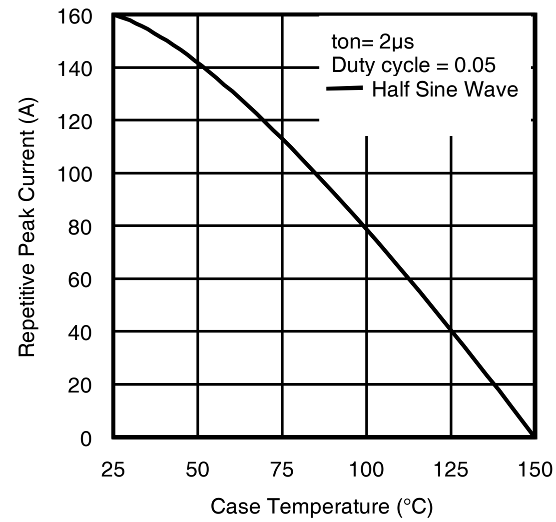


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

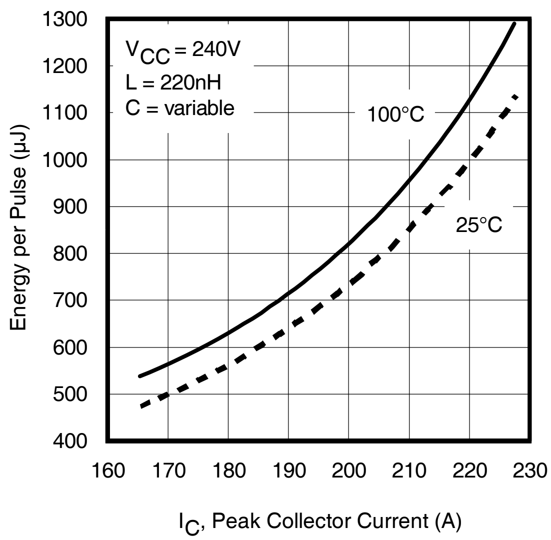


Fig 9. Typical E_{PULSE} vs. Collector Current

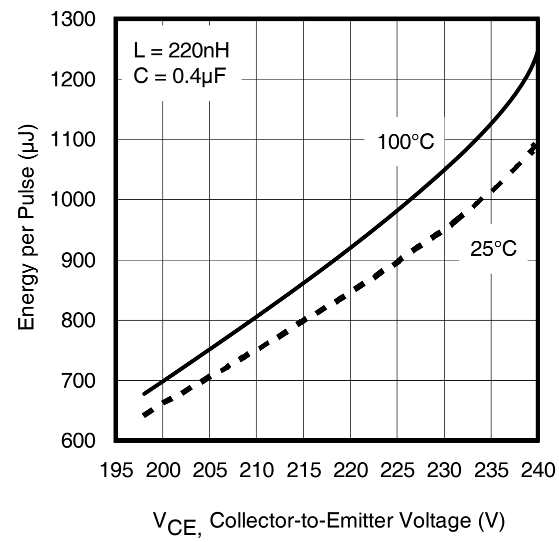


Fig 10. Typical E_{PULSE} vs. Collector-to-Emitter Voltage

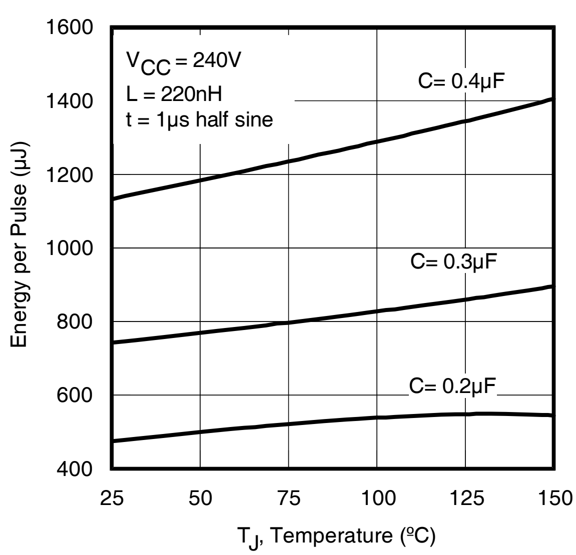


Fig 11. E_{PULSE} vs. Temperature

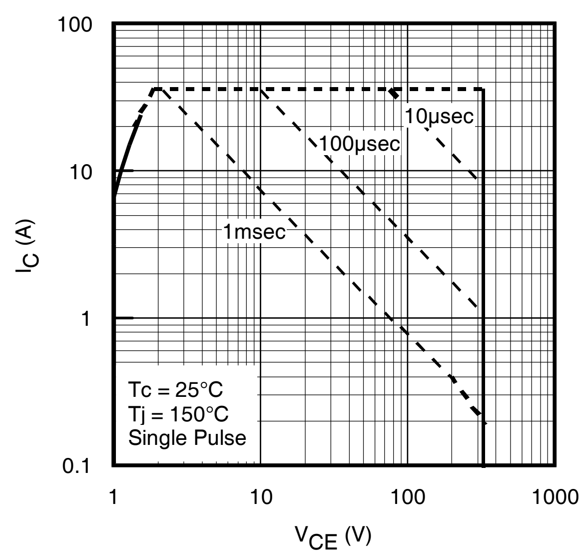


Fig 12. Forward Bias Safe Operating Area

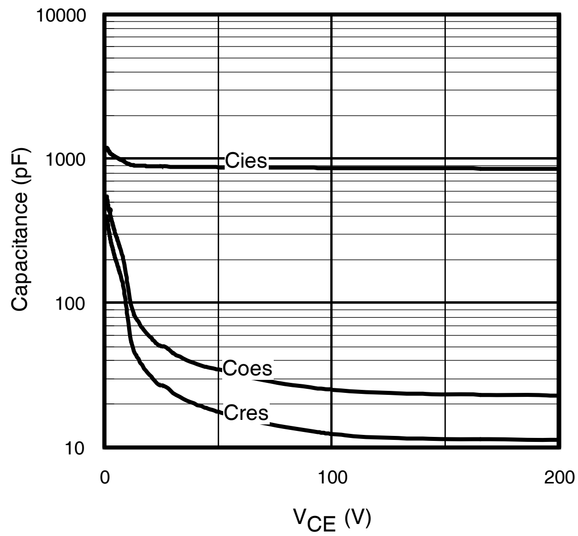


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

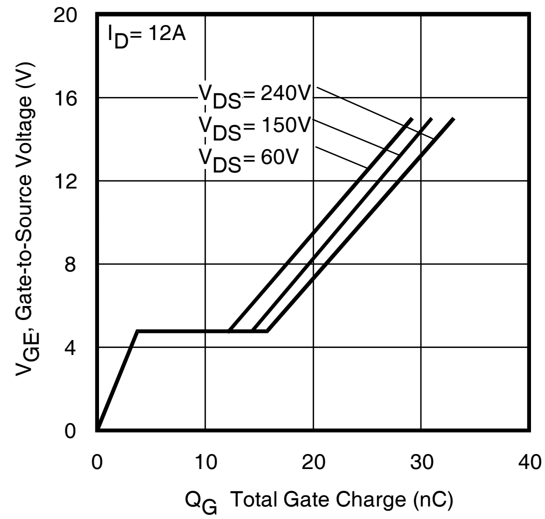


Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

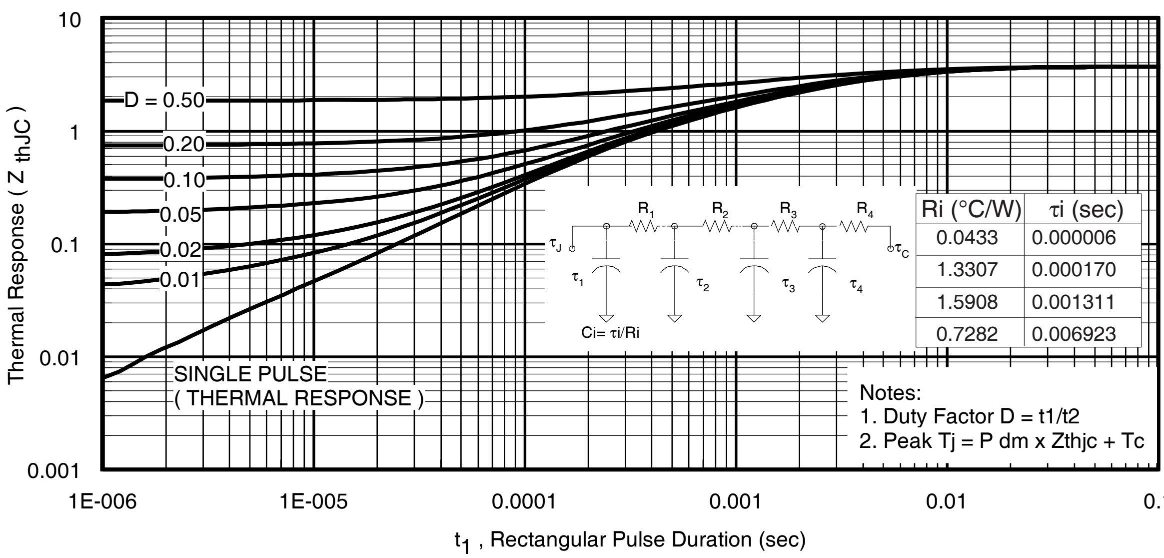


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

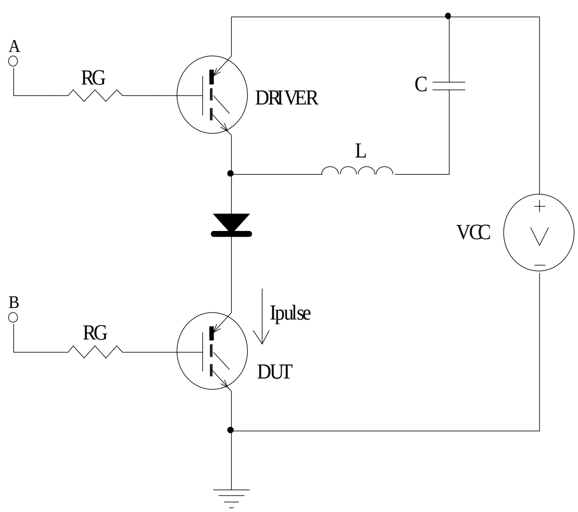


Fig 16a. t_{st} and E_{PULSE} Test Circuit

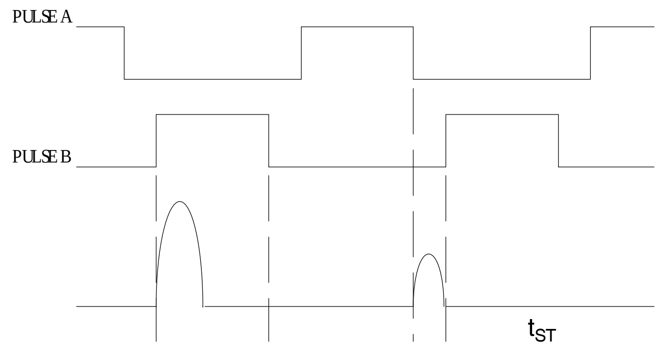


Fig 16b. t_{st} Test Waveforms

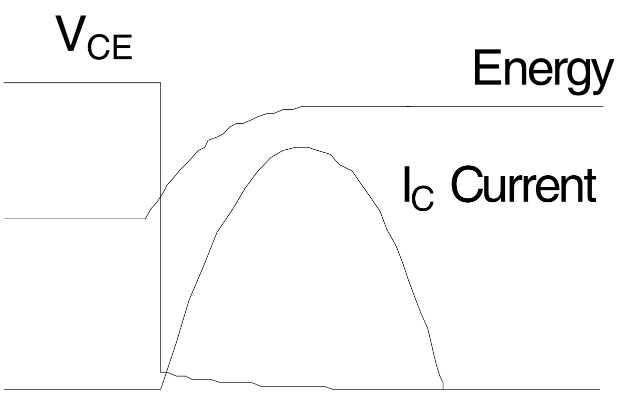


Fig 16c. E_{PULSE} Test Waveforms

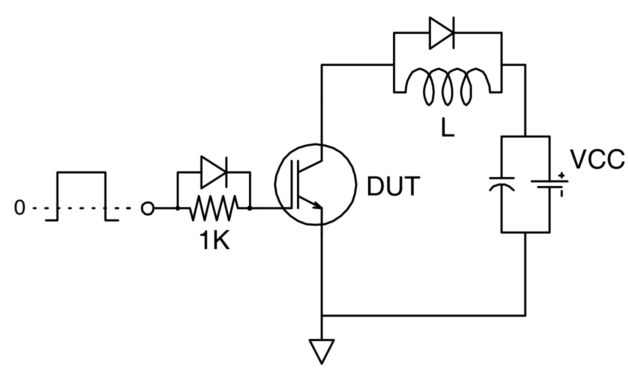
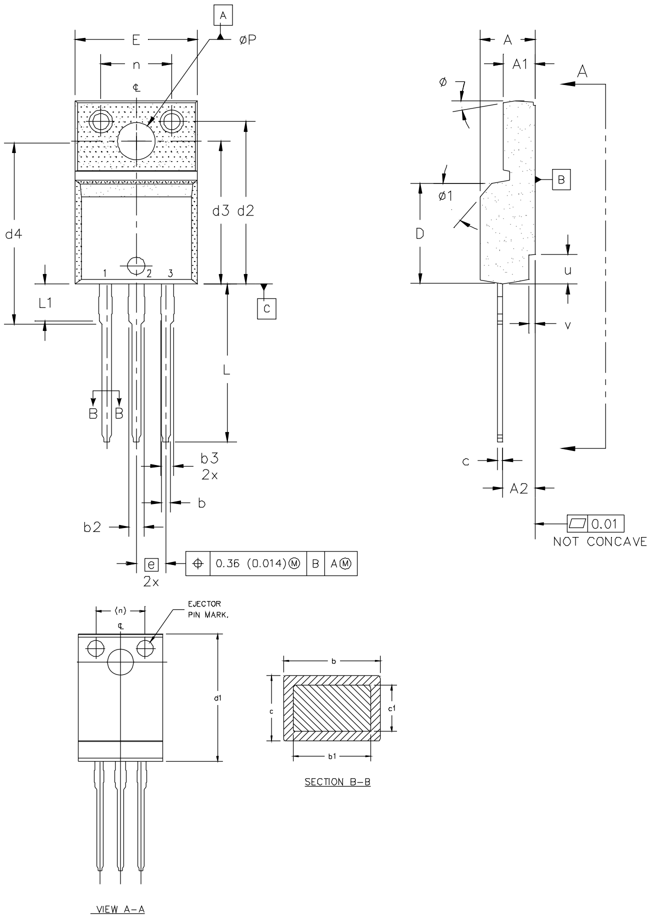


Fig. 17 - Gate Charge Circuit (turn-off)

TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	0.180	0.190	
A1	2.57	2.83	0.101	0.114	
A2	2.51	2.85	0.099	0.112	
b	0.622	0.89	0.024	0.035	
b1	0.622	0.838	0.024	0.033	5
b2	1.229	1.400	0.048	0.055	
b3	1.229	1.400	0.048	0.055	
c	0.440	0.629	0.017	0.025	
c1	0.440	0.584	0.017	0.023	
D	8.65	9.80	0.341	0.386	4
d1	15.80	16.12	0.622	0.635	
d2	13.97	14.22	0.550	0.560	
d3	12.30	12.92	0.484	0.509	
d4	8.64	9.91	0.340	0.390	
E	10.36	10.63	0.408	0.419	4
e	2.54 BSC		0.100 BSC		
L	13.20	13.73	0.520	0.541	
L1	3.10	3.50	0.122	0.138	3
n	6.05	6.15	0.238	0.242	
øP	3.05	3.45	0.120	0.136	
u	2.40	2.50	0.094	0.098	6
v	0.40	0.50	0.016	0.020	6
ø	3°	7°	3°	7°	
ø1		45°		45°	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE

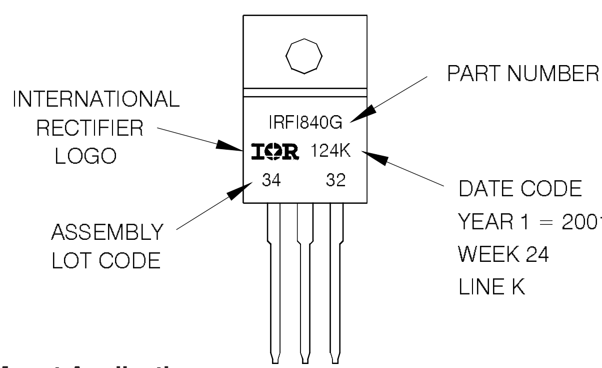
IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24, 2001
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



TO-220 Full-Pak package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Data and specifications subject to change without notice.
This product has been designed for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
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