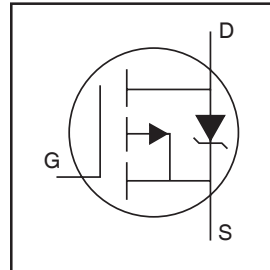


IRL5602SPbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- P-Channel
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

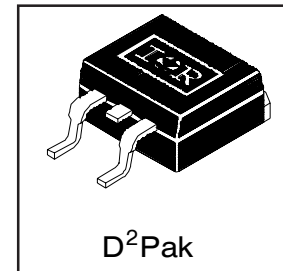


$V_{DSS} = -20V$
$R_{DS(on)} = 0.042\Omega$
$I_D = -24A$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-24	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-17	
I_{DM}	Pulsed Drain Current ①	-96	
$P_D @ T_C = 25^\circ C$	Power Dissipation	75	W
	Linear Derating Factor	0.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 8.0	V
E_{AS}	Single Pulse Avalanche Energy②	290	mJ
I_{AR}	Avalanche Current①	-12	A
E_{AR}	Repetitive Avalanche Energy①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-0.81	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-20	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.013	—	V/°C	Reference to 25°C, I _D = -1mA ^⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.042	Ω	V _{GS} = -4.5V, I _D = -12A ^④
		—	—	0.062		V _{GS} = -2.7V, I _D = -10A ^④
		—	—	0.075		V _{GS} = -2.5V, I _D = -10A ^④
V _{GS(th)}	Gate Threshold Voltage	-0.7	—	-1.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	12	—	—	S	V _{DS} = -15V, I _D = -12A ^⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V _{DS} = -20V, V _{GS} = 0V
		—	—	-250		V _{DS} = -16V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	500	nA	V _{GS} = -8.0V
	Gate-to-Source Reverse Leakage	—	—	-500		V _{GS} = 8.0V
Q _g	Total Gate Charge	—	—	44	nC	I _D = -12A
Q _{gs}	Gate-to-Source Charge	—	—	8.7		V _{DS} = -16V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	19		V _{GS} = -4.5V, See Fig. 6 and 13 ^{④⑤}
t _{d(on)}	Turn-On Delay Time	—	9.7	—	ns	V _{DD} = -10 V
t _r	Rise Time	—	73	—		I _D = -12A
t _{d(off)}	Turn-Off Delay Time	—	53	—		R _G = 6.0Ω, V _{GS} = 4.5V
t _f	Fall Time	—	84	—		R _D = 0.8Ω, See Fig. 10 ^{④⑤}
L _S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	—	1460	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	790	—		V _{DS} = -15V
C _{rss}	Reverse Transfer Capacitance	—	370	—		f = 1.0MHz, See Fig. 5 ^⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-24	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	-96		
V _{SD}	Diode Forward Voltage	—	—	-1.4	V	T _J = 25°C, I _S = -12A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	58	88	ns	T _J = 25°C, I _F = -12A
Q _{rr}	Reverse Recovery Charge	—	54	81	nC	di/dt = -100A/μs ^④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 3.0mH
R_G = 25Ω, I_{AS} = -14A. (See Figure 12)
- ③ I_{SD} ≤ -12A, di/dt ≤ 120A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

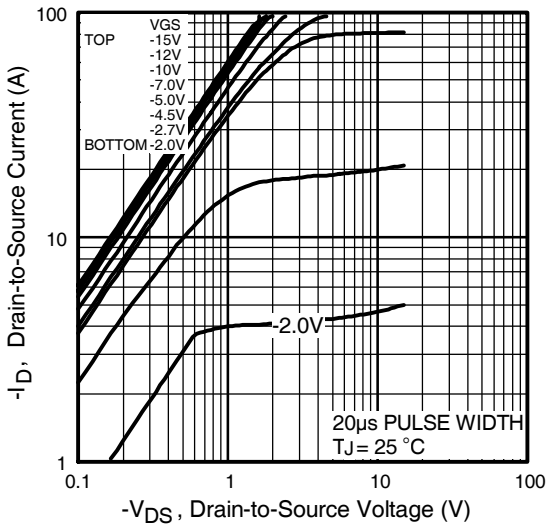


Fig 1. Typical Output Characteristics

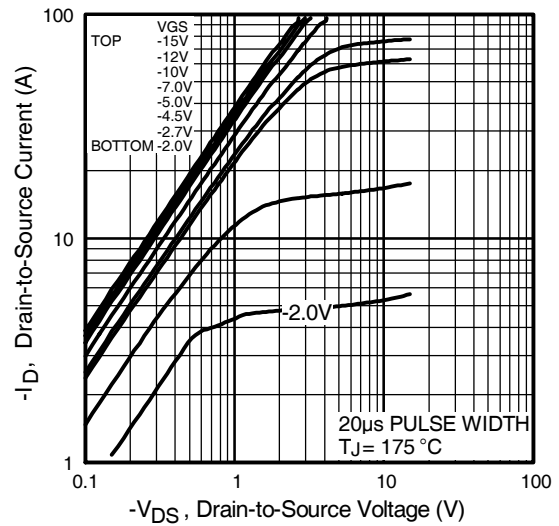


Fig 2. Typical Output Characteristics

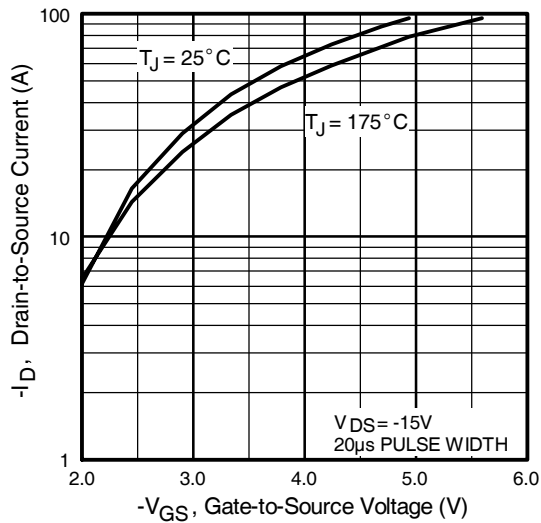


Fig 3. Typical Transfer Characteristics

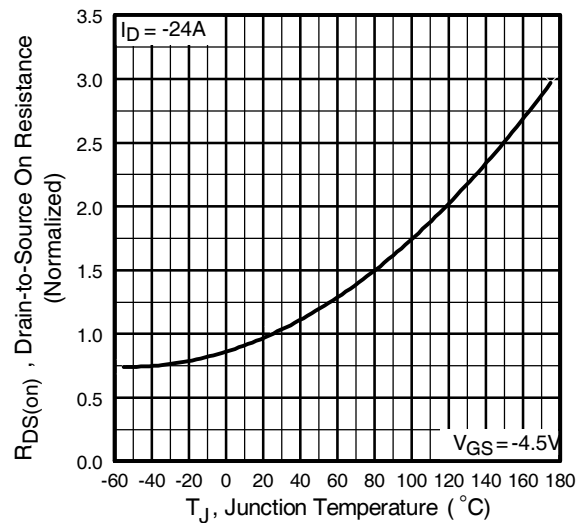


Fig 4. Normalized On-Resistance Vs. Temperature

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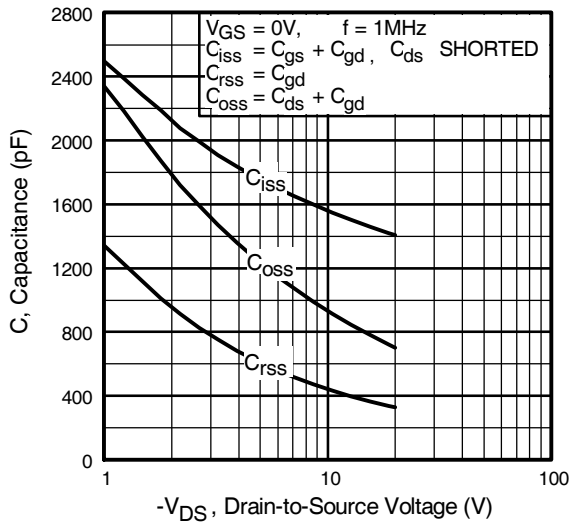


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

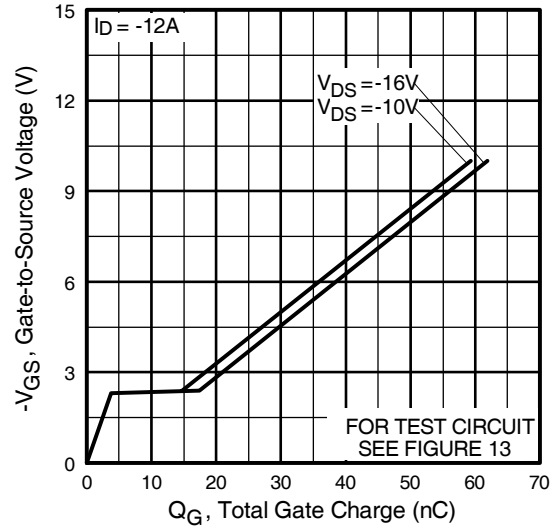


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

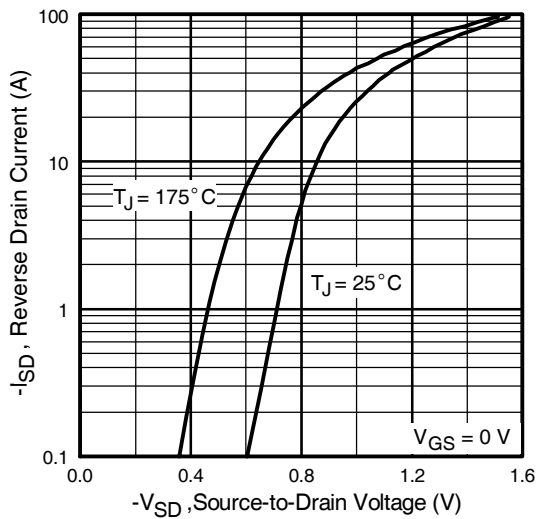


Fig 7. Typical Source-Drain Diode Forward Voltage

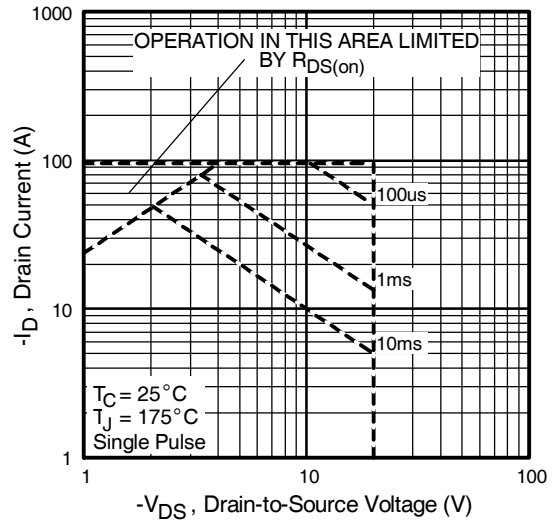


Fig 8. Maximum Safe Operating Area

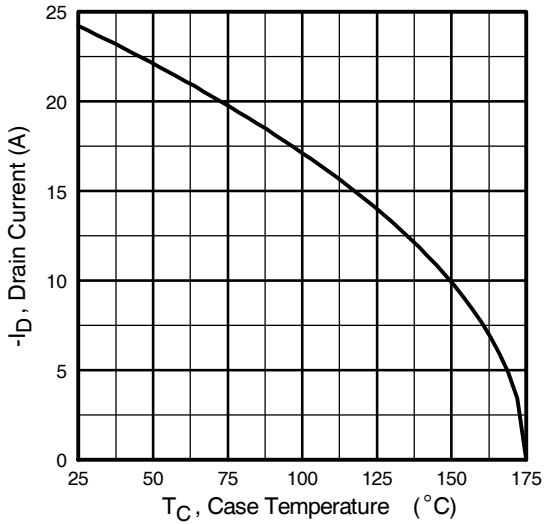


Fig 9. Maximum Drain Current Vs. Case Temperature

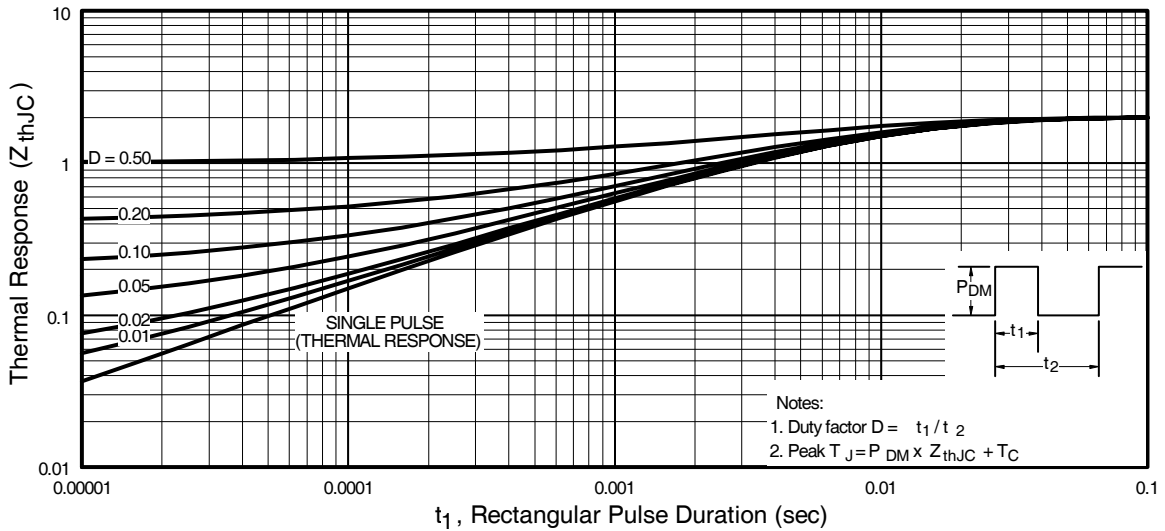
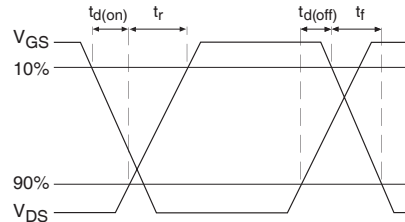
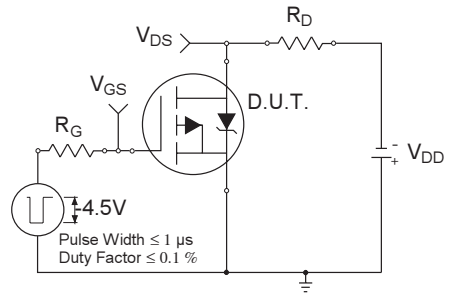


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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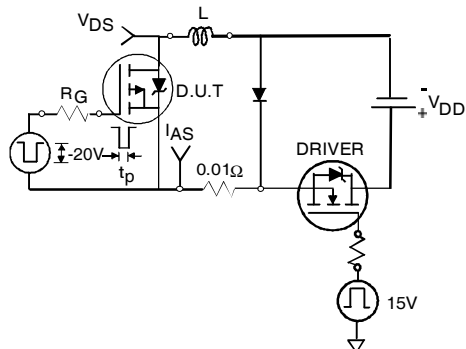


Fig 12a. Unclamped Inductive Test Circuit

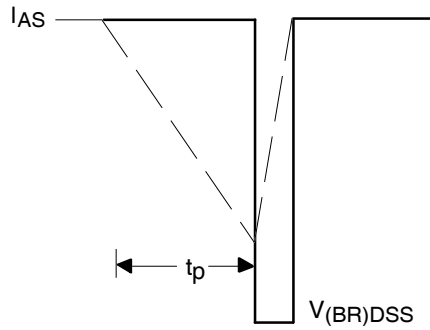


Fig 12b. Unclamped Inductive Waveforms

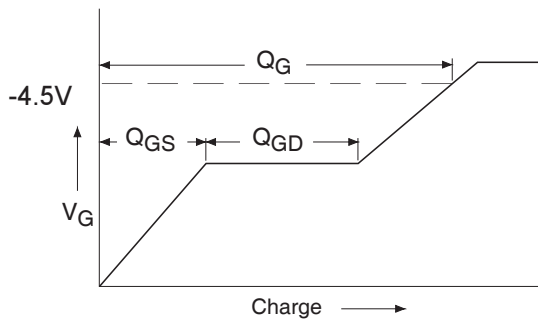


Fig 13a. Basic Gate Charge Waveform

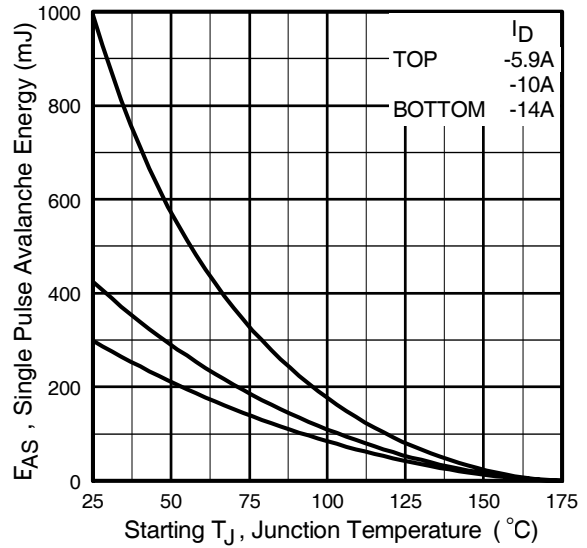


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

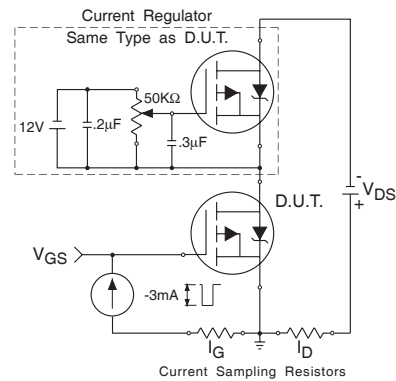
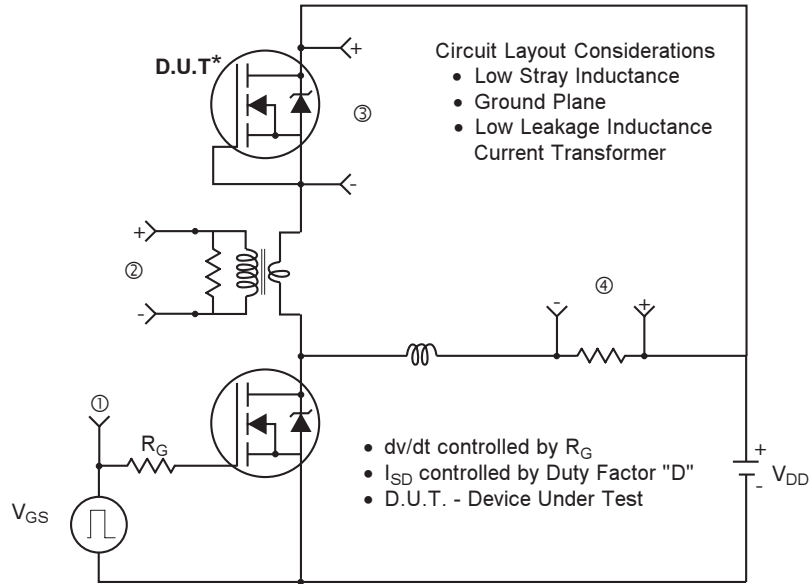
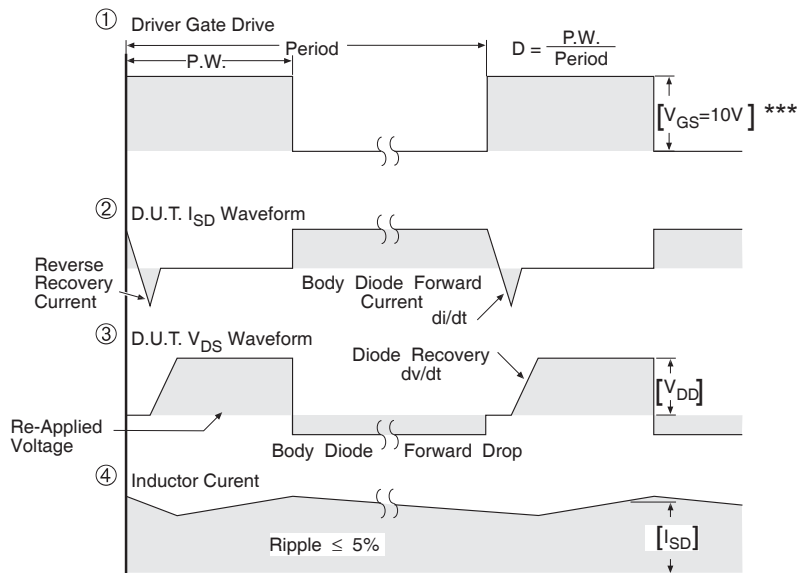


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



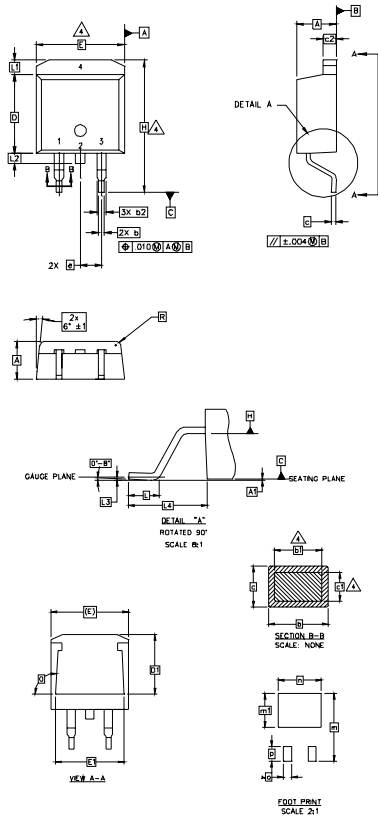
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

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D²Pak Package Outline



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190	4	
A1	0.00	0.254	.000	.010		
b	0.51	0.99	.020	.039		
b1	0.51	0.89	.020	.035		
b2	1.14	1.78	.045	.070		
c	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023		
c2	1.14	1.65	.045	.065		
D	8.51	9.65	.335	.380		3
D1	6.86		.270			3
E	9.65	10.67	.380	.420		
E1	6.22		.245			
e	2.54 BSC		.100 BSC			
h	14.61	15.88	.575	.625		
l	1.78	2.79	.070	.110		
l1		1.65		.065		
l2	1.27	1.78	.050	.070		
l3	0.25 BSC		.010 BSC			
l4	4.78	5.28	.188	.208	3	
m	17.78		.700			
m1	8.89		.350			
n	11.43		.450			
o	2.08		.082			
p	3.81		.150			
R	0.51	0.71	.020	.028		
θ	90°	93°	90°	93°		

LEAD ASSIGNMENTS

HEXFEEET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

IGBTs, CqPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

DIODES

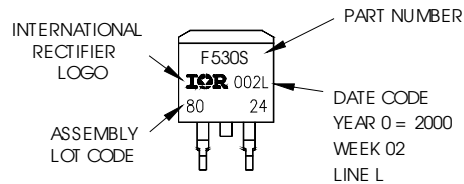
- 1.- ANODE *
- 2, 4.- CATHODE
- 3.- ANODE

* PART DEPENDENT.

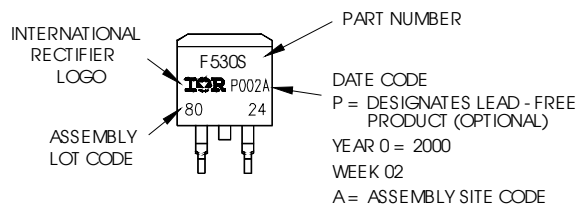
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON VVV02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position
indicates "Lead - Free"

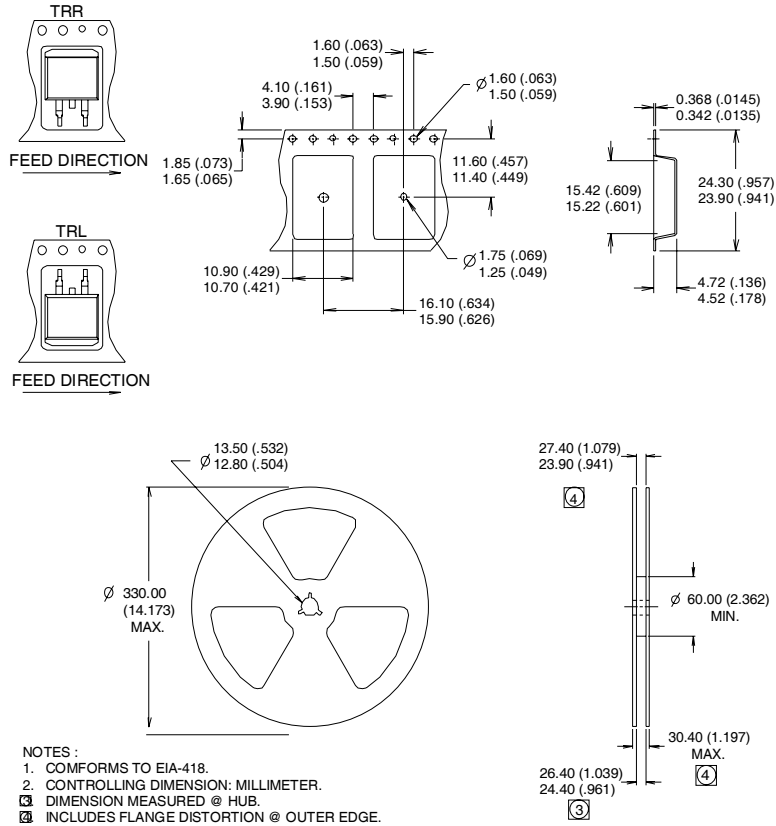


OR



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D²Pak Tape & Reel Information



Data and specifications subject to change without notice.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>