

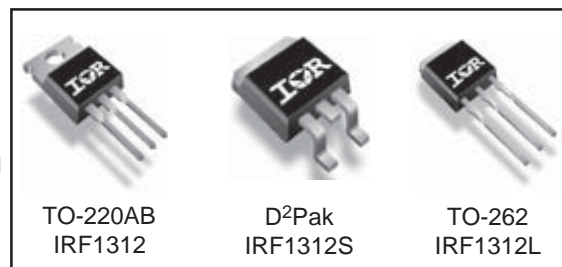
Applications

- High frequency DC-DC converters
- Motor Control
- Uninterruptible Power Supplies

V_{DSS}	$R_{DS(on) \max}$	I_D
80V	10m Ω	95A [ⓐ]

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	95 [ⓐ]	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	67 [ⓐ]	
I_{DM}	Pulsed Drain Current [ⓑ]	380	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation [ⓐ]	3.8	W
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	210	
	Linear Derating Factor	1.4	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt [ⓐ]	5.1	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.73	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface [ⓐ]	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient [ⓐ]	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) [ⓐ]	—	40	

Notes [ⓑ] through [ⓐ] are on page 11

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7/01/02

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	80	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.078	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	6.6	10	mΩ	V _{GS} = 10V, I _D = 57A ④
V _{GS(th)}	Gate Threshold Voltage	3.5	—	5.5	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 76V, V _{GS} = 0V
		—	—	250		V _{DS} = 64V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V

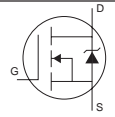
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	92	—	—	S	V _{DS} = 25V, I _D = 57A
Q _g	Total Gate Charge	—	93	140	nC	I _D = 57A
Q _{gs}	Gate-to-Source Charge	—	36	—		V _{DS} = 40V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	34	—		V _{GS} = 10V, ④
t _{d(on)}	Turn-On Delay Time	—	25	—	ns	V _{DD} = 40V
t _r	Rise Time	—	130	—		I _D = 57A
t _{d(off)}	Turn-Off Delay Time	—	47	—		R _G = 4.5Ω
t _f	Fall Time	—	51	—		V _{GS} = 10V ④
C _{iss}	Input Capacitance	—	5450	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	550	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	340	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	1910	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	380	—		V _{GS} = 0V, V _{DS} = 64V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	620	—		V _{GS} = 0V, V _{DS} = 0V to 64V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②⑥	—	250	mJ
I _{AR}	Avalanche Current①	—	57	A
E _{AR}	Repetitive Avalanche Energy①	—	21	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	95⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	380		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 57A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	64	96	ns	T _J = 25°C, I _F = 57A
Q _{rr}	Reverse Recovery Charge	—	150	230	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

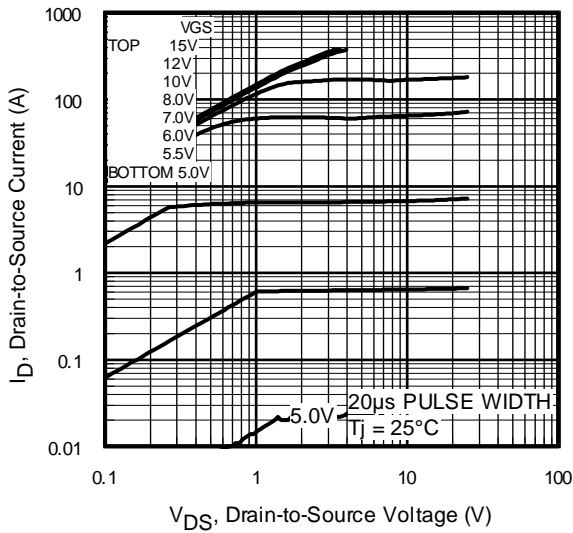


Fig 1. Typical Output Characteristics

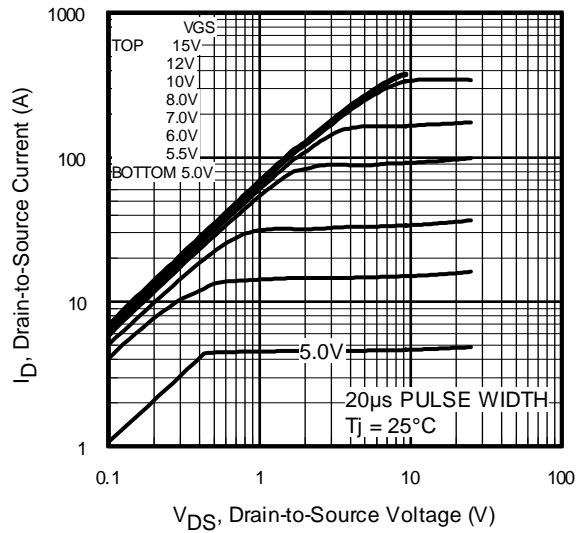


Fig 2. Typical Output Characteristics

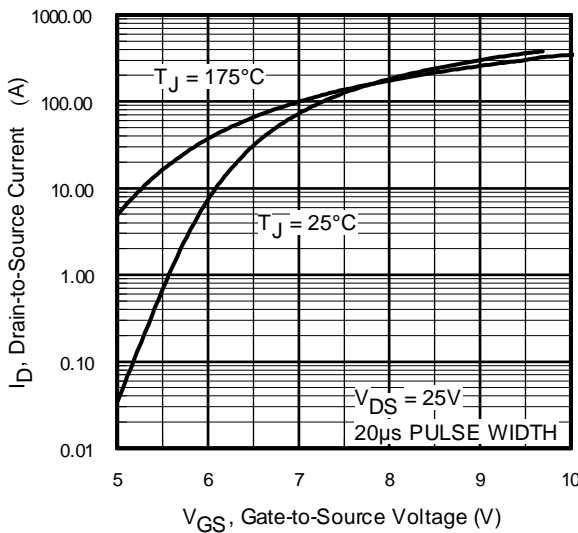


Fig 3. Typical Transfer Characteristics

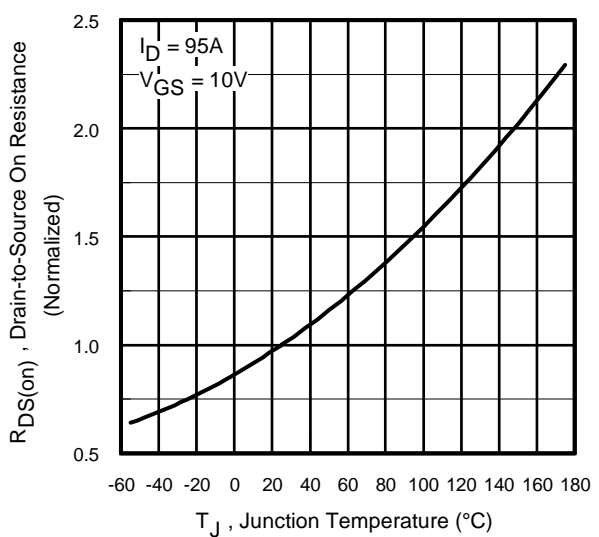


Fig 4. Normalized On-Resistance Vs. Temperature

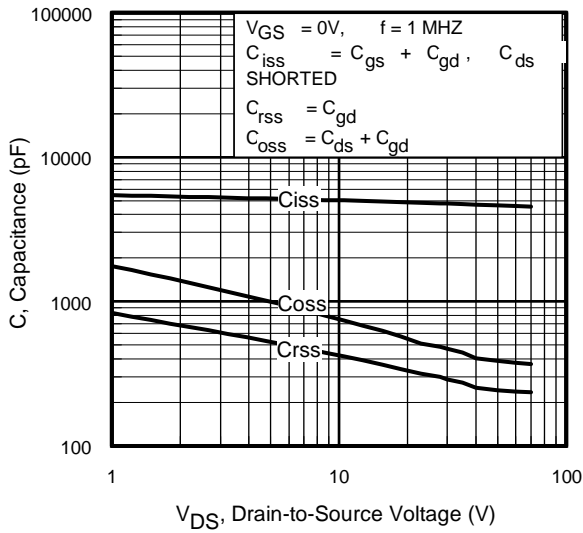


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

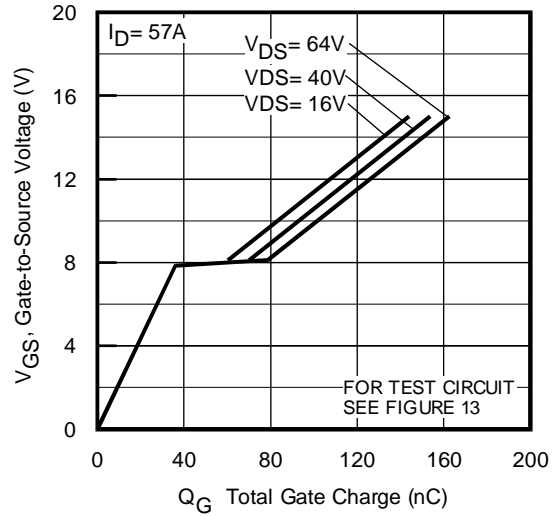


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

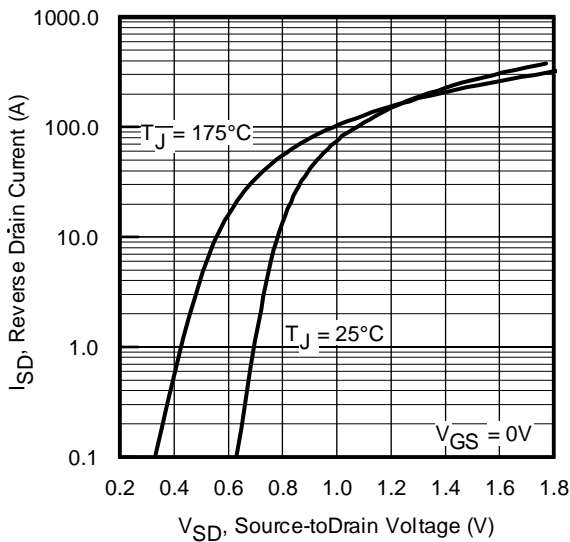


Fig 7. Typical Source-Drain Diode Forward Voltage

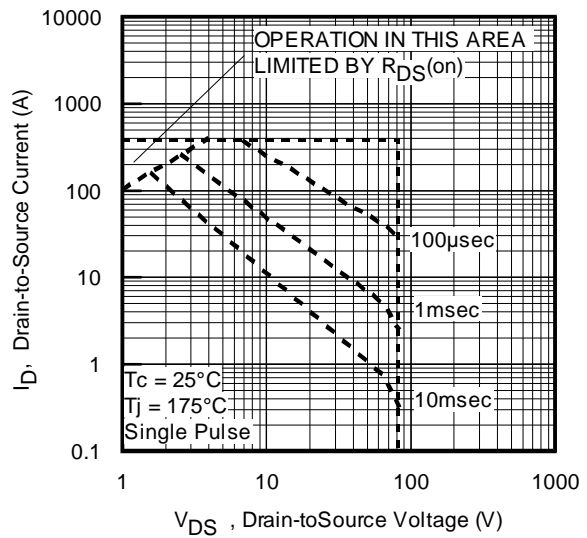


Fig 8. Maximum Safe Operating Area

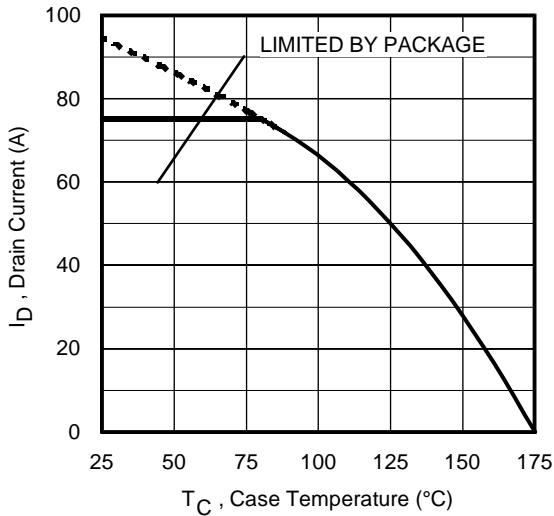


Fig 9. Maximum Drain Current Vs. Case Temperature

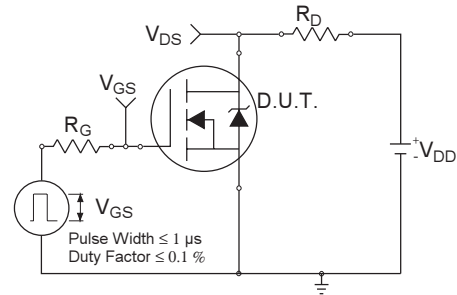


Fig 10a. Switching Time Test Circuit

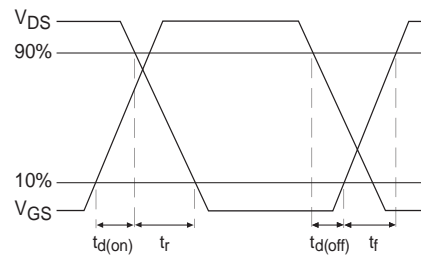


Fig 10b. Switching Time Waveforms

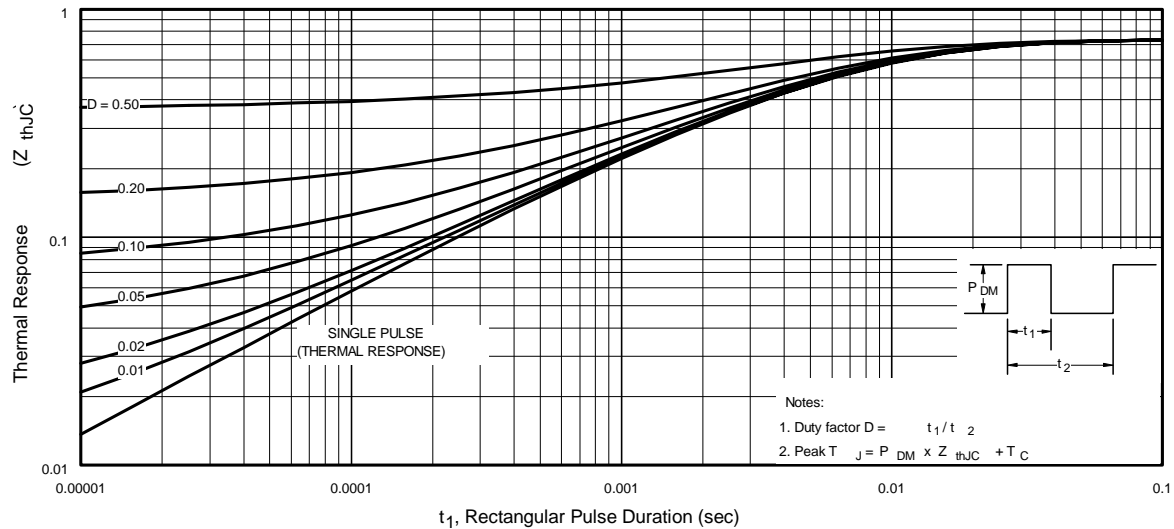


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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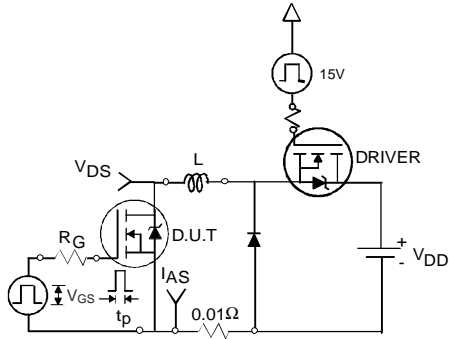


Fig 12a. Unclamped Inductive Test Circuit

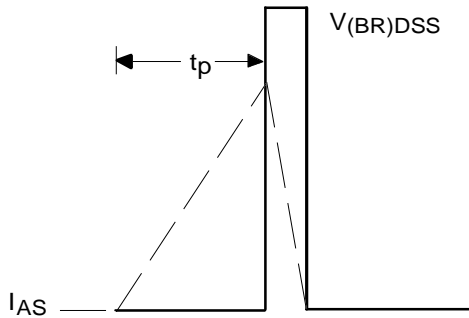


Fig 12b. Unclamped Inductive Waveforms

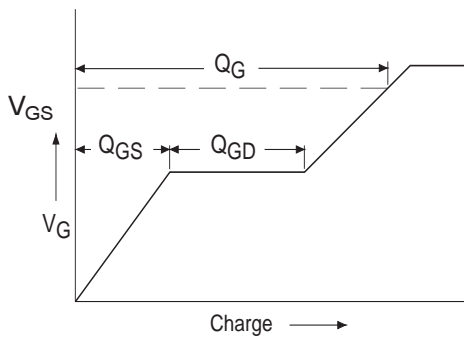


Fig 13a. Basic Gate Charge Waveform

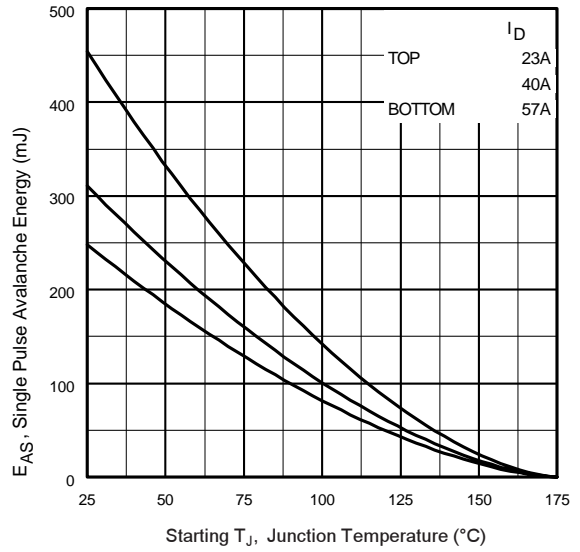


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

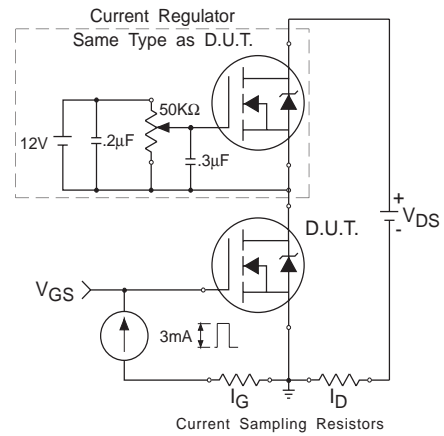
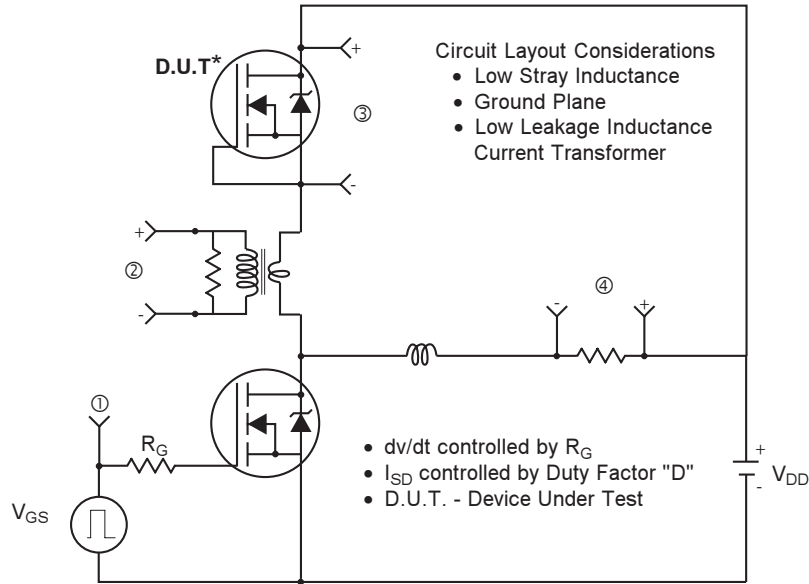
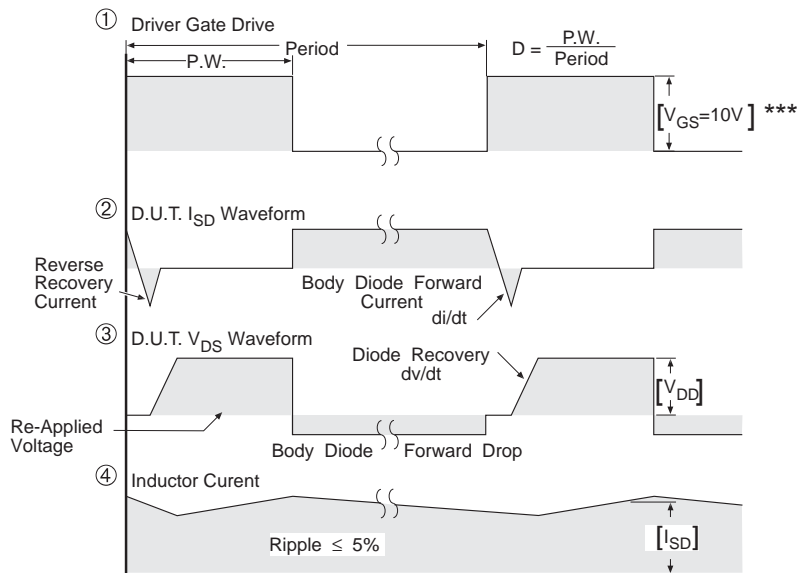


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



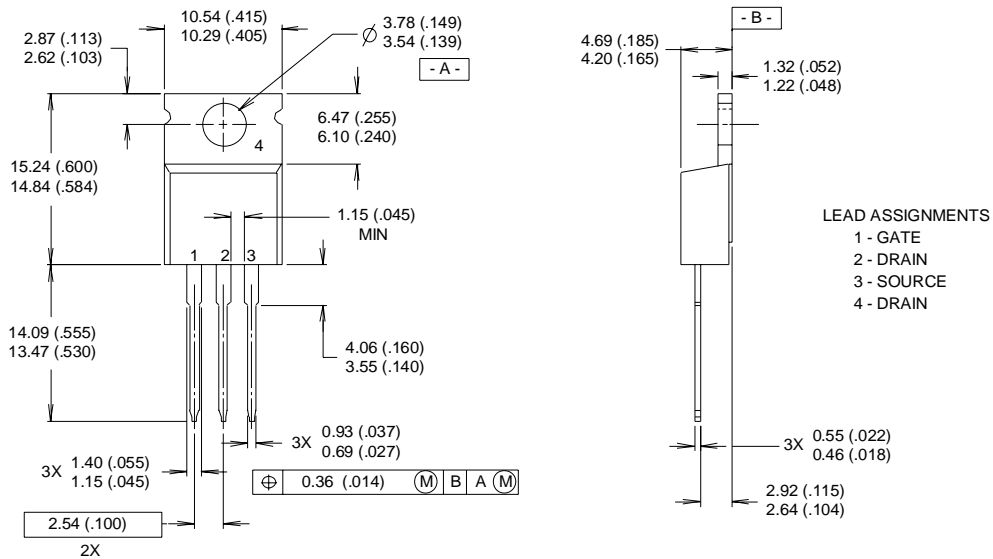
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

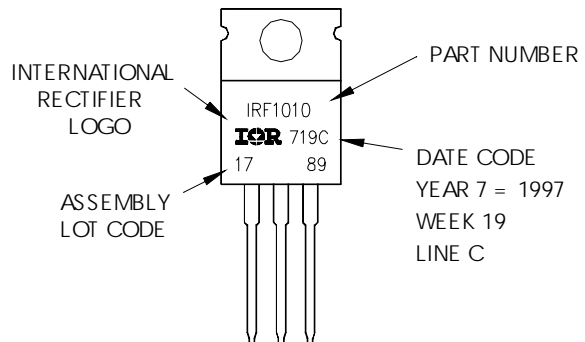


NOTES:

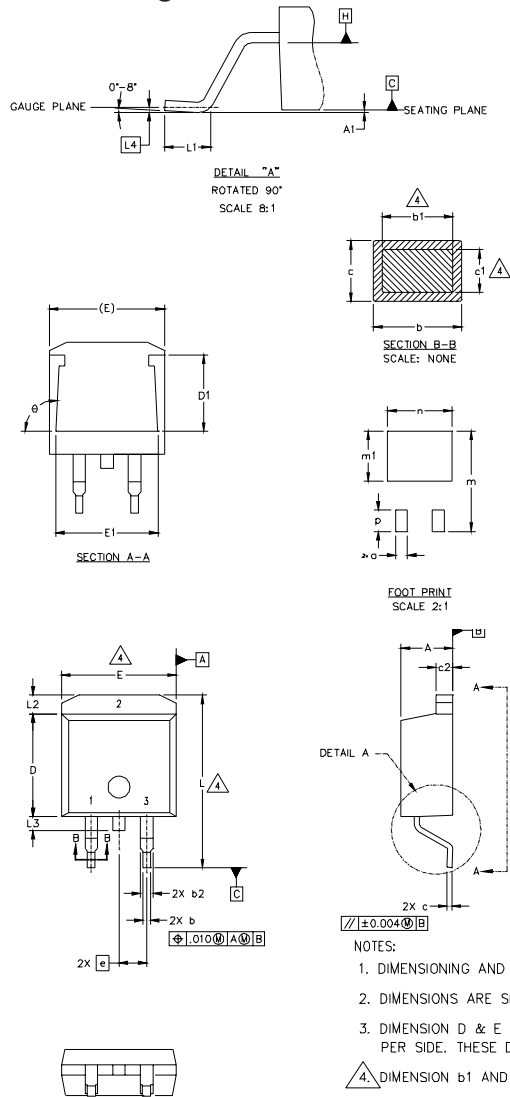
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



D²Pak Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127	.005	3	
b	0.51	0.99	.020		
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.74	.015	.029	
c1	0.43	0.63	.017	.025	3
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

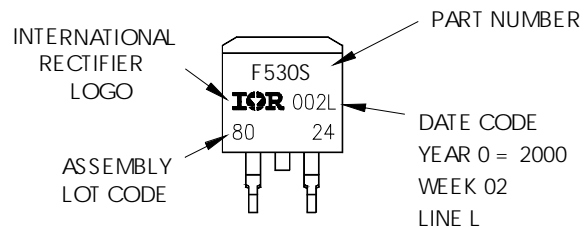
* PART DEPENDENT.

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
- CONTROLLING DIMENSION: INCH.

D²Pak Part Marking Information

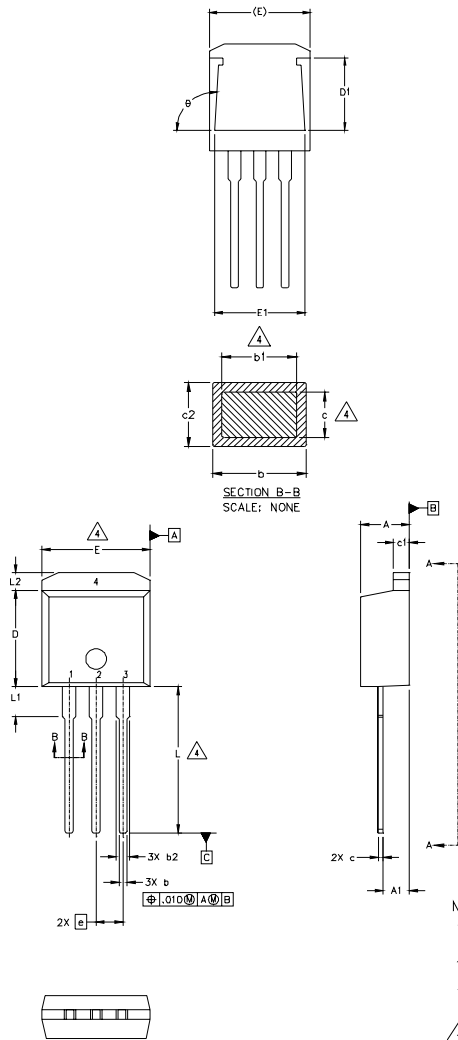
EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"



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TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

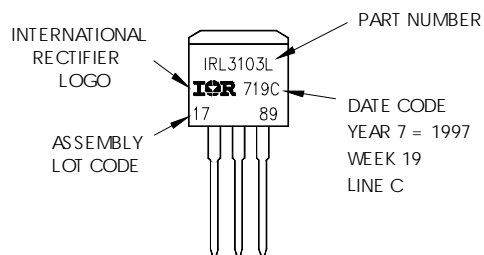
HEXFET	IGBT
1.- GATE	1- GATE
2.- DRAIN	2- COLLECTOR
3.- SOURCE	3- EMITTER
4.- DRAIN	4- COLLECTOR

NOTES:

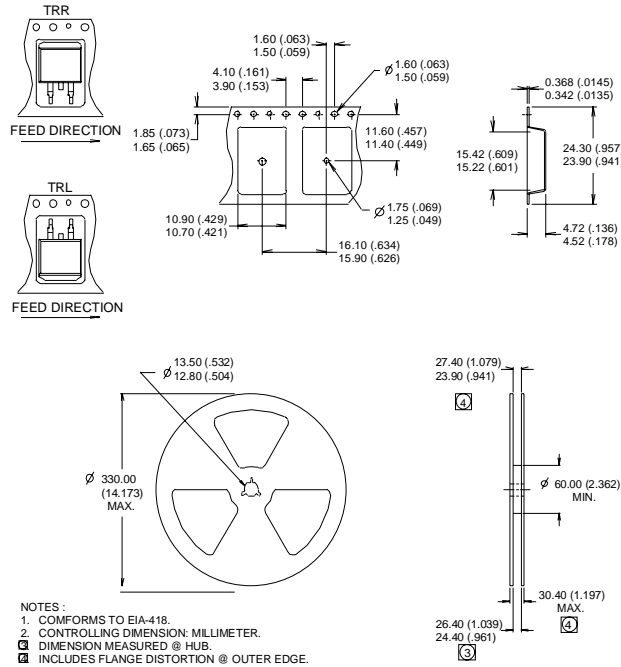
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [“.005”] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
- CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.15\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 57\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 57\text{A}$, $di/dt \leq 410\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑦ This is only applied to TO-220AB package
- ⑧ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

TO-220AB package is not recommended for Surface Mount Application

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.7/02

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>