

# **High Speed IGBT3 Chip**

## Features:

- 650V Trench & Field Stop technology
- high speed switching series third generation
- low V<sub>CE(sat)</sub>
- low EMI
- low turn-off losses
- positive temperature coefficient
- qualified according to JEDEC for target applications

#### Recommended for:

 discrete components and modules

# **Applications:**

- uninterruptible power supplies
- welding converters
- converters with high switching frequency



Chip Type	<b>V</b> <sub>CE</sub>	<i>I</i> <sub>Cn</sub> <sup>1)</sup>	Die Size	Package
IGC28T65QE	650V	50A	6.57 x 4.2 mm <sup>2</sup>	sawn on foil

<sup>&</sup>lt;sup>1)</sup>nominal collector current at Tc = 100°C, not subject to production test - verified by design/characterization

# **Mechanical Parameters**

Die size		6.57 x 4.2	_		
Emitter pad size		See chip drawing	2		
Gate pad size		0.817 x 1.52	mm <sup>2</sup>		
Area total		27.59			
Thickness		70	μm		
Wafer size		200	mm		
Max.possible chips per wafer		974			
Passivation frontside		Photoimide			
Pad metal		3200 nm AlSiCu			
Backside metal		Ni Ag –system			
Die bond		Electrically conductive epoxy glue and soft solder			
Wire bond		Al, <500μm			
Reject ink dot size		∅ 0.65mm ; max 1.2mm			
Character and inches	for original and sealed MBB bags	Ambient atmosphere air, Temperature 17°C – 25°C, < 6 month			
Storage environment	for open MBB bags	Acc. to IEC62258-3: Atmosphere >99% Nitrogen or inert gas, Humidity <25%RH, Temperature 17°C – 25°C, < 6 month			

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## **Maximum Ratings**

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, $T_{\rm vj}$ =25 °C	V <sub>CE</sub>	650	V
DC collector current, limited by $T_{\rm vjmax}$	I <sub>C</sub>	1)	А
Pulsed collector current, $t_{\rm p}$ limited by $T_{\rm vjmax}^{\ \ 2}$	$I_{c,puls}$	150	Α
Gate emitter voltage	$V_{GE}$	±20	V
Operating junction temperature	$T_{vj}$	-40 <b>+</b> 175	°C
Short circuit data <sup>2) 3)</sup> $V_{GE} = 15V$ , $V_{CC} = 400V$ , $T_{vj} = 150$ °C	tsc	5	μs

<sup>1)</sup> depending on thermal properties of assembly

# Static Characteristics (tested on wafer), $T_{vj}$ =25 °C

Parameter	Symbol	Conditions	Value			Unit
Tarameter			min.	typ.	max.	
Collector-Emitter breakdown voltage	V <sub>(BR)CES</sub>	$V_{\rm GE}$ =0V , $I_{\rm C}$ =2 mA	650			
Collector-Emitter saturation voltage	V <sub>CEsat</sub>	V <sub>GE</sub> =15V, I <sub>C</sub> =50A	1.38	1.85	2.22	V
Gate-Emitter threshold voltage	$V_{\rm GE(th)}$	$I_{\rm C}$ =0.8mA , $V_{\rm GE}$ = $V_{\rm CE}$	4.2	5.1	5.6	
Zero gate voltage collector current	I <sub>CES</sub>	V <sub>CE</sub> =650V , V <sub>GE</sub> =0V			2.8	μA
Gate-Emitter leakage current	I <sub>GES</sub>	V <sub>CE</sub> =0V , V <sub>GE</sub> =20V			150	nA
Integrated gate resistor	$r_{\rm G}$			none		Ω

# **Electrical Characteristics** (not subject to production test - verified by design / characterization)

Parameter	Symbol	Conditions	Value			Linit
Parameter			min.	typ.	max.	Unit
Collector-Emitter saturation voltage	V <sub>CEsat</sub>	$V_{\text{GE}}$ =15V, $I_{\text{C}}$ =50A, $T_{\text{vj}}$ =175 °C		2.25		V
Input capacitance	Cies	$V_{CE}$ =25V, $V_{GE}$ =0V, $f$ =1MHz		3100		pF
Reverse transfer capacitance	C <sub>res</sub>	$T_{\text{vj}} = 25 ^{\circ}\text{C}$		90		] Pi

## **Further Electrical Characteristic**

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

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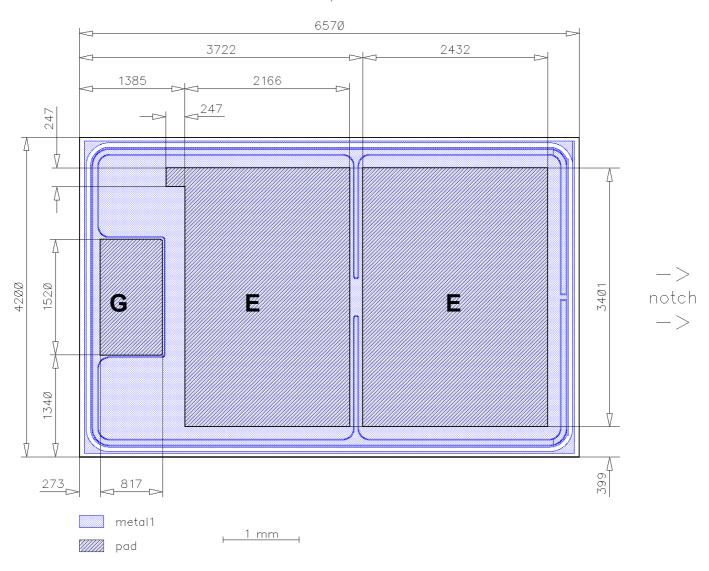
<sup>&</sup>lt;sup>2)</sup> not subject to production test - verified by design/characterization

<sup>&</sup>lt;sup>3)</sup> allowed number of short circuits: <1000; time between short circuits: >1s.



# **Chip Drawing**





**E** = Emitter

**G** = Gate



Description
AQL 0,65 for visual inspection according to failure catalogue
Electrostatic Discharge Sensitive Device according to MIL-STD 883

## **Revision History**

Version	Subjects (major changes since last revision)	Date

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