

## MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## CoolMOS™ CE

800V CoolMOS™ CE Power Transistor  
IPA80R310CE

## Data Sheet

Rev. 2.1  
Final

Power Management & Multimarket

## 1 Description

CoolMOS™ CE is a revolutionary technology for high voltage power MOSFETs. The high voltage capability combines safety with performance and ruggedness to allow stable designs at highest efficiency level. CoolMOS™ 800V CE comes with selected package choice offering the benefit of reduced system costs and higher power density designs.

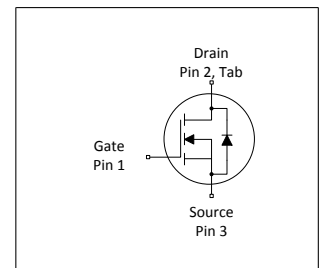
### Features

- High voltage technology
- Extreme  $dv/dt$  rated
- High peak current capability
- Low gate charge
- Low effective capacitances
- Pb-free plating, RoHS Compliant, Halogen free mold compound
- Qualified for consumer grade applications

### Applications

LED Lighting and Adapter in QR Flyback topology

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_J=25^{\circ}C$	800	V
$R_{DS(on),max}$	310	$m\Omega$
$Q_{g,typ}$	91	nC
$I_{D,pulse}$	51	A
$E_{oss}@400V$	6.7	$\mu J$
Body diode $di/dt$	400	$A/\mu s$

Type / Ordering Code	Package	Marking	Related Links
IPA80R310CE	PG-TO 220 FullPAK	8R310CE	see Appendix A



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## 2 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	16.7 10.6	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	51	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	670	mJ	$I_D=3.4\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.50	mJ	$I_D=3.4\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, repetitive	$I_{AR}$	-	-	3.40	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots640\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	35	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	$I_S$	-	-	16.7	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	51	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	4	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	400	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage for TO-220FP	$V_{ISO}$	-	-	2500	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max} < 150^\circ\text{C}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_\theta$

### 3 Thermal characteristics

**Table 3 Thermal characteristics TO-220 FullPAK**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	3.6	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

## 4 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	$V_{GS}=0\text{V}$ , $I_D=0.25\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	2.1	3.0	3.9	V	$V_{DS}=V_{GS}$ , $I_D=1\text{mA}$
Zero gate voltage drain current	$I_{DSS}$	-	-	25 250	$\mu\text{A}$	$V_{DS}=800$ , $V_{GS}=0\text{V}$ , $T_j=25^\circ\text{C}$ $V_{DS}=800$ , $V_{GS}=0\text{V}$ , $T_j=150^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20\text{V}$ , $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.25 0.78	0.31 -	$\Omega$	$V_{GS}=10\text{V}$ , $I_D=11\text{A}$ , $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$ , $I_D=11\text{A}$ , $T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	0.7	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	2320	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=100\text{V}$ , $f=1\text{MHz}$
Output capacitance	$C_{oss}$	-	90	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=100\text{V}$ , $f=1\text{MHz}$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	59	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=0\dots480\text{V}$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	124	-	pF	$I_D=\text{constant}$ , $V_{GS}=0\text{V}$ , $V_{DS}=0\dots480\text{V}$
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=16.7\text{A}$ , $R_G=4.7\Omega$ ; see table 9
Rise time	$t_r$	-	15	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=16.7\text{A}$ , $R_G=4.7\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	72	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=16.7\text{A}$ , $R_G=4.7\Omega$ ; see table 9
Fall time	$t_f$	-	6	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=16.7\text{A}$ , $R_G=4.7\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	12	-	nC	$V_{DD}=640\text{V}$ , $I_D=16.7\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate to drain charge	$Q_{gd}$	-	46	-	nC	$V_{DD}=640\text{V}$ , $I_D=16.7\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate charge total	$Q_g$	-	91	-	nC	$V_{DD}=640\text{V}$ , $I_D=16.7\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate plateau voltage	$V_{plateau}$	-	6.0	-	V	$V_{DD}=640\text{V}$ , $I_D=16.7\text{A}$ , $V_{GS}=0$ to $10\text{V}$

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 480V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 480V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	1	-	V	$V_{GS}=0V, I_F=16.7A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	550	-	ns	$V_R=400V, I_F=16.7A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	15	-	$\mu C$	$V_R=400V, I_F=16.7A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	51	-	A	$V_R=400V, I_F=16.7A, di_F/dt=100A/\mu s$ ; see table 8

### 5 Electrical characteristics diagrams

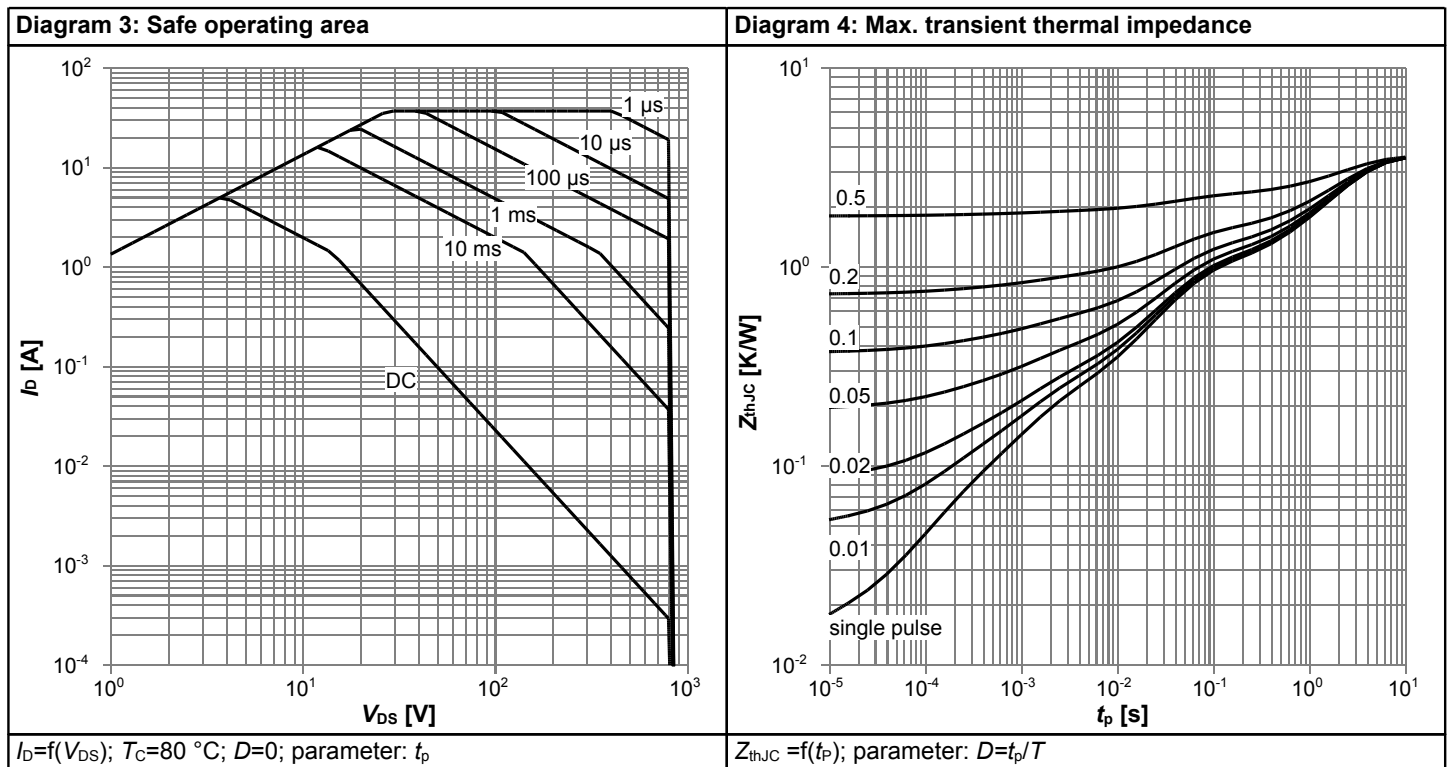
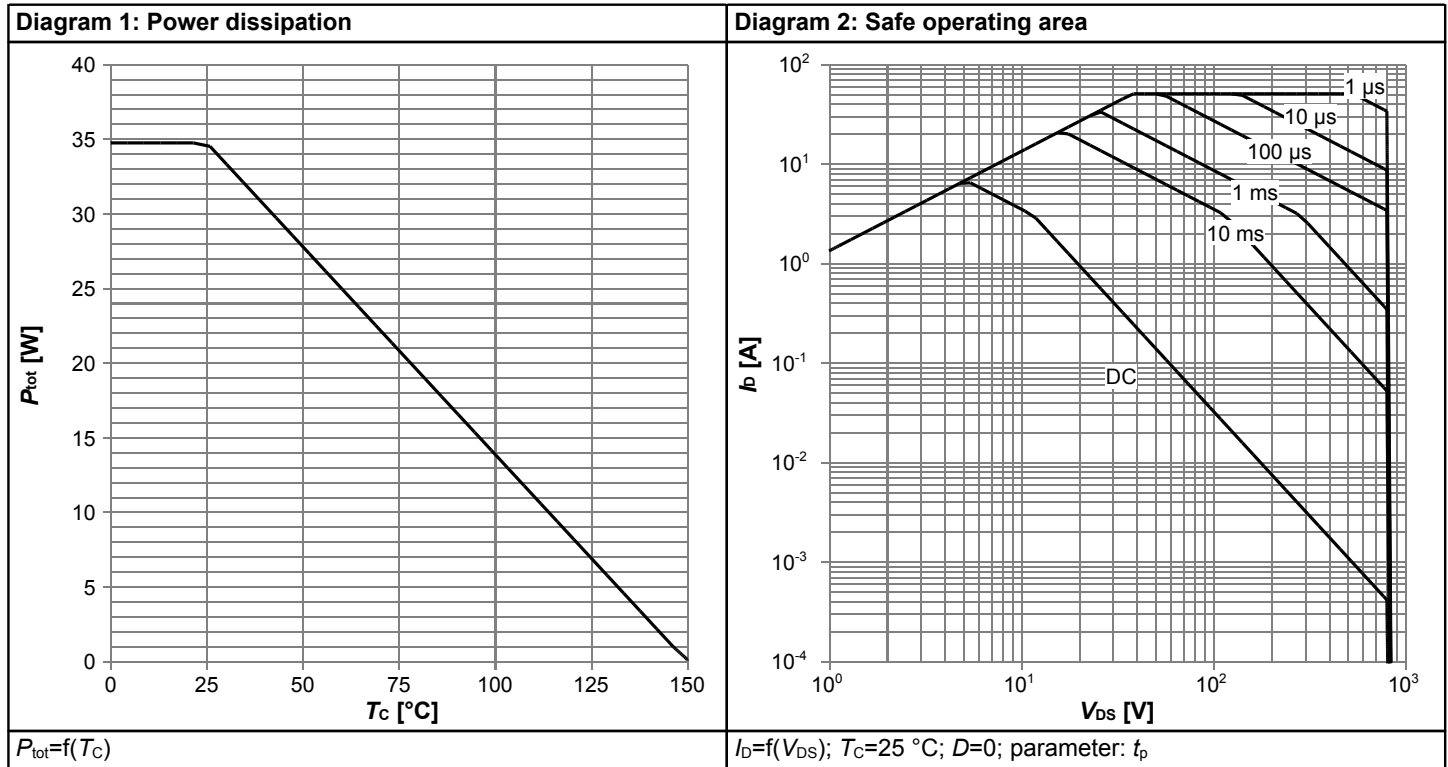
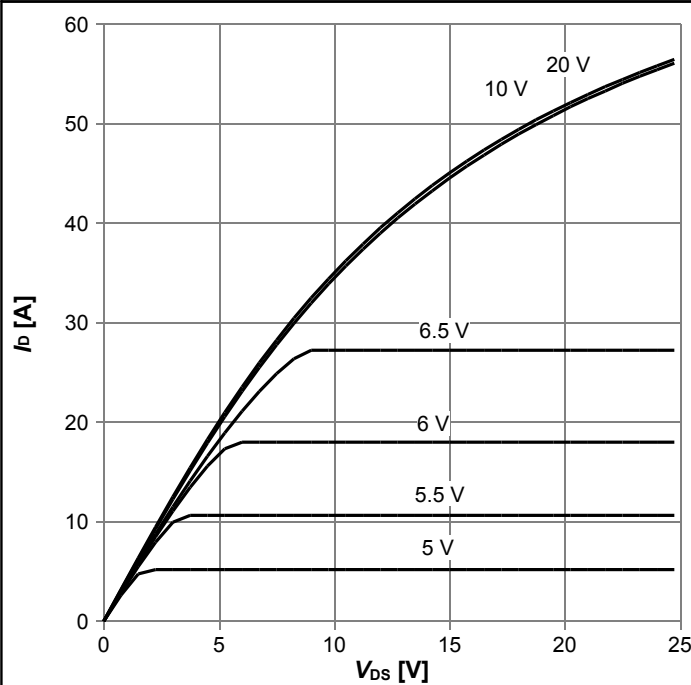


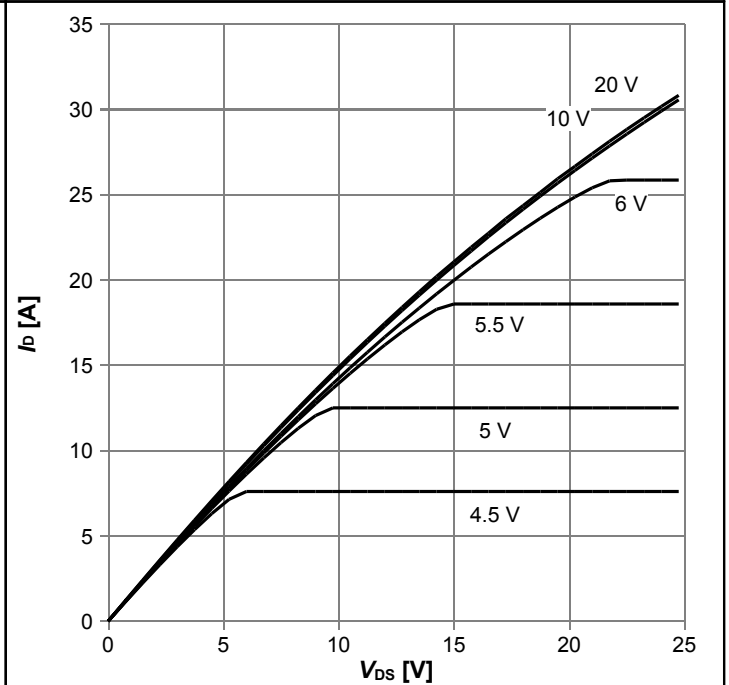


Diagram 5: Typ. output characteristics



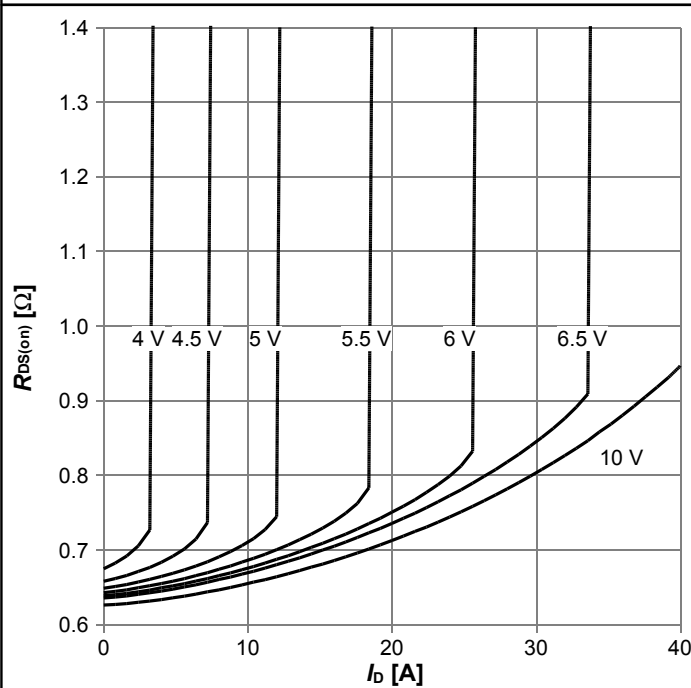
$I_D = f(V_{DS})$ ;  $T_j = 25^\circ\text{C}$ ;  $t_p = 10 \mu\text{s}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



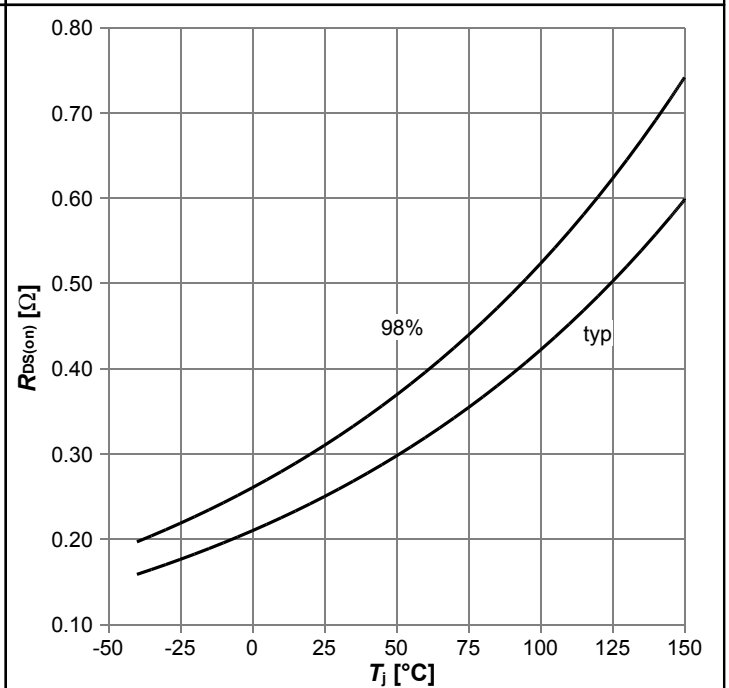
$I_D = f(V_{DS})$ ;  $T_j = 150^\circ\text{C}$ ;  $t_p = 10 \mu\text{s}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



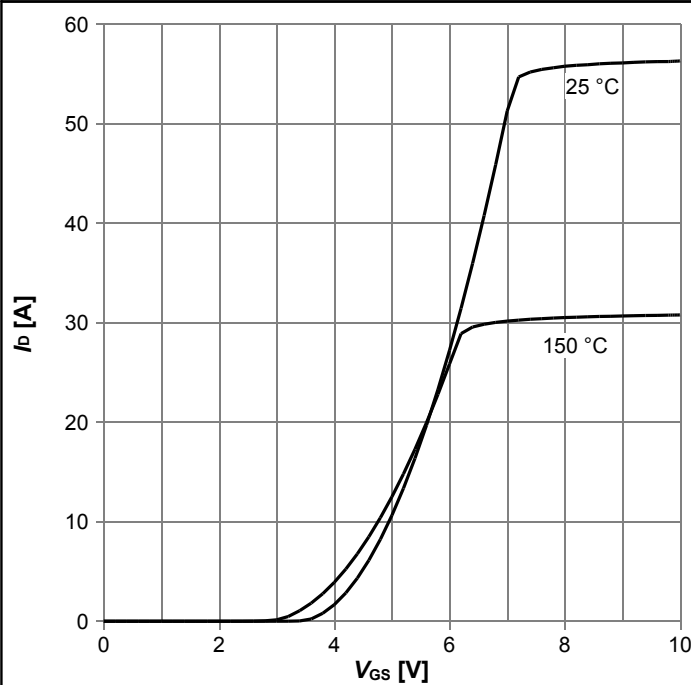
$R_{DS(on)} = f(I_D)$ ;  $T_j = 150^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



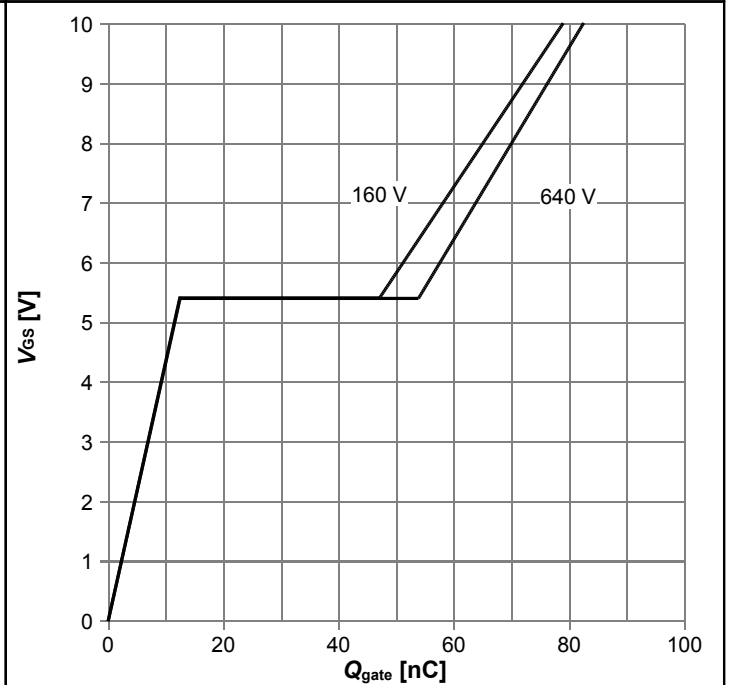
$R_{DS(on)} = f(T_j)$ ;  $I_D = 11.0 \text{ A}$ ;  $V_{GS} = 10 \text{ V}$

Diagram 9: Typ. transfer characteristics



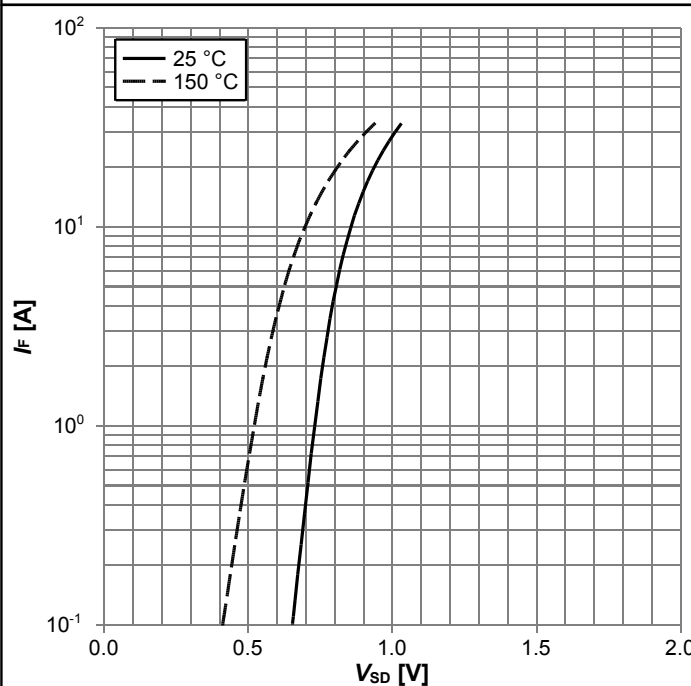
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; t_p = 10 \mu s; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



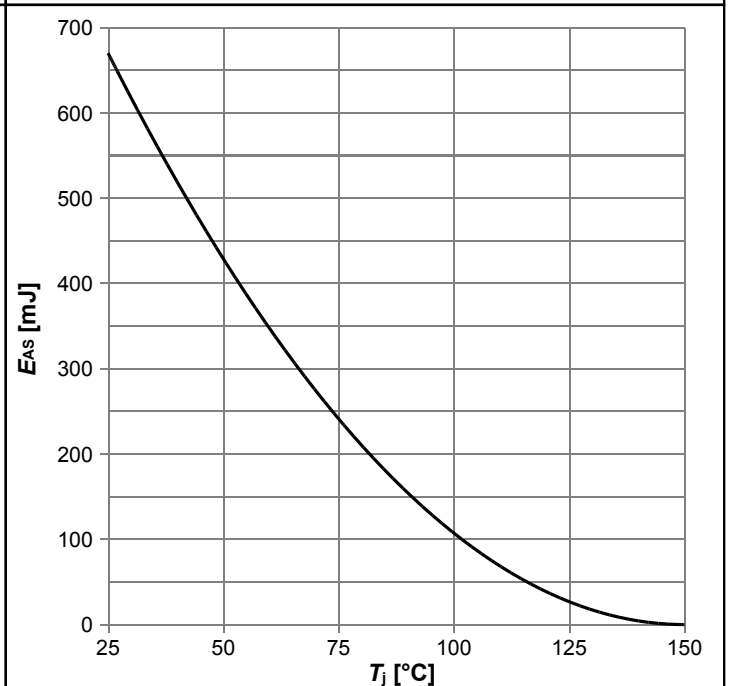
$V_{GS} = f(Q_{gate}); I_D = 17 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



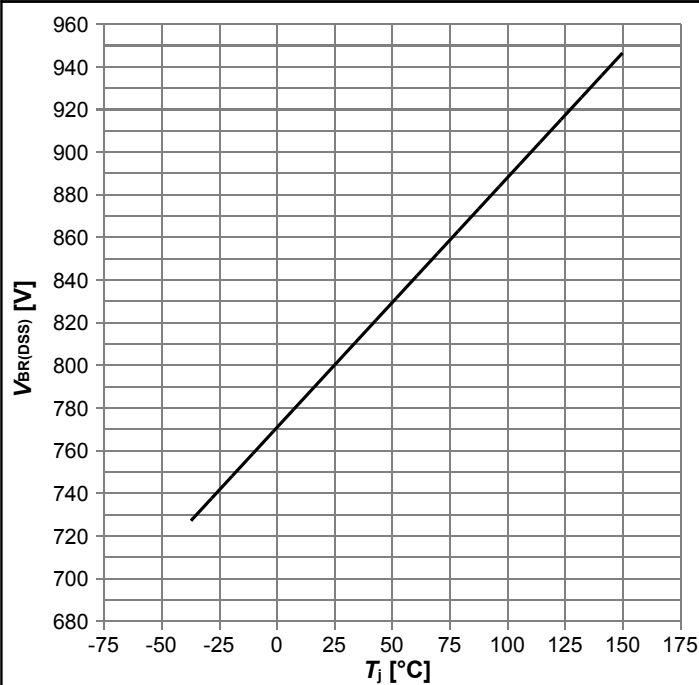
$I_F = f(V_{SD}); t_p = 10 \mu s; \text{parameter: } T_j$

Diagram 12: Avalanche energy



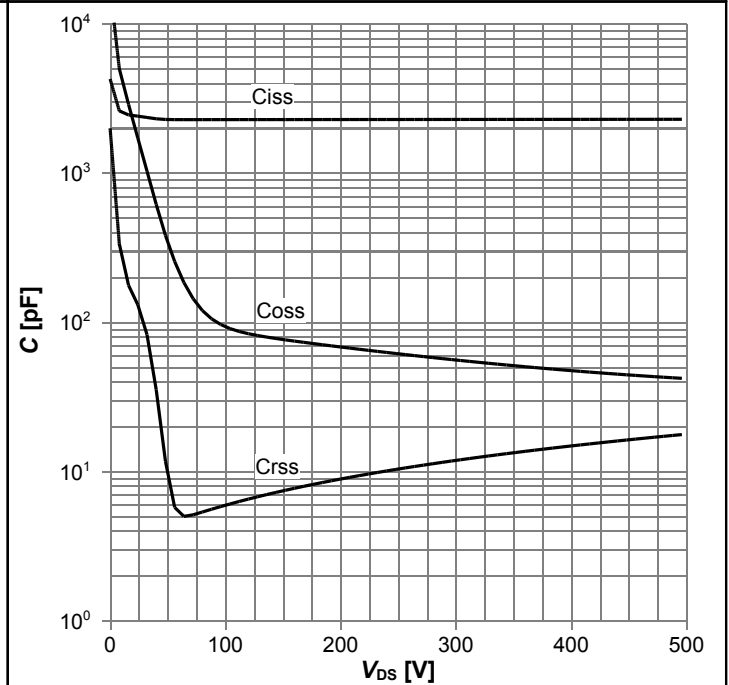
$E_{AS} = f(T_j); I_D = 3.4 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



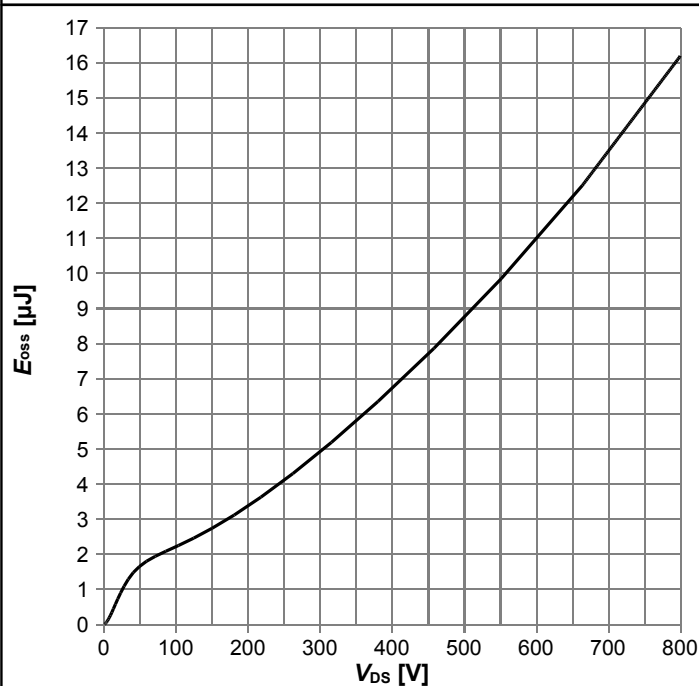
$V_{BR(DSS)}=f(T_j); I_D=0.25 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

## 6 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform

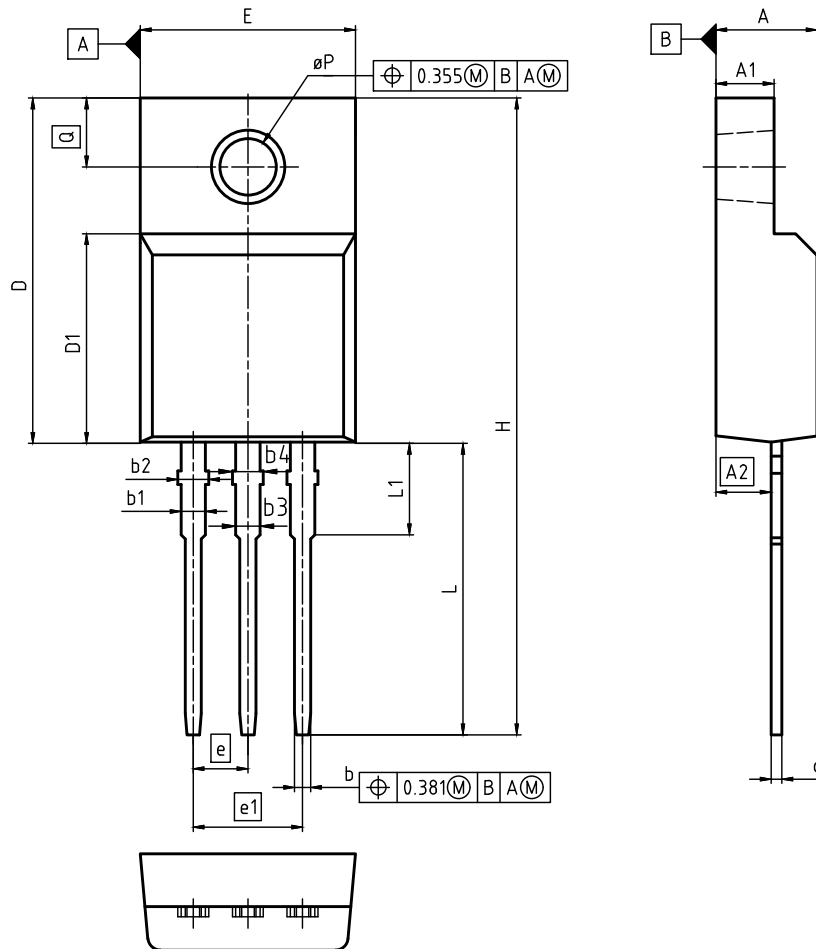
**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform

## 7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

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04

Dimensions do not include mold flash, protrusions or gate burrs

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

## 8 Appendix A

Table 11 Related Links

- IFX CoolMOS™ CE Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ CE application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ CE simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPA80R310CE

Revision: 2015-06-23, Rev. 2.1

### Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-09-25	Release of final version
2.1	2015-06-23	Continuous current Id update

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