International IOR Rectifier

IRFS4510PbF
IRFSL4510PbF

HEXFET® Power MOSFET

| V_{DSS}		100V
$R_{DS(on)}$	typ.	11.3mΩ
	max.	13.9mΩ
$I_{D \ (Silicon \ Limited)}$		61A

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free

D²Pak
IRFS4510PbF

TO-262
IRFSL4510PbF
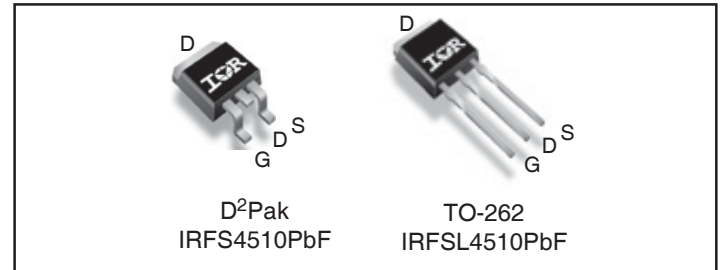
G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	61	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	43	
I_{DM}	Pulsed Drain Current ①	250	
P_D @T_C = 25°C	Maximum Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	3.2	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

$E_{AS \ (Thermally \ limited)}$	Single Pulse Avalanche Energy ②	130	mJ
I_{AR}	Avalanche Current	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ④		mJ

Thermal Resistance

Parameter		Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	——	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑦⑧	——	40	

www.irf.com

1

4/10/12

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.11	——	V/°C	Reference to 25°C, I_D = 5mA①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	11.3	13.9	mΩ	V_{GS} = 10V, I_D = 37A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 100µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 100V, V_{GS} = 0V
		——	——	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
R_G	Internal Gate Resistance	——	0.6	——	Ω	

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	100	——	——	S	V_{DS} = 25V, I_D = 37A
Q_g	Total Gate Charge	——	58	87	nC	I_D = 37A
Q_{gs}	Gate-to-Source Charge	——	14	——		V_{DS} =50V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	18			V_{GS} = 10V ④
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	——	40	——		I_D = 37A, V_{DS} =0V, V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	——	13	——	ns	V_{DD} = 65V
t_r	Rise Time	——	32	——		I_D = 37A
$t_{d(off)}$	Turn-Off Delay Time	——	28	——		R_G =2.7Ω
t_f	Fall Time	——	28	——		V_{GS} = 10V ④
C_{iss}	Input Capacitance	——	3180	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	220	——		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	——	120	——		f = 1.0MHz, See Fig.5
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related) ⑥	——	260	——		V_{GS} = 0V, V_{DS} = 0V to 80V ⑥, See Fig.11
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑤	——	325	——		V_{GS} = 0V, V_{DS} = 0V to 80V ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	61	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	250	A	
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 37A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	54	81	ns	T_J = 25°C $\quad V_R$ = 85V,
		——	60	90		T_J = 125°C $\quad I_F$ = 37A
Q_{rr}	Reverse Recovery Charge	——	95	140	nC	T_J = 25°C $\quad$ di/dt = 100A/µs ④
		——	130	195		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	3.3	——	A	T_J = 25°C
t_{on}	Forward Turn-On Time				Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.192mH
R_G = 25Ω, I_{AS} = 37A, V_{GS} =10V. Part not recommended for use above this value.

③ I_{SD} ≤ 37A, di/dt ≤ 1550A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ R_θ is measured at T_J approximately 90°C.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
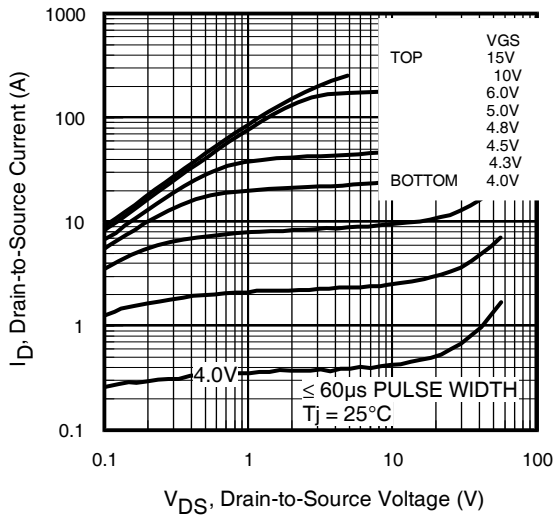
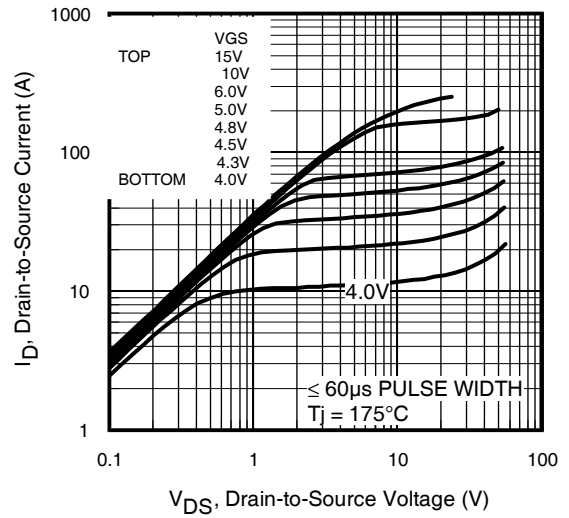**Fig 1.** Typical Output Characteristics
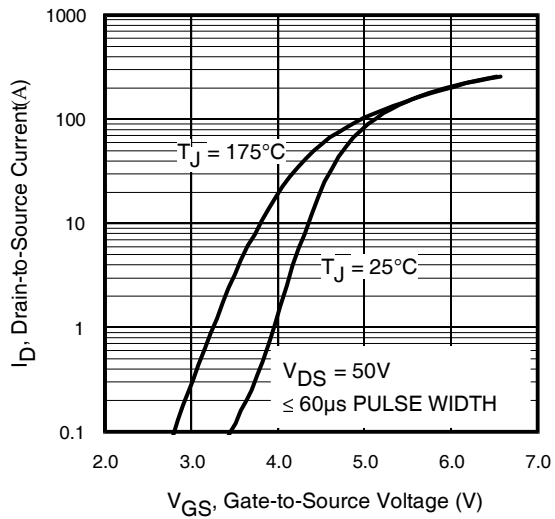

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics
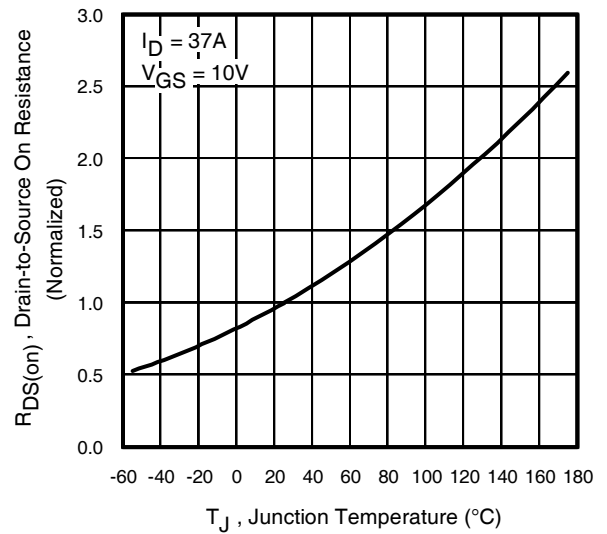

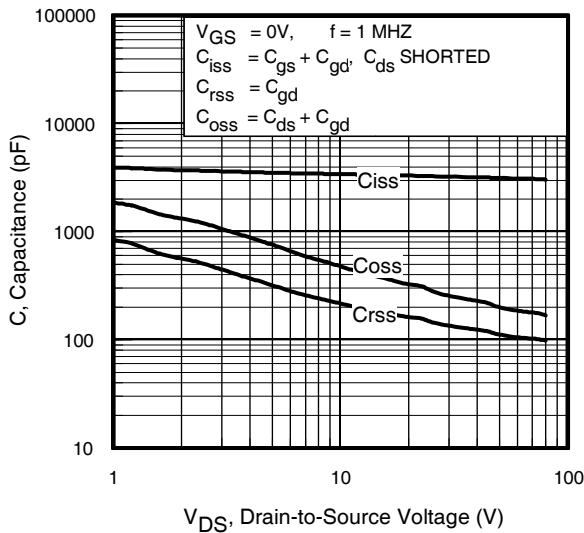**Fig 4.** Normalized On-Resistance vs. Temperature

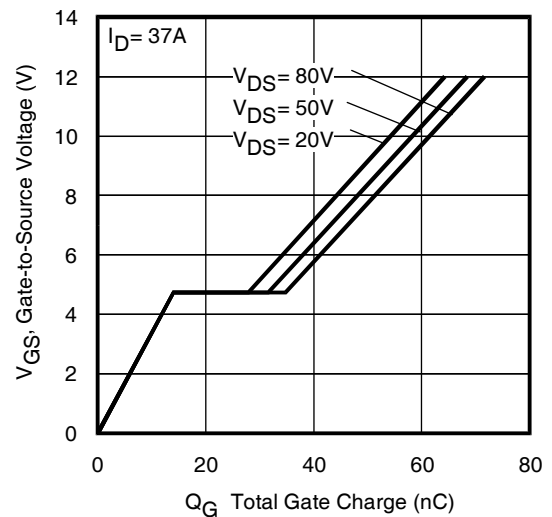**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

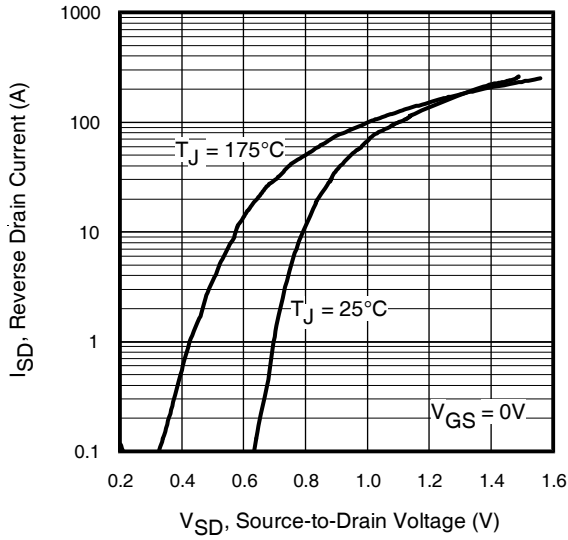**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage
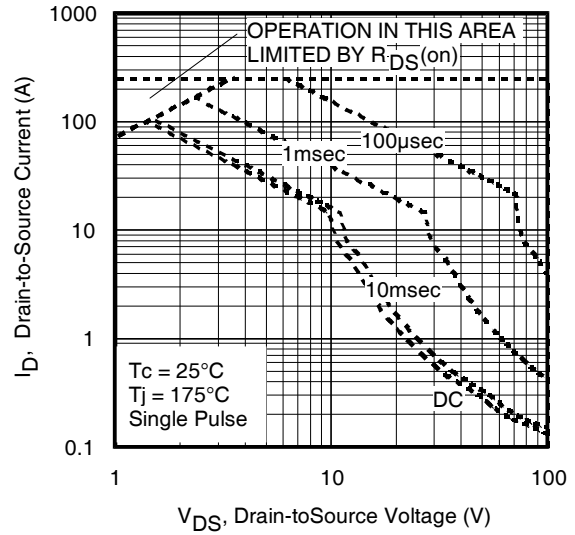
Fig 7. Typical Source-Drain Diode Forward Voltage
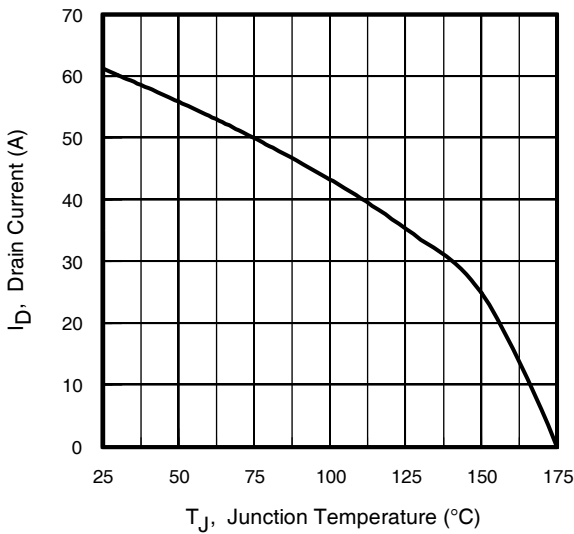

Fig 8. Maximum Safe Operating Area
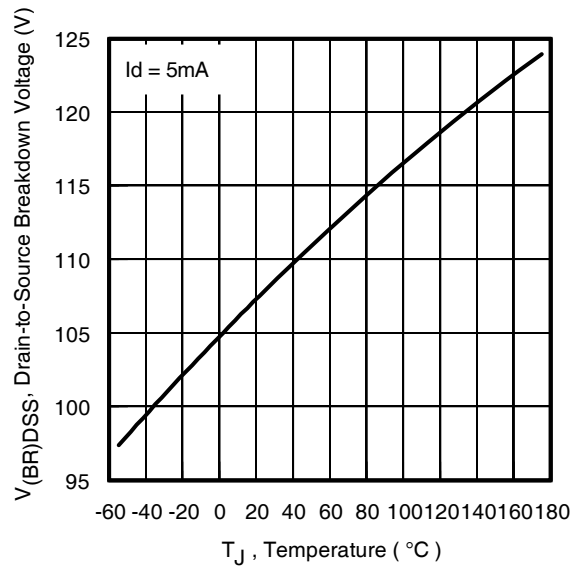

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage
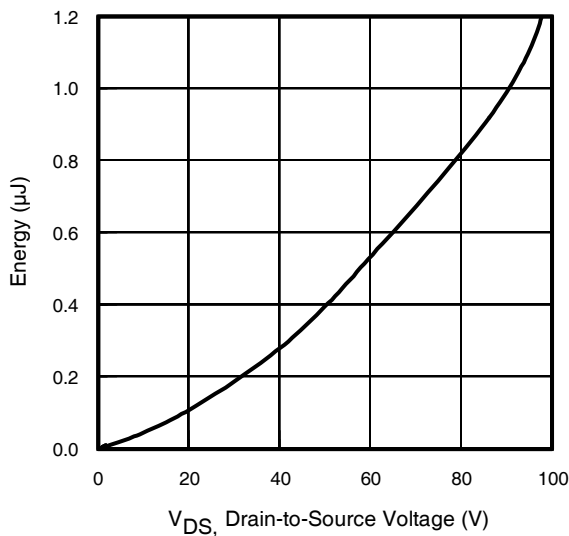
Fig 11. Typical C_{OSS} Stored Energy
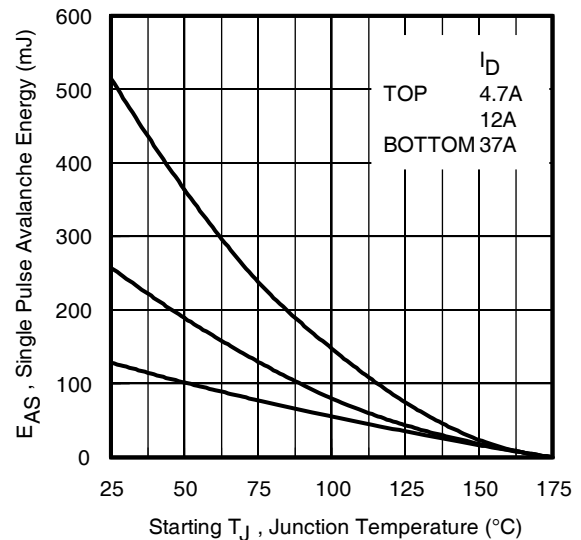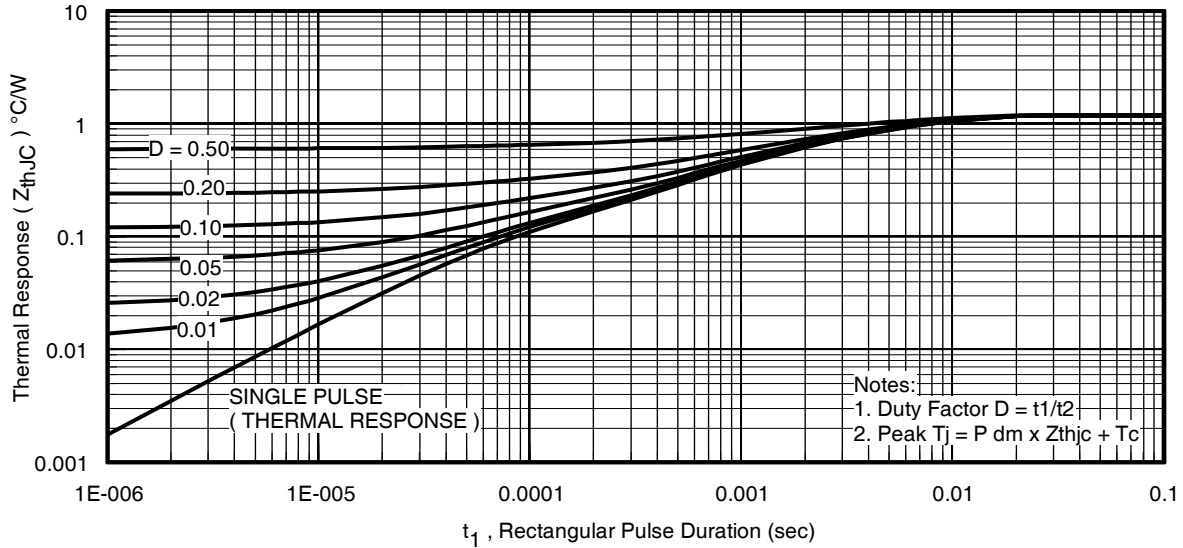

Fig 12. Maximum Avalanche Energy vs. DrainCurrent

4

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case
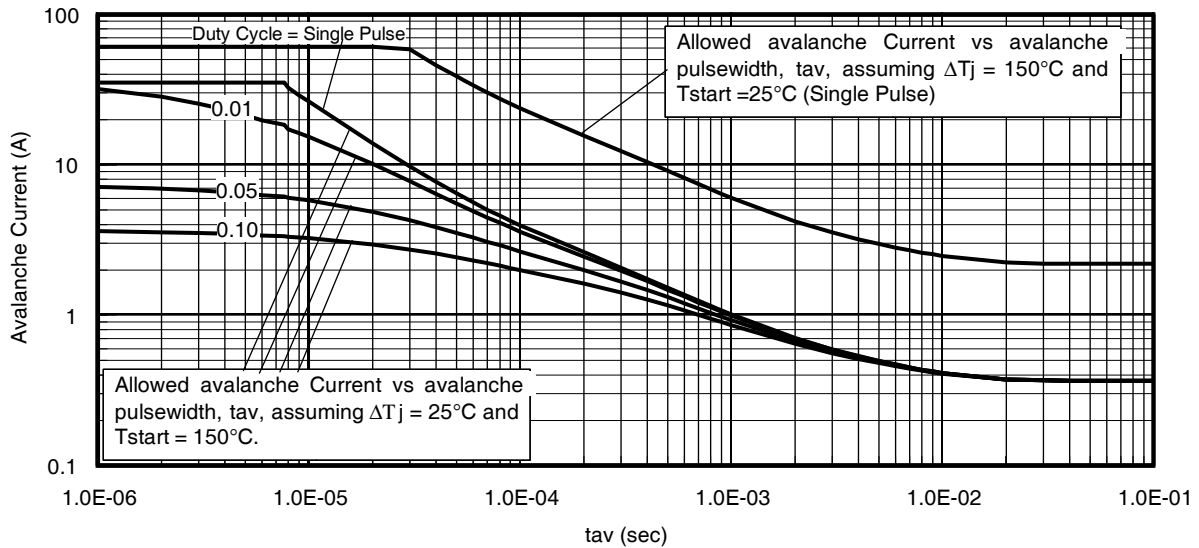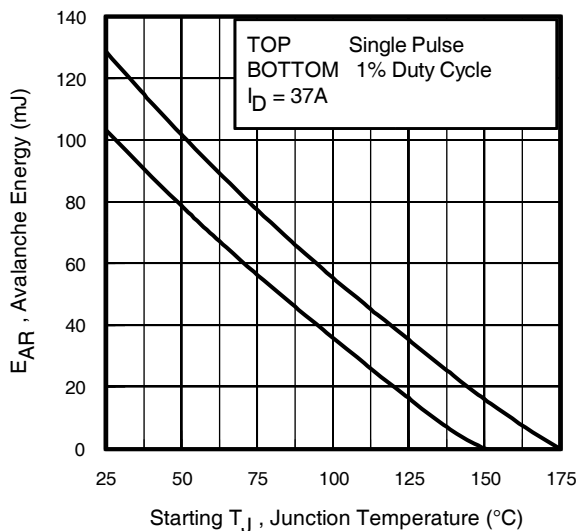
Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

Fig 14. Typical Avalanche Current vs.Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   Z_{thJC}(D, t_{av}) = Transient thermal resistance, see Figures 13)

$$P_{D (ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
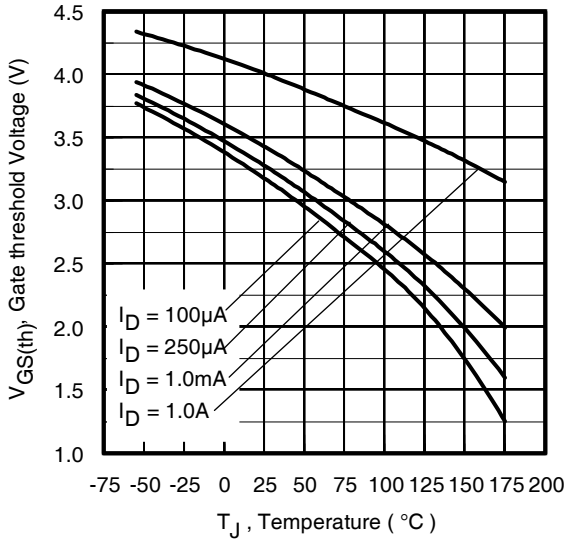$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$

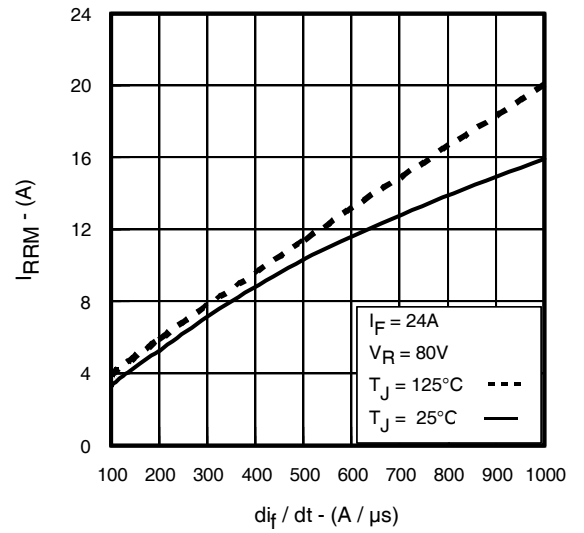**Fig 16.** Threshold Voltage vs. Temperature

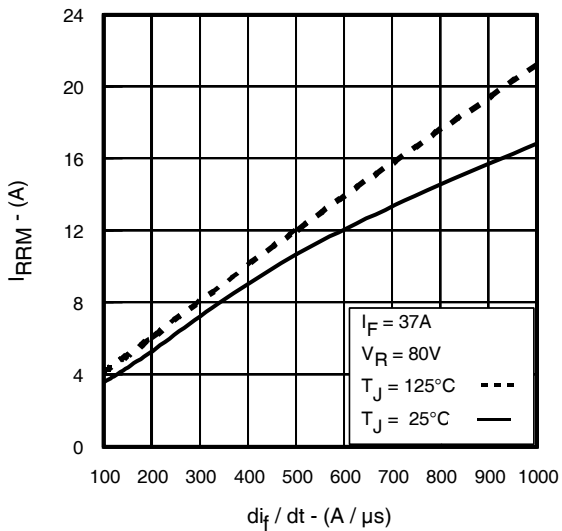**Fig. 17** - Typical Recovery Current vs. di$_f$/dt
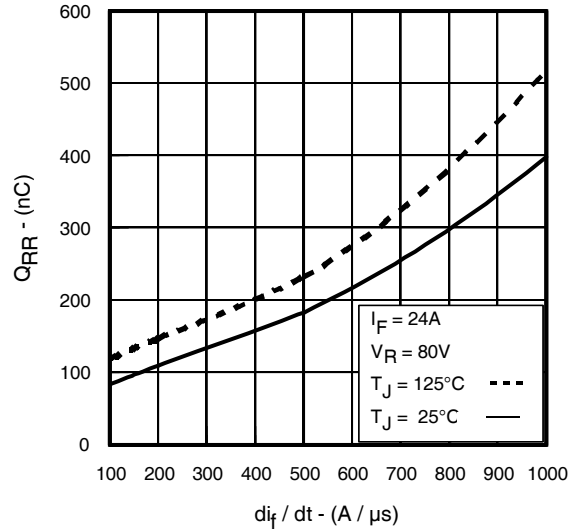

Fig. 18 - Typical Recovery Current vs. di$_f$/dt
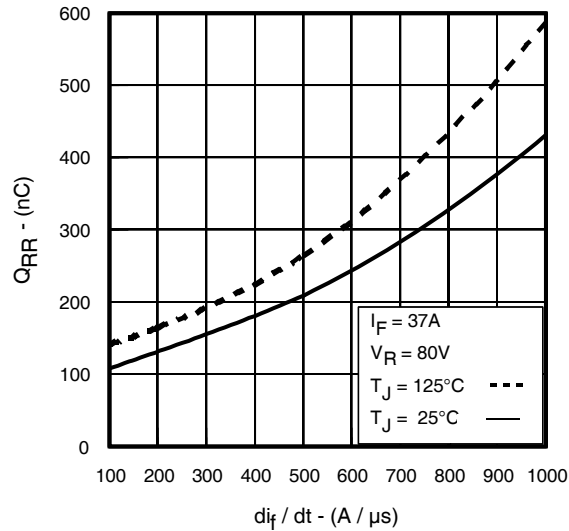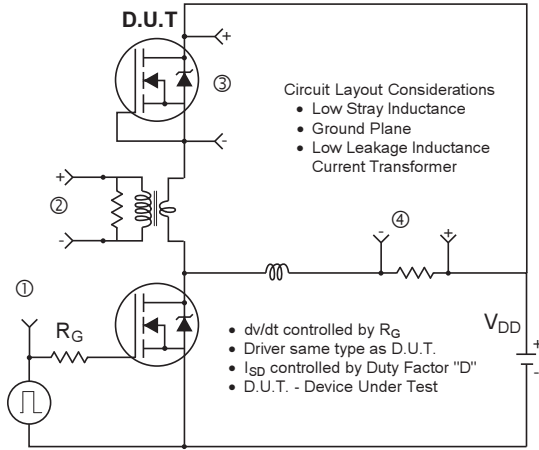

Fig. 19 - Typical Stored Charge vs. di$_f$/dt

Fig. 20 - Typical Stored Charge vs. di$_f$/dt

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs
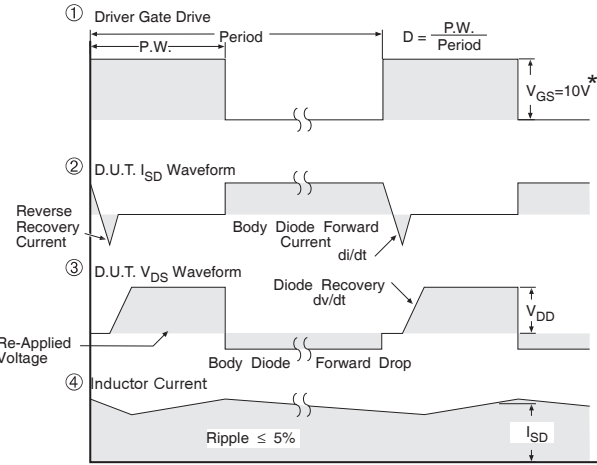
* V_{GS} = 5V for Logic Level Devices
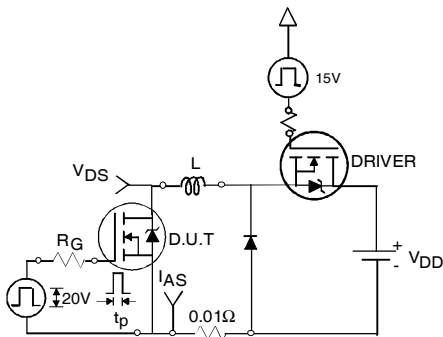

Fig 22a. Unclamped Inductive Test Circuit
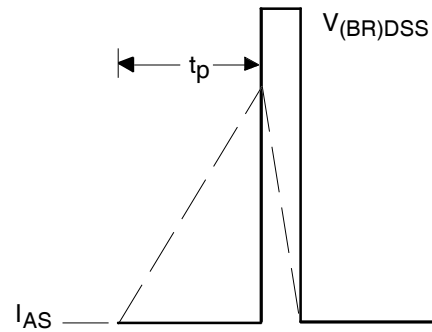

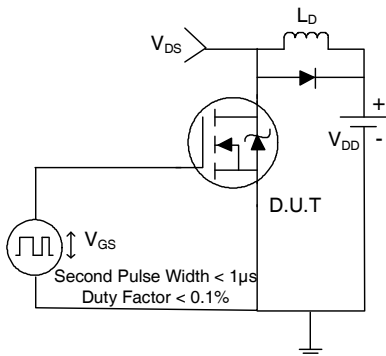**Fig 22b.** Unclamped Inductive Waveforms
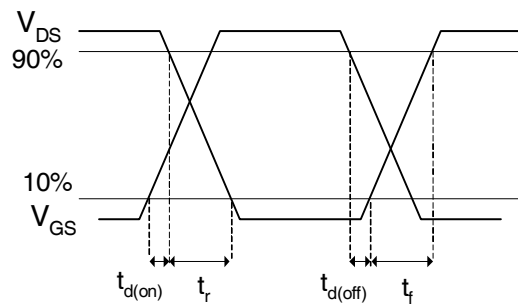

Fig 23a. Switching Time Test Circuit

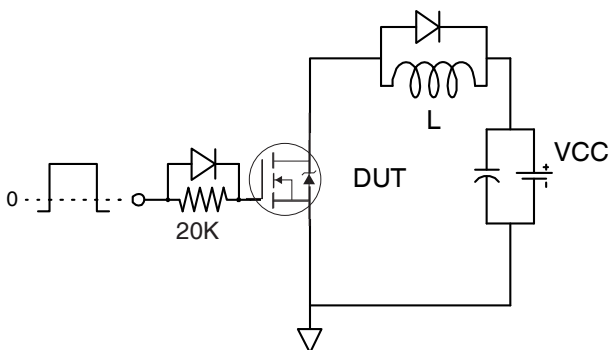
Fig 23b. Switching Time Waveforms

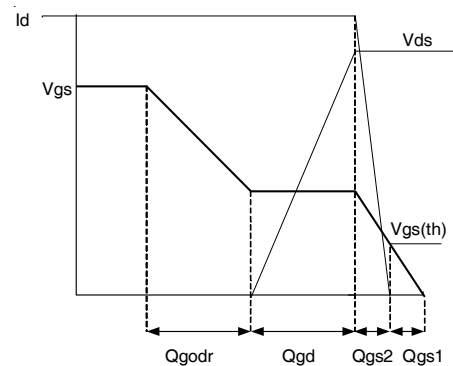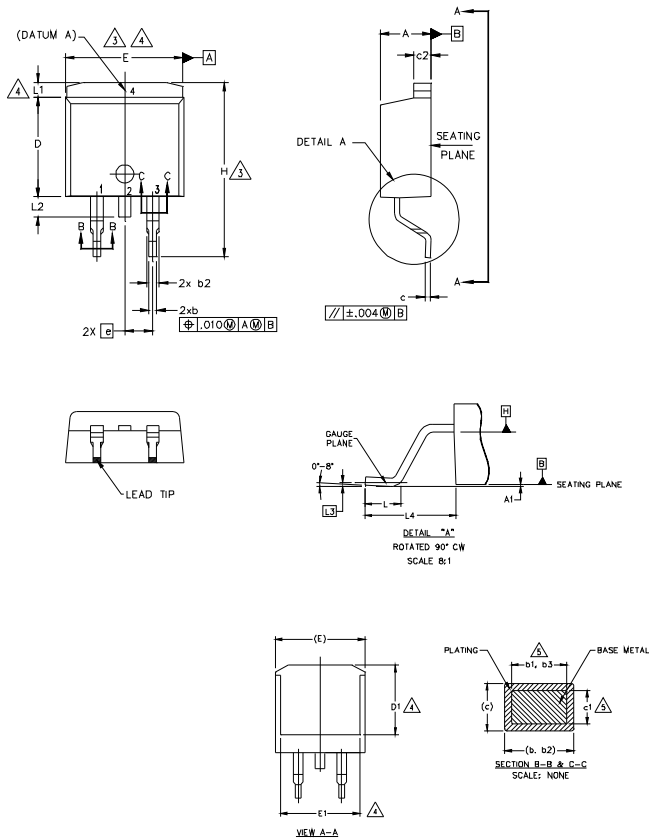**Fig 24a.** Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform

D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994

2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

△3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.

△4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.

△5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.

6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.

7. CONTROLLING DIMENSION: INCH.

8. OUTLINE CONFORMS TO JEDEC OUTLINE TO−263AB.

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.65	–	.066	4
L2	1.27	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

1.− GATE
2, 4.− DRAIN
3.− SOURCE

IGBTs, CoPACK

1.− GATE
2, 4.− COLLECTOR
3.− EMITTER

DIODES

1.− ANODE *
2, 4.− CATHODE
3.− ANODE

* PART DEPENDENT.

D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024 ASSEMBLED ON WW 02, 2000 IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead − Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L

OR

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
P = DESIGNATES LEAD - FREE PRODUCT (OPTIONAL)
YEAR 0 = 2000
WEEK 02
A = ASSEMBLY SITE CODE

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

www.irf.com

International IƏR Rectifier
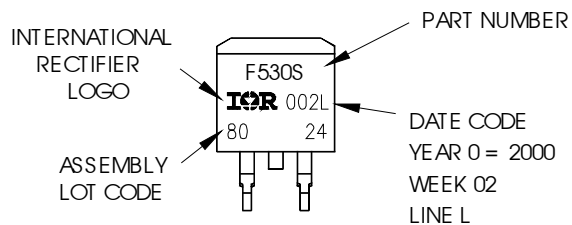
TO-262 Package Outline
Dimensions are shown in millimeters (inches)
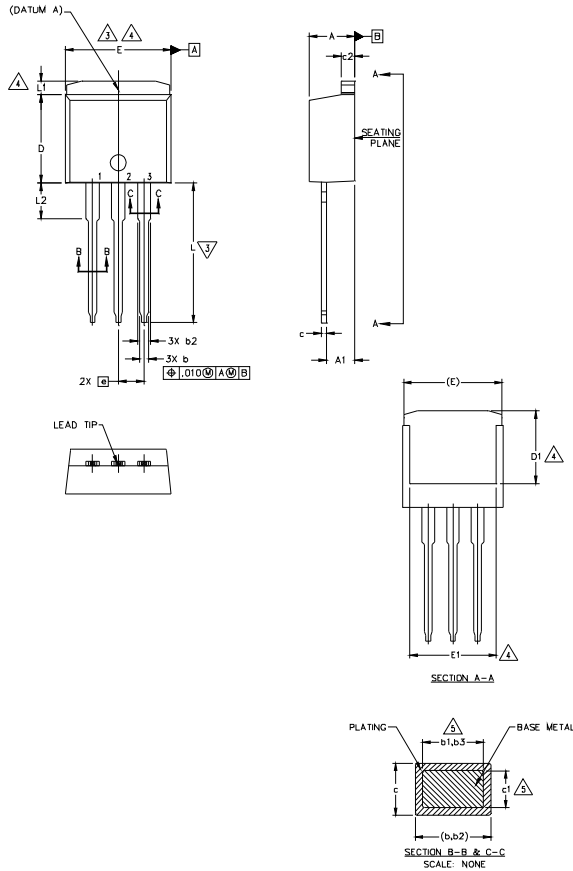
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	–	1.65	–	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBTs, CoPACK
1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

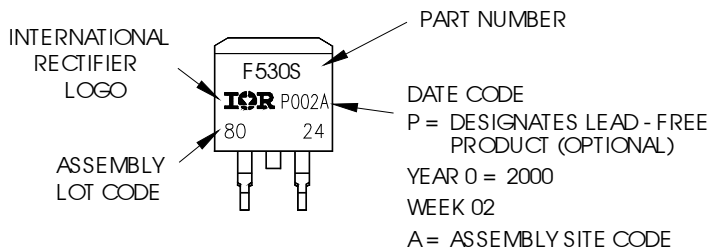## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

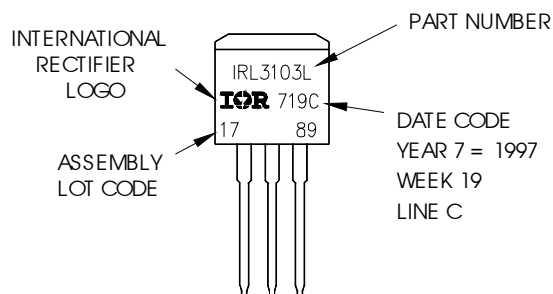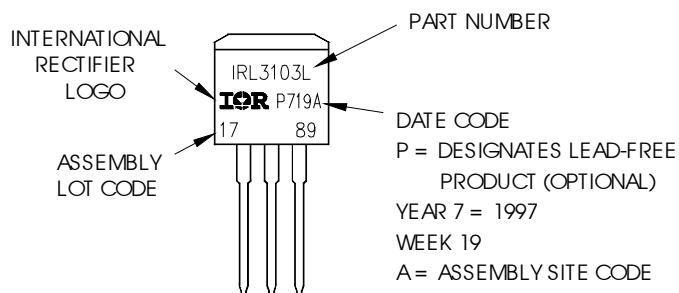Note: "P" in assembly line position indicates "Lead – Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

OR

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
P = DESIGNATES LEAD-FREE
       PRODUCT (OPTIONAL)
YEAR 7 = 1997
WEEK 19
A = ASSEMBLY SITE CODE

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)

TRR

FEED DIRECTION

TRL

FEED DIRECTION

1.60 (.063)
1.50 (.059)

⌀ 1.60 (.063)
1.50 (.059)

4.10 (.161)
3.90 (.153)

0.368 (.0145)
0.342 (.0135)

1.85 (.073)
1.65 (.065)

11.60 (.457)
11.40 (.449)

24.30 (.957)
23.90 (.941)

15.42 (.609)
15.22 (.601)

10.90 (.429)
10.70 (.421)

⌀ 1.75 (.069)
1.25 (.049)

4.72 (.136)
4.52 (.178)

16.10 (.634)
15.90 (.626)

13.50 (.532)
⌀ 12.80 (.504)

27.40 (1.079)
23.90 (.941)

④

⌀ 330.00
(14.173)
MAX.

⌀ 60.00 (2.362)
MIN.

30.40 (1.197)
MAX.

④

26.40 (1.039)
24.40 (.961)

③
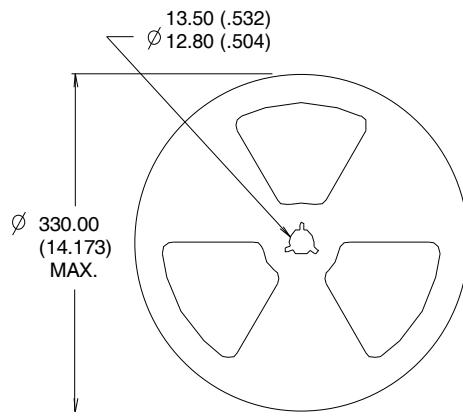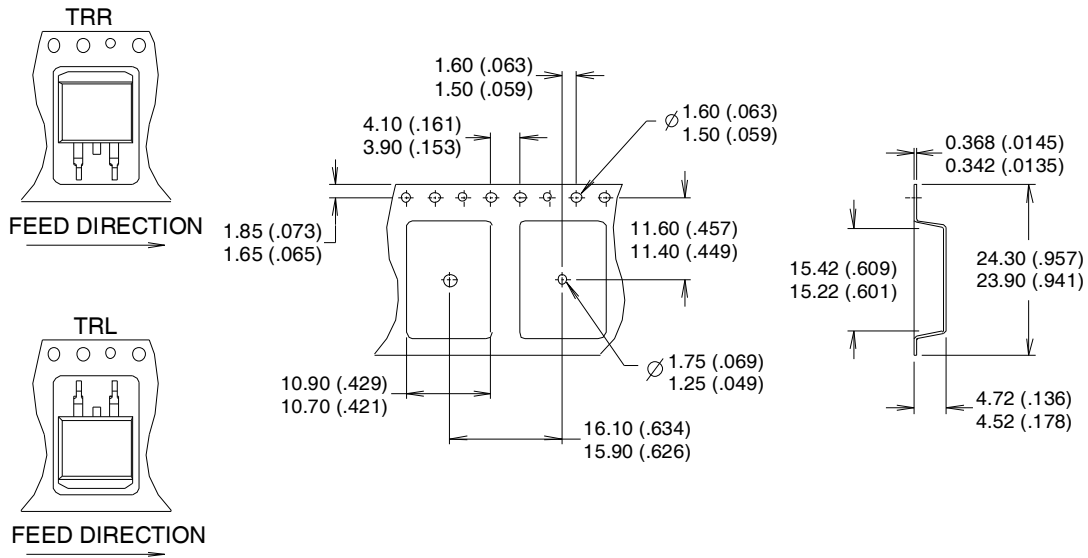
NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
③ DIMENSION MEASURED @ HUB.
④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.
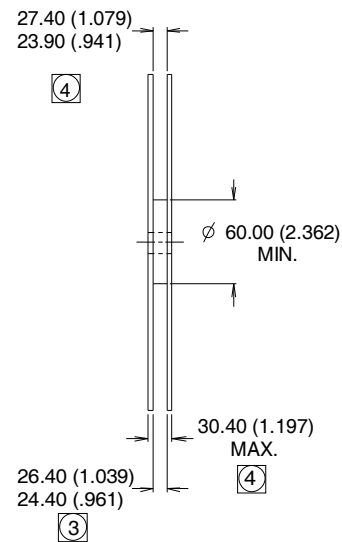
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie") .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.