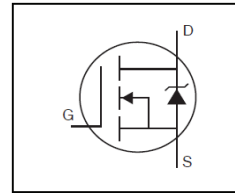


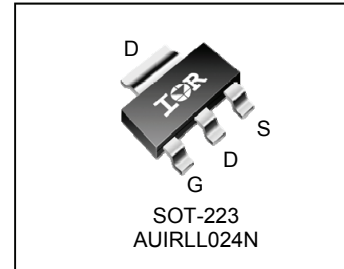
Features

- Advanced Planar Technology
- Low On-Resistance
- Logic Level Gate Drive
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *

HEXFET® Power MOSFET



V_{DSS}	55V
$R_{DS(on)}$ max.	0.065Ω
I_D	3.1A



G	D	S
Gate	Drain	Source

Description

Specifically designed for Automotive applications, this Cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRLL024N	SOT-223	Tape and Reel	2500	AUIRLL024NTR

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑥	4.4	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	3.1	
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	2.5	
I_{DM}	Pulsed Drain Current ①	12	
$P_D @ T_A = 25^\circ C$	Maximum Power Dissipation (PCB Mount) ⑥	2.1	W
$P_D @ T_A = 25^\circ C$	Maximum Power Dissipation (PCB Mount) ⑤	1.0	
	Linear Derating Factor (PCB Mount) ⑤	8.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	120	mJ
I_{AR}	Avalanche Current ①	3.1	A
E_{AR}	Repetitive Avalanche Energy ①⑤	0.1	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑤	90	120	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑥	50	60	

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*Qualification standards can be found at www.infineon.com

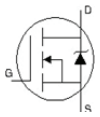
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	55	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.048	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.065	Ω	V _{GS} = 10V, I _D = 3.1A ④
		—	—	0.080		V _{GS} = 5.0V, I _D = 2.5A ④
		—	—	0.100		V _{GS} = 4.0V, I _D = 1.6A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Trans conductance	3.3	—	—	S	V _{DS} = 25V, I _D = 1.9A
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 55V, V _{GS} = 0V
		—	—	250		V _{DS} = 44V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -16V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

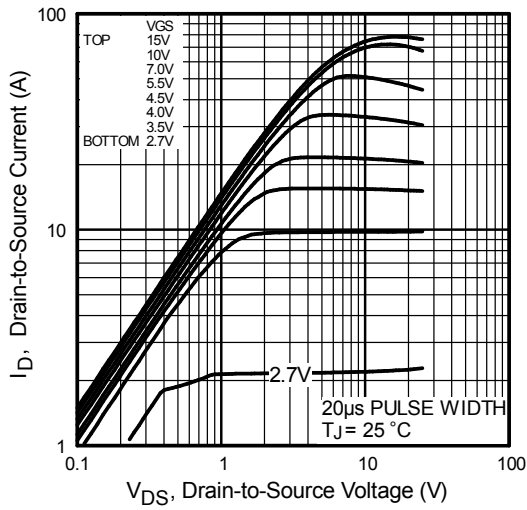
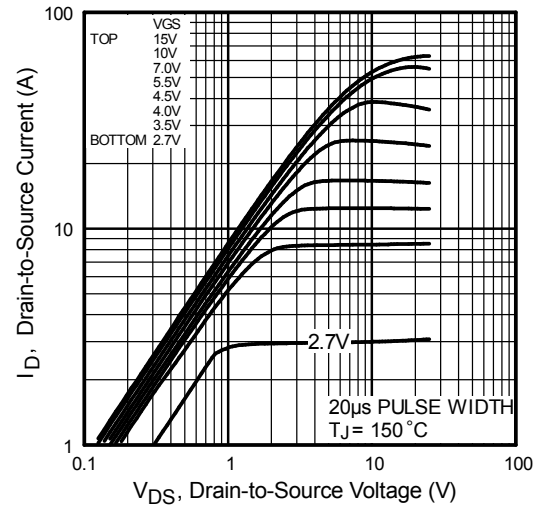
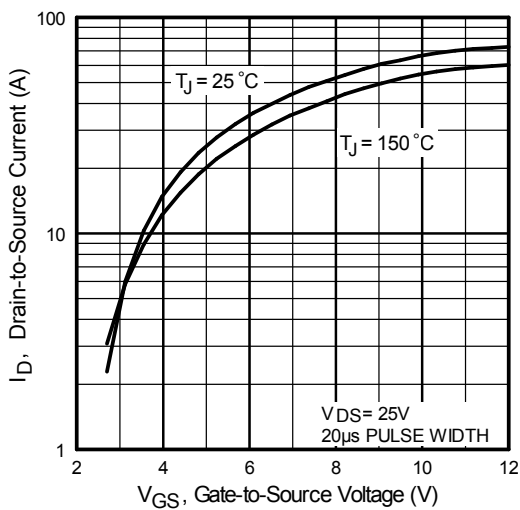
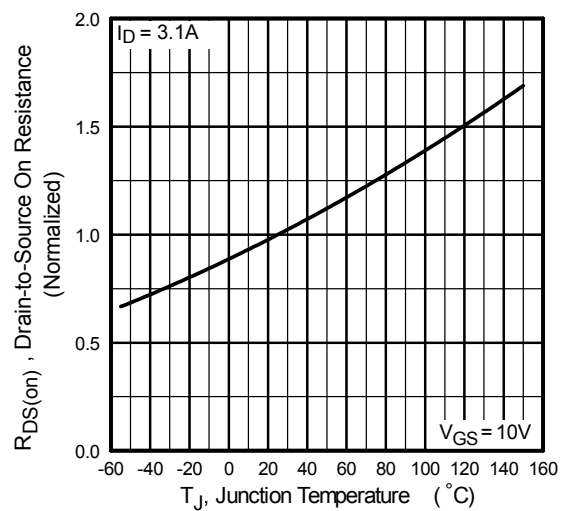
Q _g	Total Gate Charge	—	10.4	15.6	nC	I _D = 1.9A
Q _{gs}	Gate-to-Source Charge	—	1.5	2.3		V _{DS} = 44V
Q _{gd}	Gate-to-Drain Charge	—	5.5	8.3		V _{GS} = 5.0V, See Fig 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	7.4	—	ns	V _{DD} = 28V
t _r	Rise Time	—	21	—		I _D = 1.9A
t _{d(off)}	Turn-Off Delay Time	—	18	—		R _G = 24Ω
t _f	Fall Time	—	25	—		R _D = 15Ω, See Fig. 10 ④
C _{iss}	Input Capacitance	—	510	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	140	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	58	—		f = 1.0MHz, See Fig.5

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	12		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 1.9A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	39	58	ns	T _J = 25°C, I _F = 1.9A,
Q _{rr}	Reverse Recovery Charge	—	63	94	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 25mH, R_G = 25Ω, I_{AS} = 3.1A. (See fig. 12)
- ③ I_{SD} ≤ 1.9A, di/dt ≤ 270A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ When mounted on FR-4 board using minimum recommended footprint.
- ⑥ When mounted on 1 inch square copper board, for comparison with other SMD devices.


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

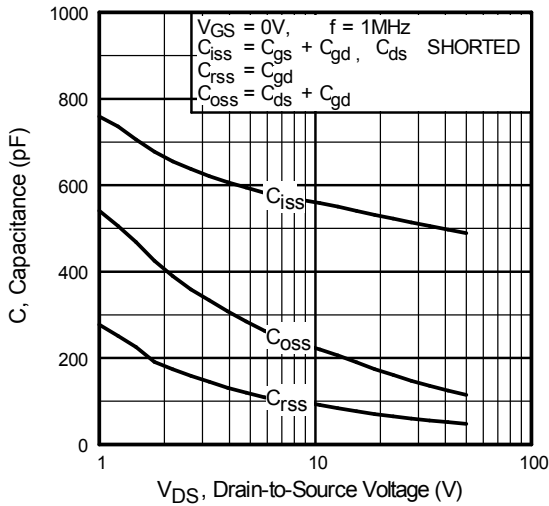


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

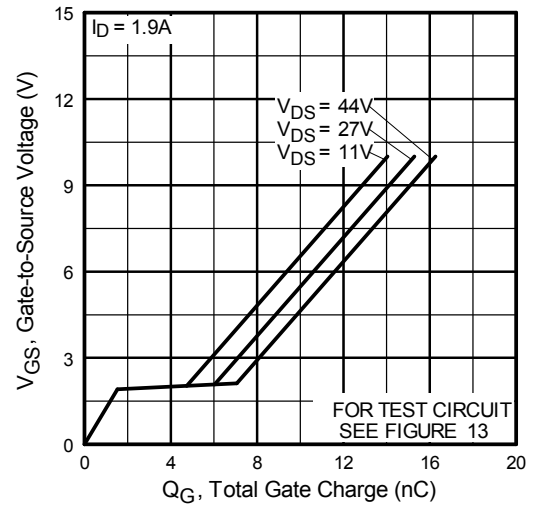


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

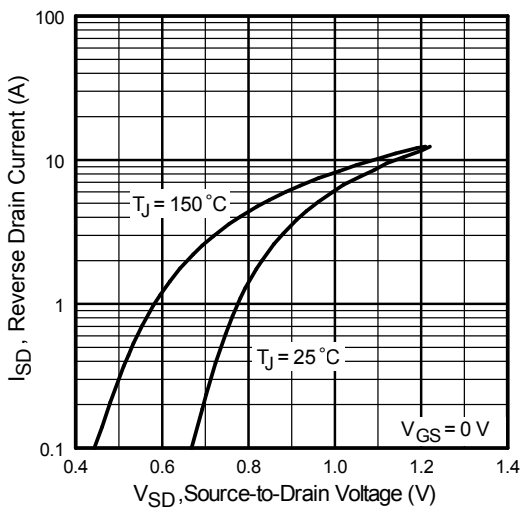


Fig 7 Typical Source-to-Drain Diode Forward Voltage

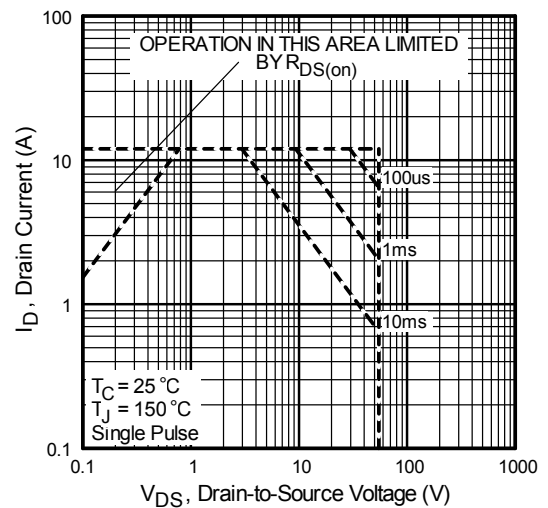


Fig 8. Maximum Safe Operating Area

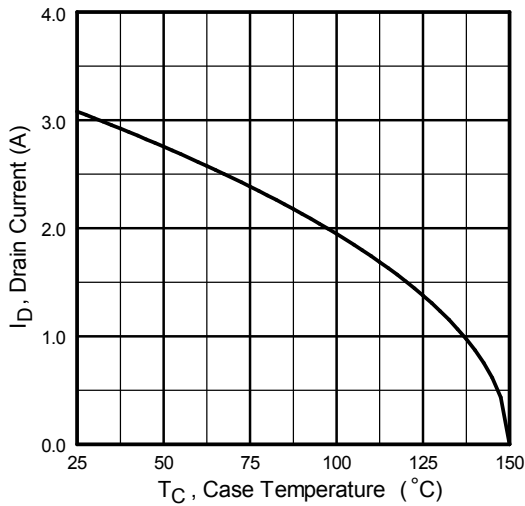


Fig 9. Maximum Drain Current Vs. Case Temperature

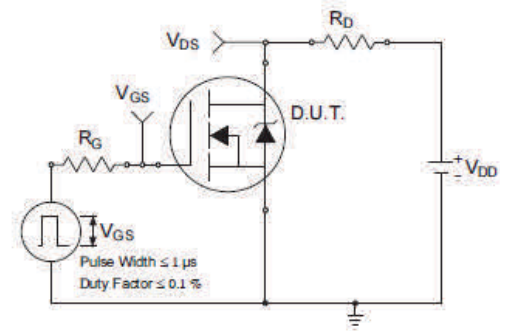


Fig 10a. Switching Time Test Circuit

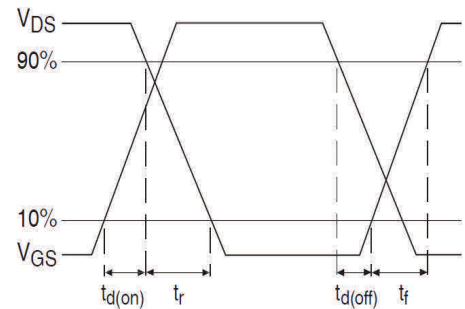


Fig 10b. Switching Time Waveforms

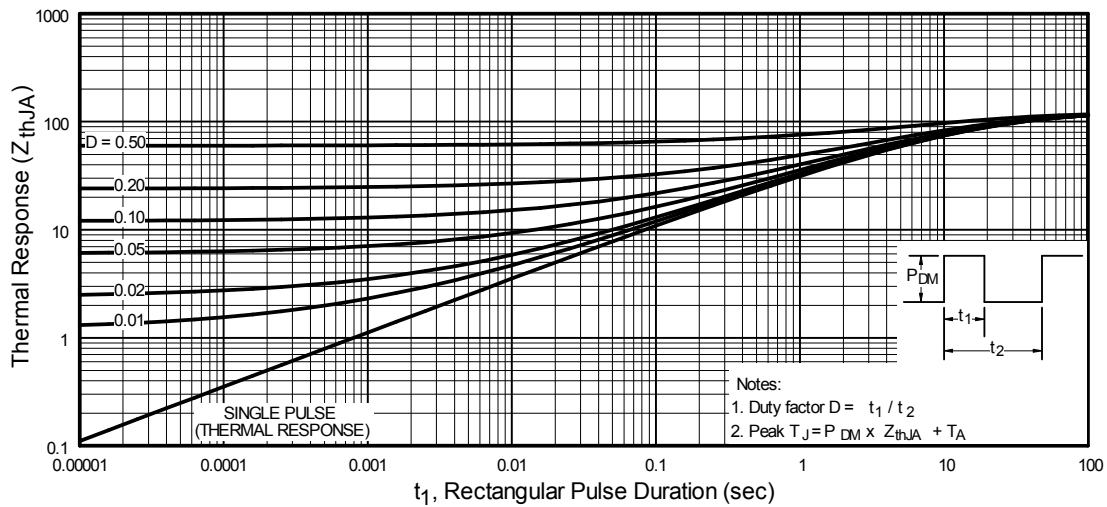
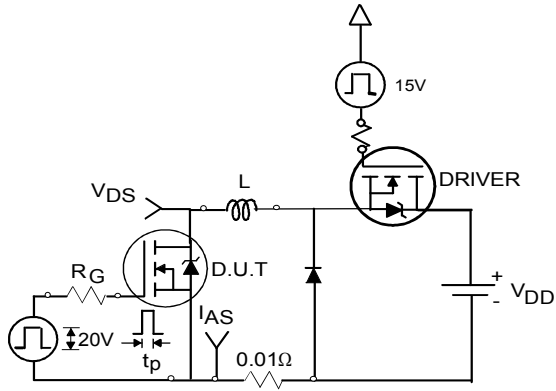
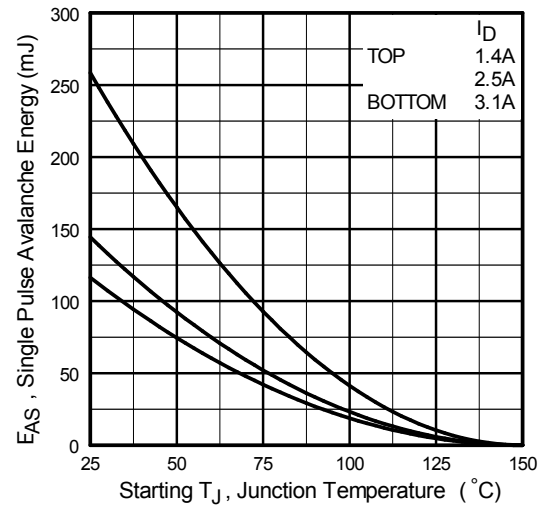
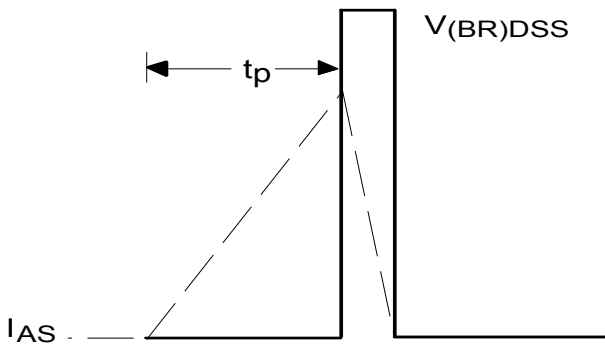
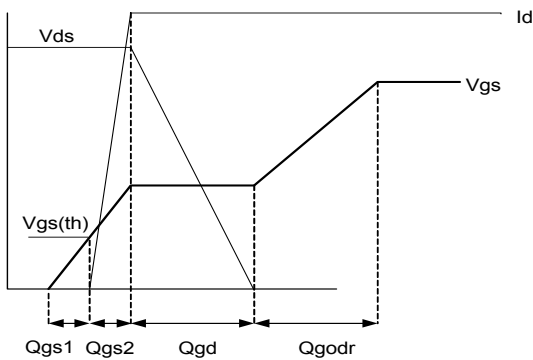
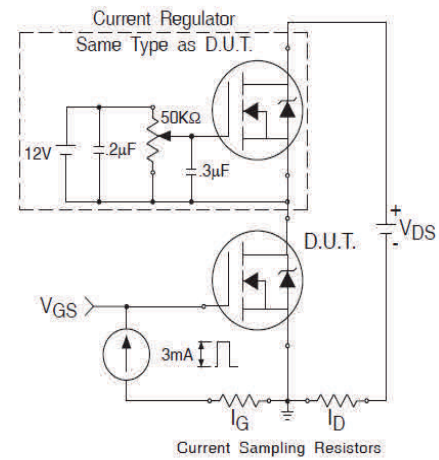
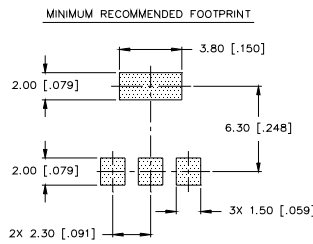
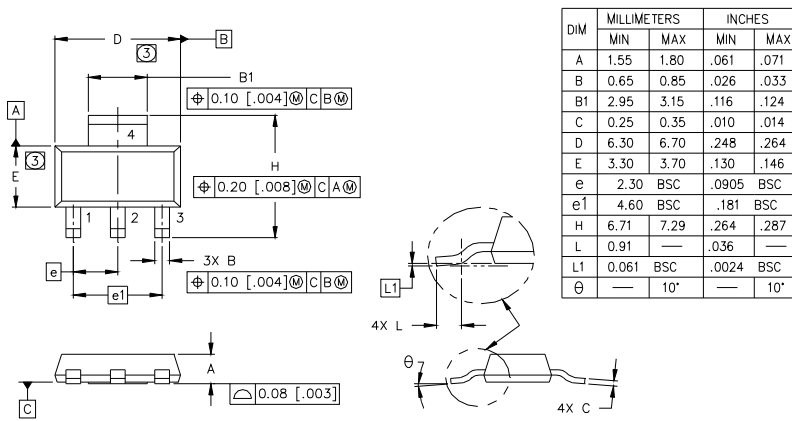


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient


Fig 12a. Unclamped Inductive Test Circuit

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

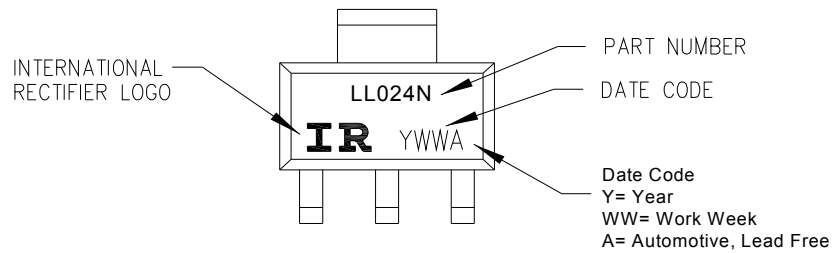
SOT-223 (TO-261AA) Package Outline (Dimensions are shown in millimeters (inches))



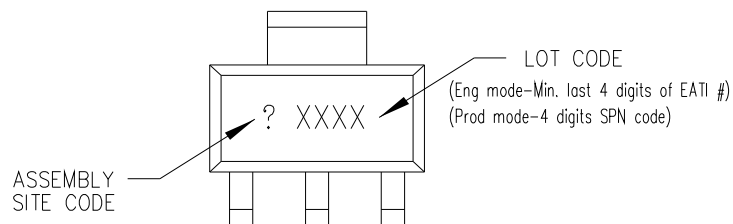
- LEAD ASSIGNMENTS**
- 1 = GATE
 - 2 = DRAIN
 - 3 = SOURCE
 - 4 = DRAIN

- NOTES:**
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSIONS DO NOT INCLUDE MOLD FLASH.
 4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-261AA.
 5. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

SOT-223(TO-261AA) Part Marking Information

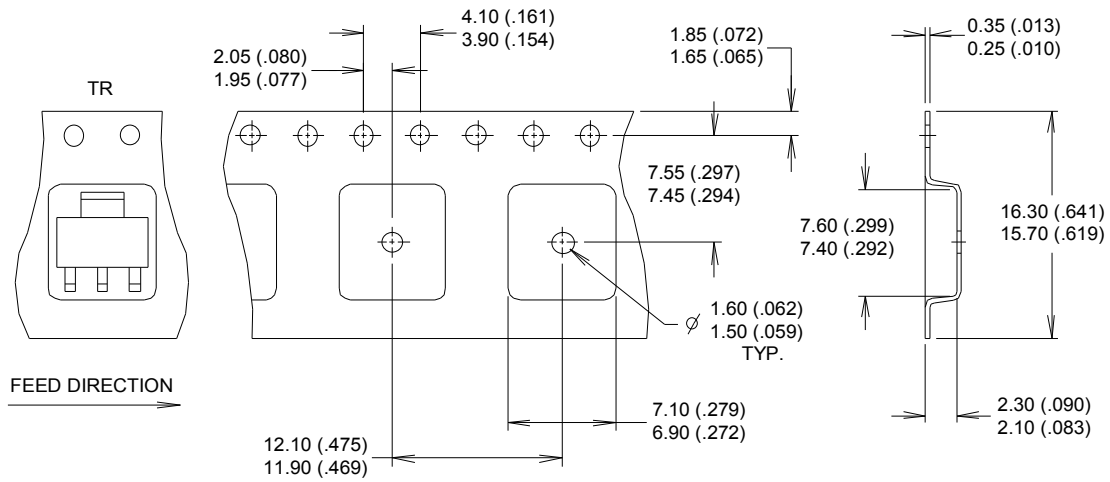


TOP MARKING

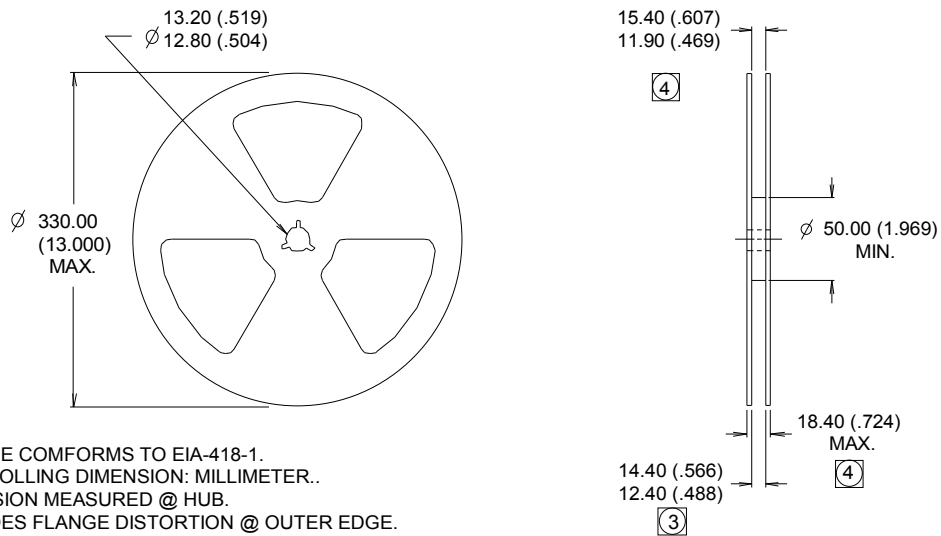


BOTTOM MARKING

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

SOT-223(TO-261AA) Tape and Reel (Dimensions are shown in millimeters (inches))


- NOTES :
1. CONTROLLING DIMENSION: MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.
 3. EACH $\varnothing 330.00$ (13.00) REEL CONTAINS 2,500 DEVICES.



- NOTES :
1. OUTLINE COMFORMS TO EIA-418-1.
 2. CONTROLLING DIMENSION: MILLIMETER..
 - ③ DIMENSION MEASURED @ HUB.
 - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOT-223	MSL1
ESD	Machine Model	Class M2 (+/- 150V) [†] AEC-Q101-002	
	Human Body Model	Class H1A (+/- 500V) [†] AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
3/25/2014	<ul style="list-style-type: none"> Added "Logic Level Gate Drive" bullet in the features section on page 1 Updated part marking on page 7 Updated data sheet with new IR corporate template
10/29/2015	<ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1.

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