PD-94764O

IRHLUB7970Z4
JANSR2N7626UB

An Infineon Technologies Company

RADIATION HARDENED LOGIC LEVEL POWER MOSFET SURFACE MOUNT (UB)

60V, P-CHANNEL
REF: MIL-PRF-19500/745
R7 TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHLUB7970Z4	100 kRads(Si)	1.4Ω	-0.53A	JANSR2N7626UB
IRHLUB7930Z4	300 kRads(Si)	1.4Ω	-0.53A	JANSF2N7626UB

Refer to Page 10 for 3 Additional Part Numbers - IRHLUBN7970Z4, IRHLUBC7970Z4, IRHLUBCN7970Z4

UB
(SHIELDED METAL LID)

Description

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Surface Mount
- Light Weight
- Complementary N-Channel Available- IRHLUB770Z4, IRHLUBN770Z4 IRHLUBC770Z4, IRHLUBCN770Z4

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = -4.5V, T_C = 25°C	Continuous Drain Current	-0.53	A
I_{D2} @ V_{GS} = -4.5V, T_C = 100°C	Continuous Drain Current	-0.33	
I_{DM} @T_C = 25°C	Pulsed Drain Current ①	-2.12	
P_D @T_C = 25°C	Maximum Power Dissipation	0.57	W
	Linear Derating Factor	0.0045	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy ②	33.5	mJ
I_{AR}	Avalanche Current ①	-0.53	A
E_{AR}	Repetitive Avalanche Energy ①	0.06	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-4.4	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	43 (Typical)	mg

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.055	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.40	Ω	V_{GS} = -4.5V, I_{D2} = -0.33A ④
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.0	V	V_{DS} = V_{GS}, I_D = -250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	3.1	—	mV/°C	
Gfs	Forward Transconductance	0.8	—	—	S	V_{DS} = -10V, I_{D2} = -0.33A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	µA	V_{DS} = -48V, V_{GS} = 0V
		—	—	-10		V_{DS} = -48V, V_{GS} = 0V, T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -10V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 10V
Q_G	Total Gate Charge	—	—	3.6	nC	I_{D1} = -0.53A
Q_{GS}	Gate-to-Source Charge	—	—	1.5		V_{DS} = -30V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	1.8		V_{GS} = -4.5V
$t_{d(on)}$	Turn-On Delay Time	—	—	22	ns	V_{DD} = -30V
Tr	Rise Time	—	—	22		I_{D1} = -0.53A
$t_{d(off)}$	Turn-Off Delay Time	—	—	27		R_G = 24Ω
t_f	Fall Time	—	—	27		V_{GS} = -5.0V
$L_S + L_D$	Total Inductance	—	8.4	—	nH	Measured from center of Drain pad to center of source pad
C_{iss}	Input Capacitance	—	167	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	43	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	10	—		f = 100KHz
R_G	Gate Resistance	—	56	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-0.53	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-2.12		
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_J =25°C, I_S =-0.53A, V_{GS} =0V ④
t_{rr}	Reverse Recovery Time	—	—	50	ns	T_J = 25°C, I_F = -0.53A, V_{DD} ≤ 25V, di/dt = -100A/µs ④
Q_{rr}	Reverse Recovery Charge	—	—	25	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	220	°C/W
$R_{\theta JL}$	Junction-to-Lead	—	—	40	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② V_{DD} = -25V, starting T_J = 25°C, L =238mH, Peak I_L = -0.53A, V_{GS} = -10V
③ I_{SD} ≤ -0.53A, di/dt ≤ -100A/µs, V_{DD} ≤ -60V, T_J ≤ 150°C
④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
⑤ Total Dose Irradiation with V_{GS} Bias. -10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
⑥ Total Dose Irradiation with V_{DS} Bias. -48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 300 kRads (Si) [1] Min.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	——	V	V_{GS} = 0V, I_D = -250µA
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0	V	V_{DS} = V_{GS}, I_D = -250µA
I_{GSS}	Gate-to-Source Leakage Forward	——	-100	nA	V_{GS} = -10V
I_{GSS}	Gate-to-Source Leakage Reverse	——	100	nA	V_{GS} = 10V
I_{DSS}	Zero Gate Voltage Drain Current	——	-1.0	µA	V_{DS} = -48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	——	1.36	Ω	V_{GS} = -4.5V, I_{D2} = -0.33A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (UB)	——	1.40	Ω	V_{GS} = -4.5V, I_{D2} = -0.33A
V_{SD}	Diode Forward Voltage	——	-5.0	V	V_{GS} = 0V, I_S = -0.53A

1. Part numbers IRHLUB7970Z4, IRHLUB7930Z4 and additional part numbers listed on page 10

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm^2))	Energy (MeV)	Range (µm)	VDS (V) @ VGS = 0V	@ VGS = 2V	@ VGS = 4V	@ VGS = 5V	@ VGS = 6V	@ VGS = 7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-60	-60	-60	-60	-60	-50
62 ± 5%	355 ± 7.5%	33 ± 7.5%	-60	-60	-60	-60	-60	——
85 ± 5%	380 ± 7.5%	29 ± 7.5%	-60	-60	-60	-60	——	——

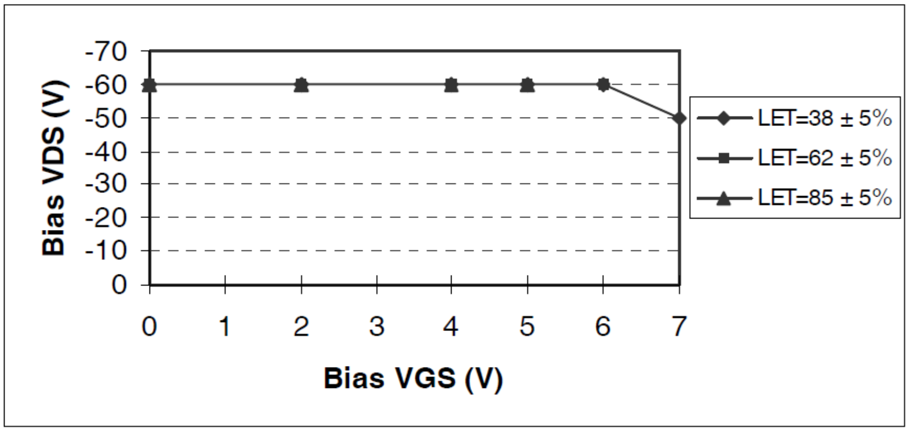


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

Pre-Irradiation

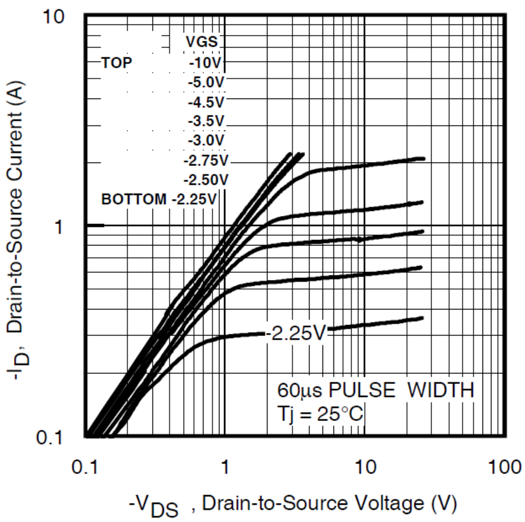


Fig 1. Typical Output Characteristics

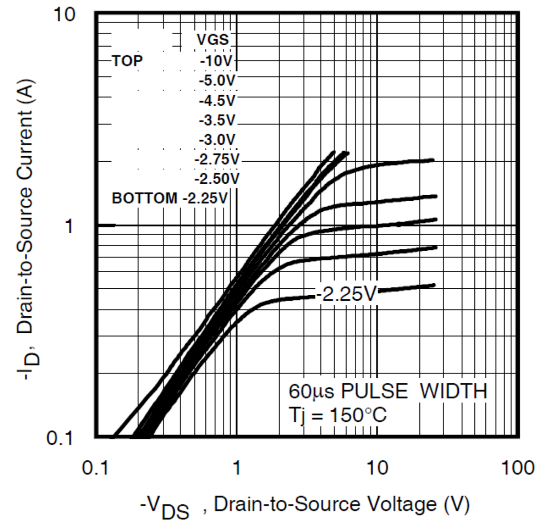


Fig 2. Typical Output Characteristics

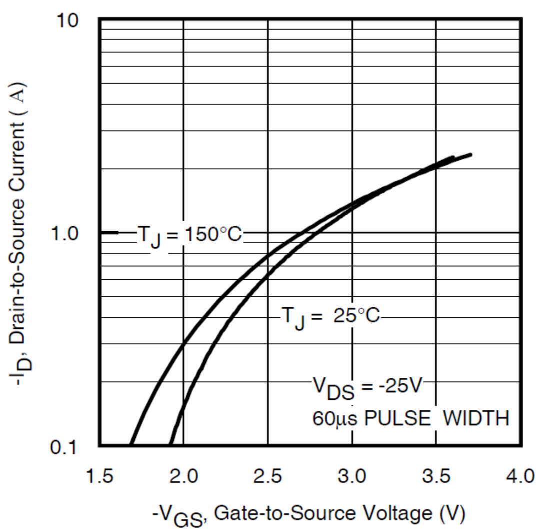


Fig 3. Typical Transfer Characteristics

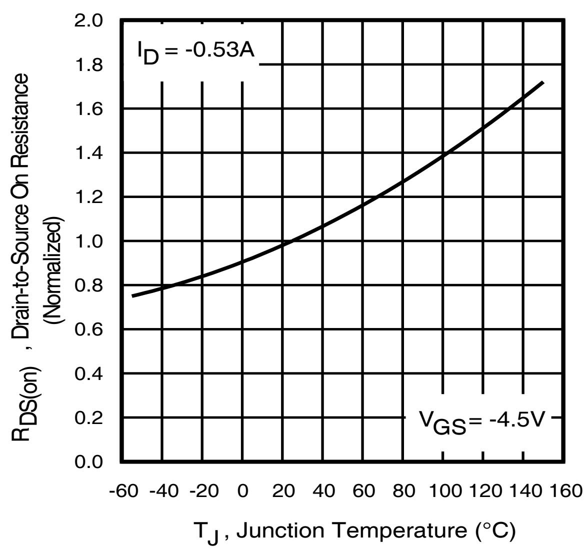


Fig 4. Normalized On-Resistance Vs. Temperature

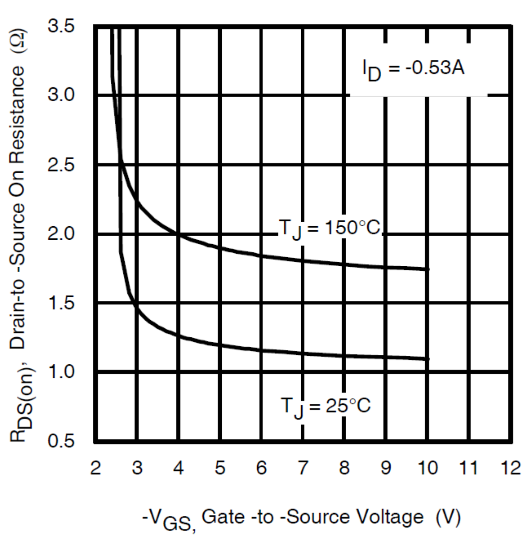


Fig 5. Typical On-Resistance Vs Gate Voltage

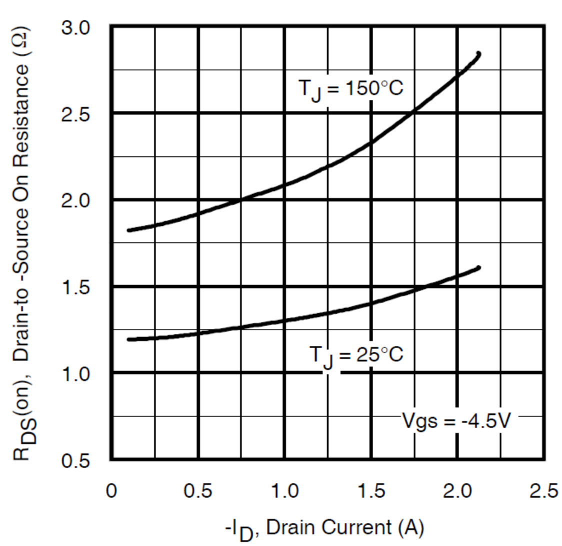


Fig 6. Typical On-Resistance Vs Drain Current

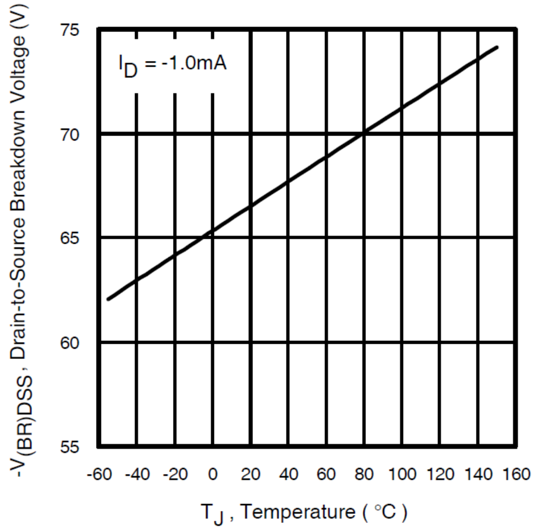


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

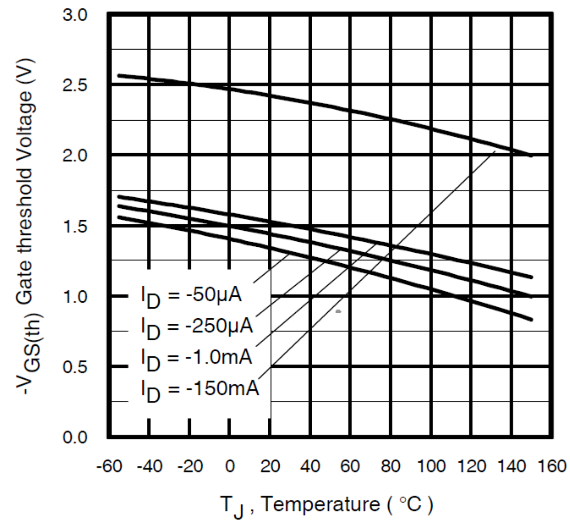


Fig 8. Typical Threshold Voltage Vs Temperature

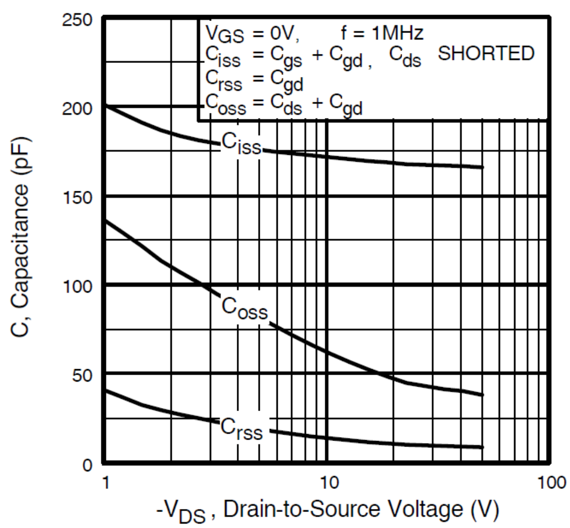


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

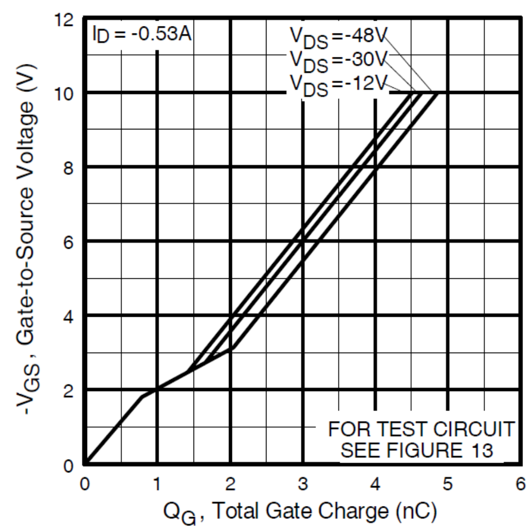


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

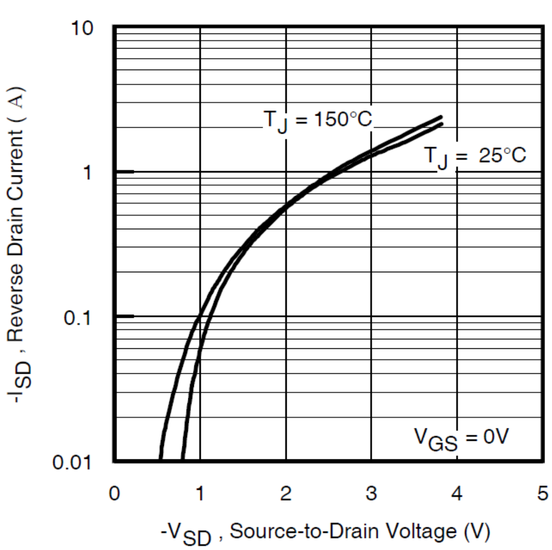


Fig 11. Typical Source-Drain Diode Forward Voltage

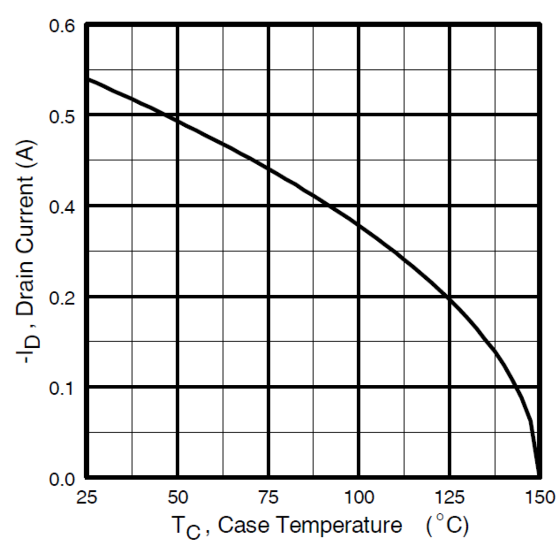


Fig 12. Maximum Drain Current Vs.Case Temperature

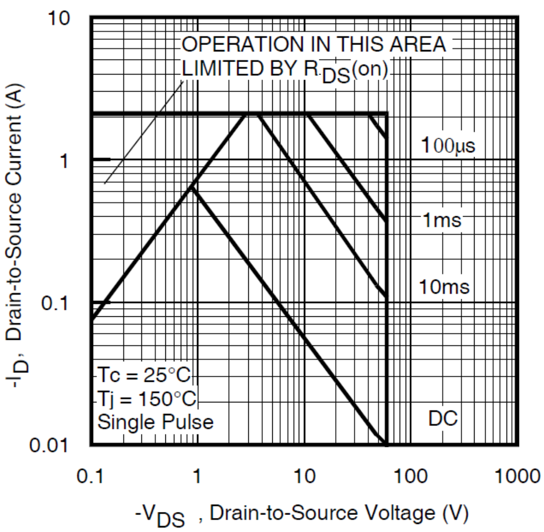


Fig 13. Maximum Safe Operating Area

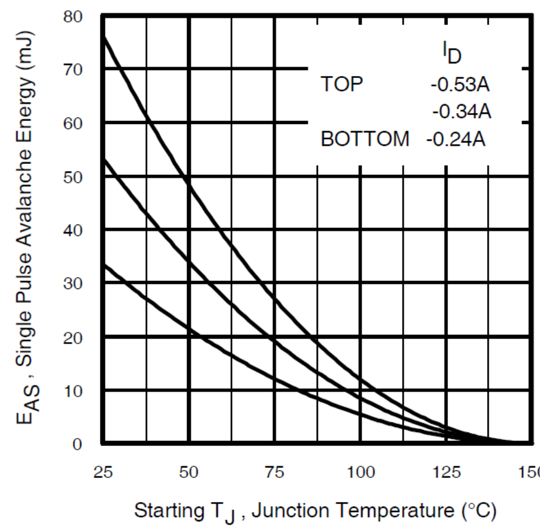


Fig 14. Maximum Avalanche Energy Vs. Drain Current

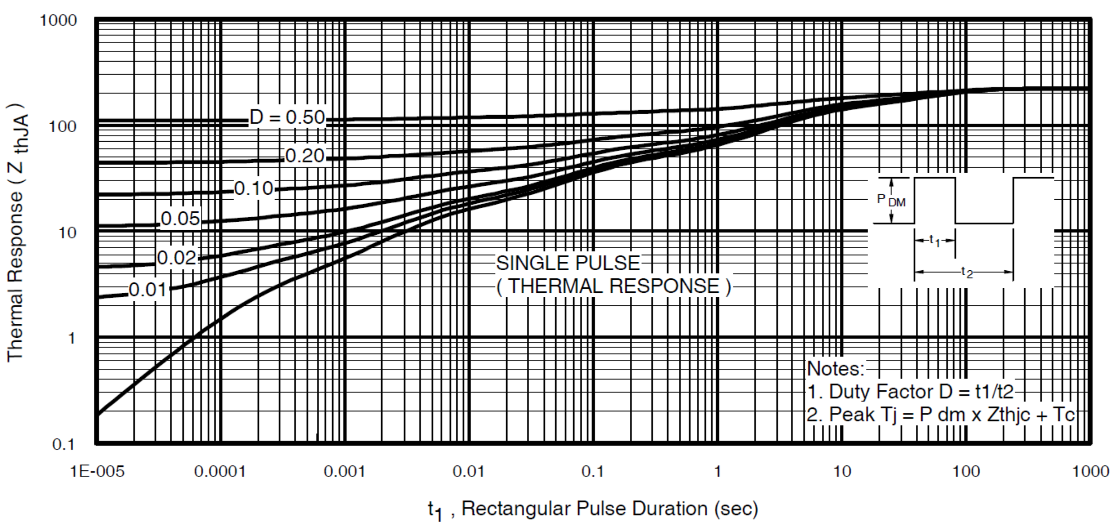


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

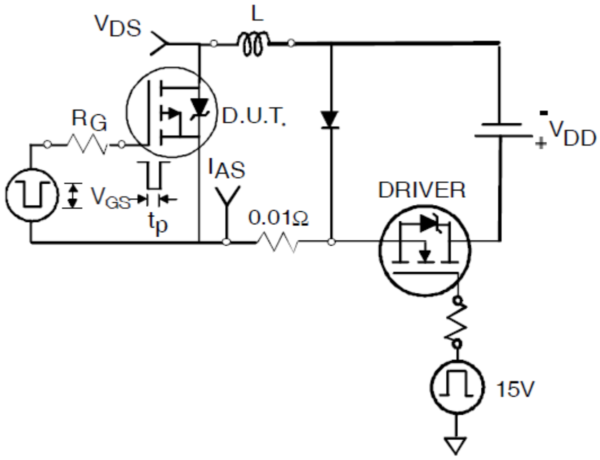


Fig 16a. Unclamped Inductive Test Circuit

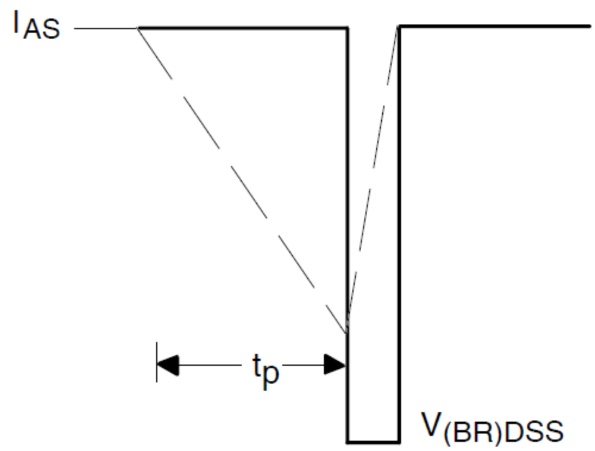


Fig 16b. Unclamped Inductive Waveforms

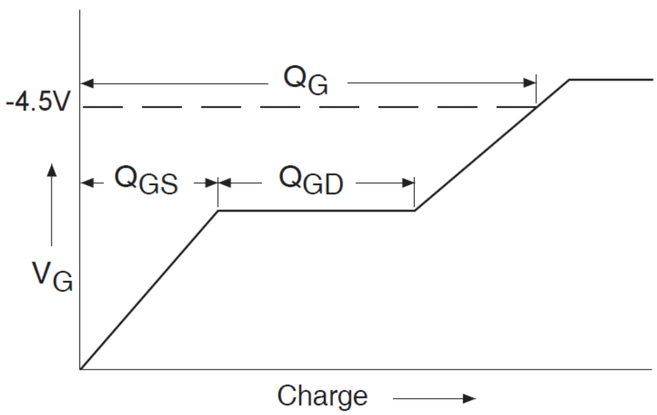


Fig 17a. Gate Charge Waveform

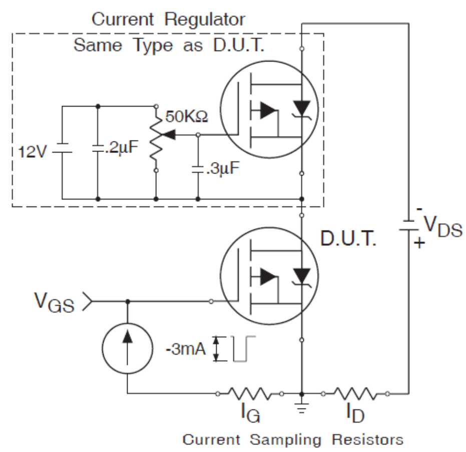


Fig 17b. Gate Charge Test Circuit

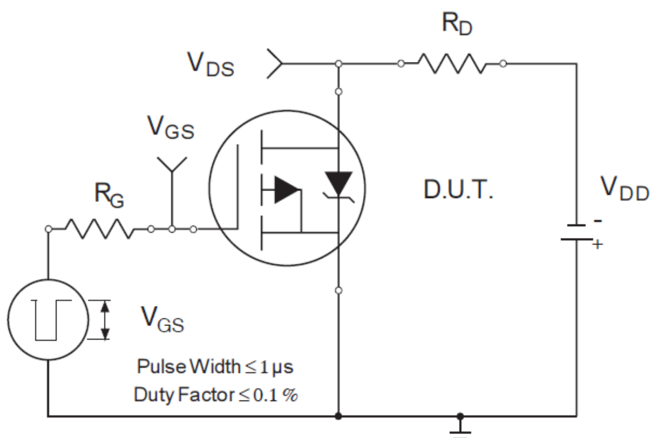


Fig 18a. Switching Time Test Circuit

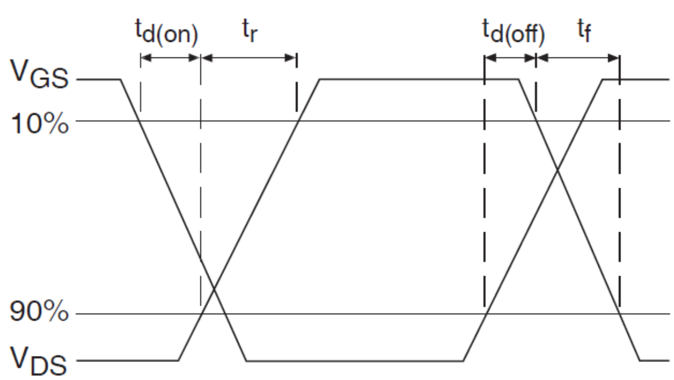
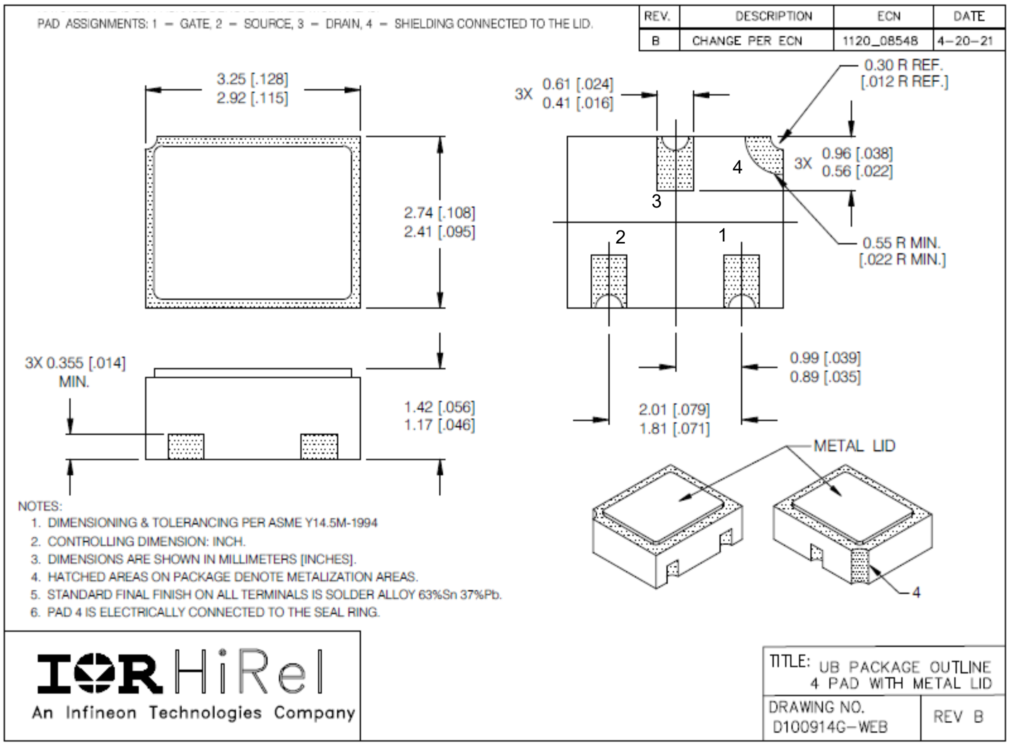


Fig 18b. Switching Time Waveforms

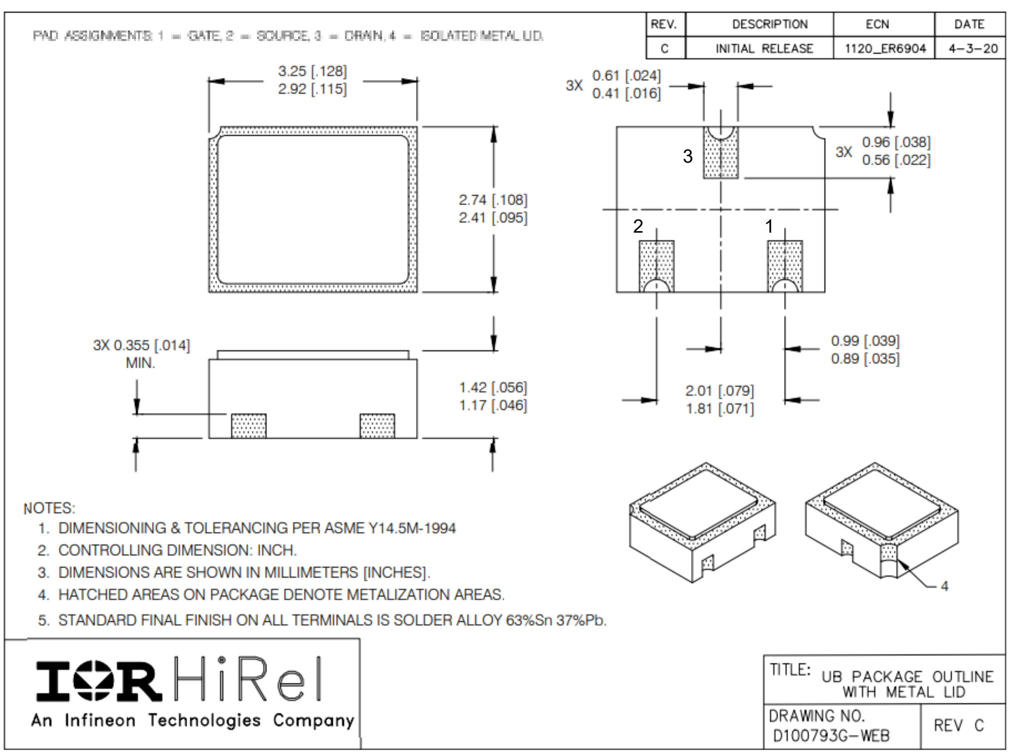
Note: For the most updated package outline, please see the website: UB

Case Outline and Dimensions - UB (Shielded Metal Lid Connected to 4th Pad)



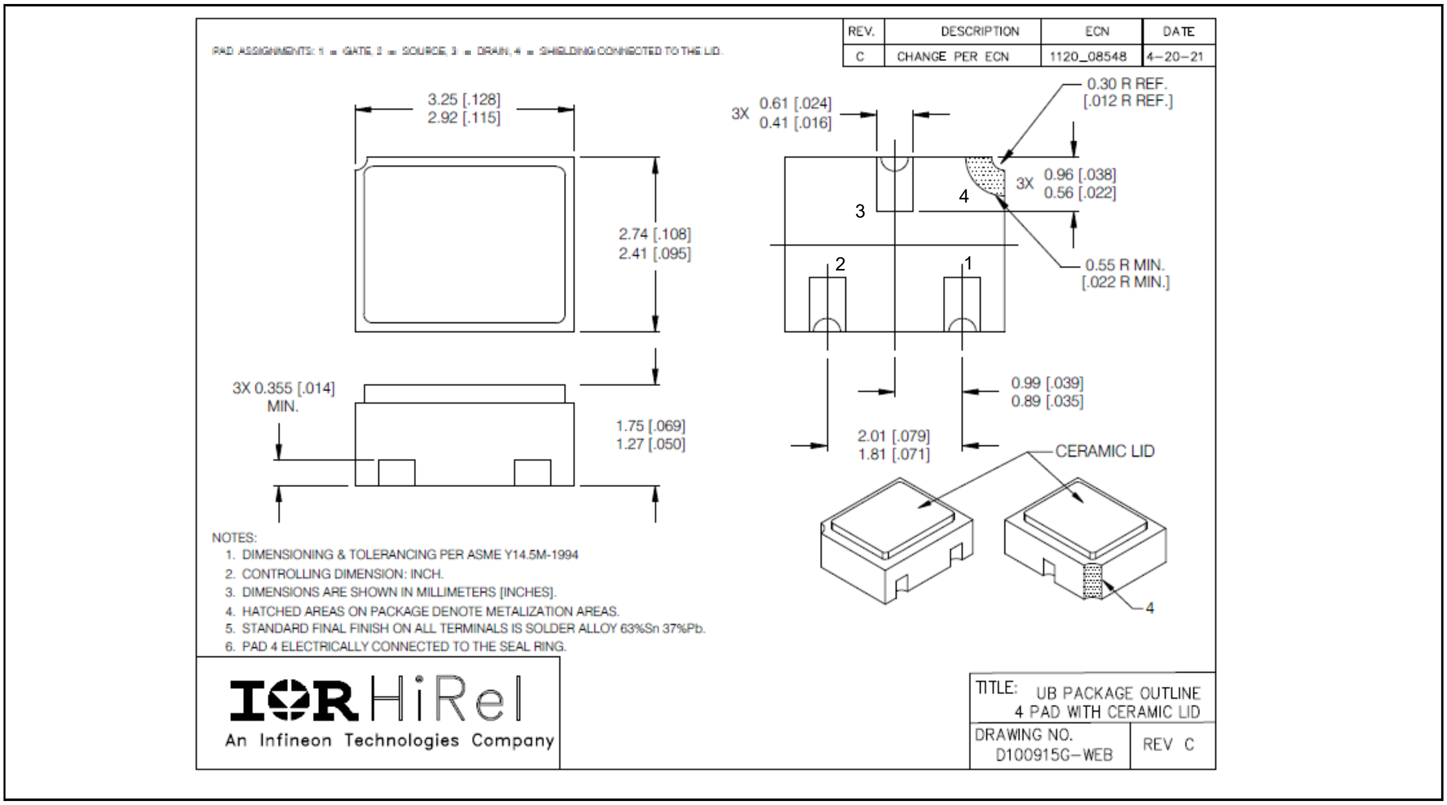
Note: For the most updated package outline, please see the website: UBN

Case Outline and Dimensions - UBN (Isolated Metal Lid, No 4th Pad)



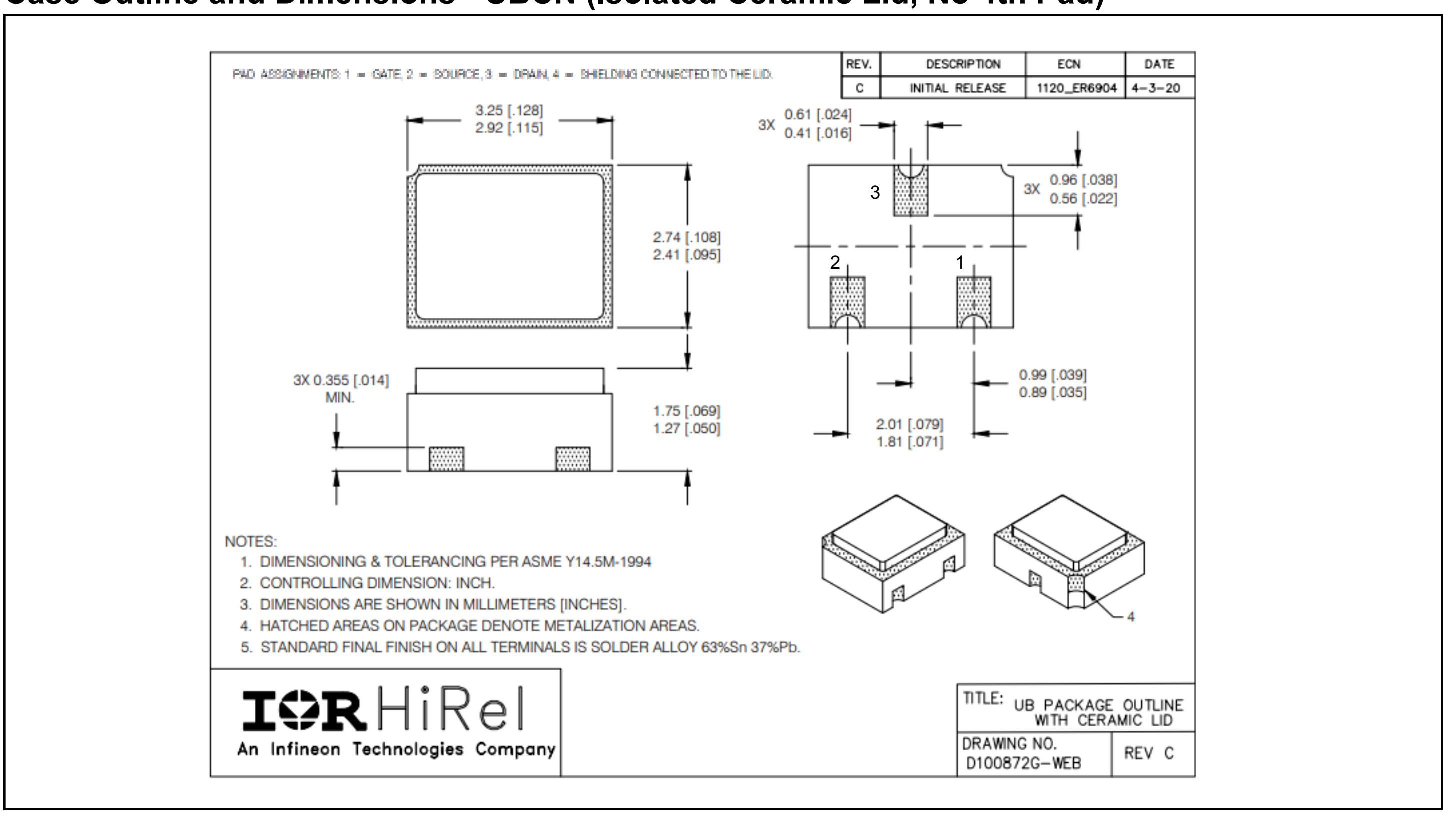
Note: For the most updated package outline, please see the website: [UBC](UBC)

Case Outline and Dimensions - UBC (Shielded Ceramic Lid Connected to 4th Pad)



Note: For the most updated package outline, please see the website: UBCN

Case Outline and Dimensions - UBCN (Isolated Ceramic Lid, No 4th Pad)



Additional Product Summary (continued from pages 1 and 3)

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number	 UBN (ISOLATED METAL LID)
IRHLUBN7970Z4	100 kRads(Si)	1.4Ω	-0.53A	JANSR2N7626UBN	
IRHLUBN7930Z4	300 kRads(Si)	1.4Ω	-0.53A	JANSF2N7626UBN	

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number	 UBC (SHIELDED CERAMIC LID)
IRHLUBC7970Z4	100 kRads(Si)	1.4Ω	-0.53A	JANSR2N7626UBC	
IRHLUBC7930Z4	300 kRads(Si)	1.4Ω	-0.53A	JANSF2N7626UBC	

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number	 UBCN (ISOLATED CERAMIC LID)
IRHLUBCN7970Z4	100 kRads(Si)	1.4Ω	-0.53A	JANSR2N7626UBCN	
IRHLUBCN7930Z4	300 kRads(Si)	1.4Ω	-0.53A	JANSF2N7626UBCN	

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