

IRHNJ597034
JANSR2N7520U3

IRHNJC597034
JANSR2N7520U3C
60V, P-CHANNEL

REF: MIL-PRF-19500/732



**RADIATION HARDENED
POWER MOSFET
SURFACE MOUNT (SMD-0.5)**

Product Summary

Part Number	Radiation Level	R _{D5(on)}	I _D	QPL Part Number
IRHNJ597034	100K Rads (Si)	0.085Ω	-21A	JANSR2N7520U3
IRHNJ593034	300K Rads (Si)	0.085Ω	-21A	JANSF2N7520U3

Refer to Page 8 for Additional Part Number -
IRHNJC597034 - SMD-0.5 (Ceramic Lid)



International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low R_{D5(on)} and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Ultra Low R_{D5(on)}
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

	Parameter	Units	
I _D @ V _{GS} = -12V, T _C = 25°C	Continuous Drain Current	A	-21
I _D @ V _{GS} = -12V, T _C = 100°C	Continuous Drain Current		-13.3
I _{DM}	Pulsed Drain Current ①		-84
P _D @ T _C = 25°C	Max. Power Dissipation	W	75
	Linear Derating Factor	W/°C	0.6
V _{GS}	Gate-to-Source Voltage	V	±20
E _{AS}	Single Pulse Avalanche Energy ②	mJ	110
I _{AR}	Avalanche Current ①	A	-21
E _{AR}	Repetitive Avalanche Energy ①	mJ	7.5
dv/dt	Peak Diode Recovery dv/dt ③	V/ns	-2.0
T _J	Operating Junction	°C	-55 to 150
T _{STG}	Storage Temperature Range		
	Pckg. Mounting Surface Temp.		300 (for 5s)
	Weight	g	1.0 (Typical)

For footnotes refer to the last page

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1

02/11/15

Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	-60	—	—	V	$V_{GS} = 0\text{V}, I_D = -1.0\text{mA}$
$\Delta BVDSS/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.063	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1.0\text{mA}$
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.085	Ω	$V_{GS} = -12\text{V}, I_D = -13.3\text{A}_4$
VGS(th)	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -1.0\text{mA}$
gfs	Forward Transconductance	10	—	—	S	$V_{DS} = -15\text{V}, I_{DS} = -13.3\text{A}_4$
IDSS	Zero Gate Voltage Drain Current	—	—	-10	μA	$V_{DS} = -48\text{V}, V_{GS} = 0\text{V}$
		—	—	-25		$V_{DS} = -48\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
IGSS	Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20\text{V}$
IGSS	Gate-to-Source Leakage Reverse	—	—	100		$V_{GS} = 20\text{V}$
Qg	Total Gate Charge	—	—	45	nC	$V_{GS} = -12\text{V}, I_D = -21\text{A}$
Qgs	Gate-to-Source Charge	—	—	18		$V_{DS} = -30\text{V}$
Qgd	Gate-to-Drain ('Miller') Charge	—	—	13		
td(on)	Turn-On Delay Time	—	—	25	ns	
tr	Rise Time	—	—	65		
td(off)	Turn-Off Delay Time	—	—	75		
tf	Fall Time	—	—	50		
LS + LD	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
Ciss	Input Capacitance	—	1540	—	pF	$V_{GS} = 0\text{V}, V_{DS} = -25\text{V}$ $f = 1.0\text{MHz}$
Coss	Output Capacitance	—	590	—		
Crss	Reverse Transfer Capacitance	—	60	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
IS	Continuous Source Current (Body Diode)	—	—	-21	A	
ISM	Pulse Source Current (Body Diode) ①	—	—	-84		
VSD	Diode Forward Voltage	—	—	-5.0	V	$T_j = 25^\circ\text{C}, I_S = -21\text{A}, V_{GS} = 0\text{V}_4$
trr	Reverse Recovery Time	—	—	100	ns	$T_j = 25^\circ\text{C}, I_F = -21\text{A}, dI/dt \leq -100\text{A}/\mu\text{s}$
		—	—	200		
QRR	Reverse Recovery Charge	—	—	nC		$V_{DD} \leq -25\text{V}_4$
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
RthJC	Junction-to-Case	—	—	1.67	$^\circ\text{C/W}$	
RthJ-PCB	Junction-to-PC board	—	6.9	—		soldered to a 2" sq. copper-clad board

Note: Corresponding Spice and Saber models are available on International Rectifier website.

For footnotes refer to the last page

Radiation Characteristics

IRHNJ597034, JANSR2N7520U3

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ $T_j = 25^\circ\text{C}$, Post Total Dose Irradiation ⁽⁵⁾⁽⁶⁾

	Parameter	100K Rads(Si) ¹		300KRads(Si) ²		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	-60	—	V	$\text{V}_{\text{GS}} = 0\text{V}, \text{I}_D = -1.0\text{mA}$
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	-2.0	-4.0	-2.0	-5.0		$\text{V}_{\text{GS}} = \text{V}_{\text{DS}}, \text{I}_D = -1.0\text{mA}$
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	$\text{V}_{\text{GS}} = -20\text{V}$
I_{GSS}	Gate-to-Source Leakage Reverse	—	100	—	100		$\text{V}_{\text{GS}} = 20\text{ V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	-10	—	-10	μA	$\text{V}_{\text{DS}} = -48\text{V}, \text{V}_{\text{GS}} = 0\text{V}$
$\text{R}_{\text{DS(on)}}$	Static Drain-to-Source ⁽⁴⁾ On-State Resistance (TO-3)	—	0.087	—	0.087	Ω	$\text{V}_{\text{GS}} = -12\text{V}, \text{I}_D = -13.3\text{A}$
$\text{R}_{\text{DS(on)}}$	Static Drain-to-Source ⁽⁴⁾ On-State Resistance (SMD-0.5)	—	0.085	—	0.085	Ω	$\text{V}_{\text{GS}} = -12\text{V}, \text{I}_D = -13.3\text{A}$
V_{SD}	Diode Forward Voltage ⁽⁴⁾	—	-5.0	—	-5.0	V	$\text{V}_{\text{GS}} = 0\text{V}, \text{I}_S = -21\text{A}$

1. Part number IRHNJ597034 and additional part number listed on page 8

2. Part number IRHNJ593034 and additional part number listed on page 8

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)				
			@VGS = 0V	@VGS = 5V	@VGS = 10V	@VGS = 15V	@VGS = 20V
38 ± 5%	270 ± 7.5%	35 ± 7.5%	-60	-60	-60	-60	-60
61 ± 5%	330 ± 7.5%	30 ± 7.5%	-60	-60	-60	-45	-25
84 ± 5%	350 ± 10%	28 ± 7.5%	-60	-60	-60	-	-

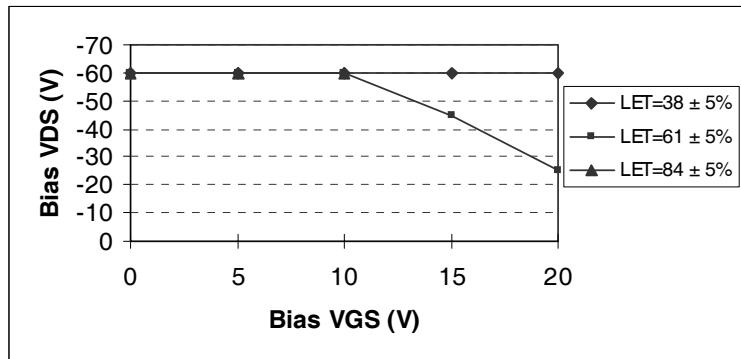


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

IRHNJ597034, JANSR2N7520U3

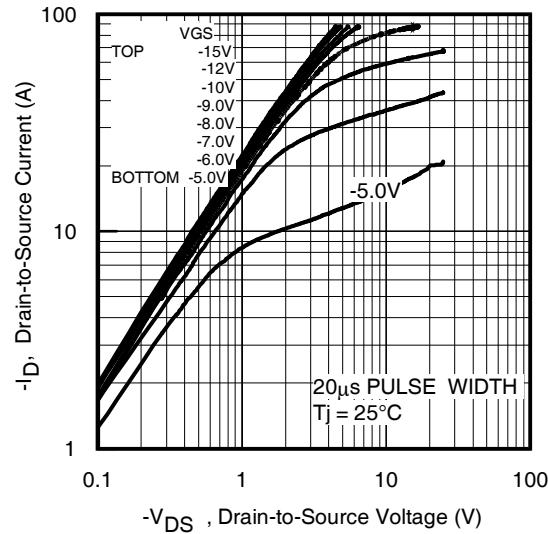


Fig 1. Typical Output Characteristics

Pre-Irradiation

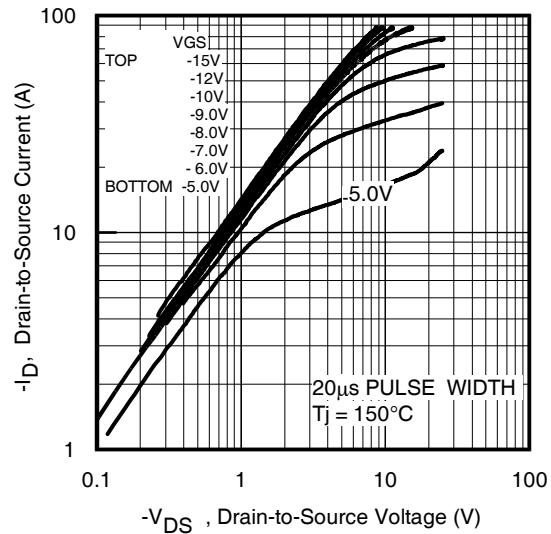


Fig 2. Typical Output Characteristics

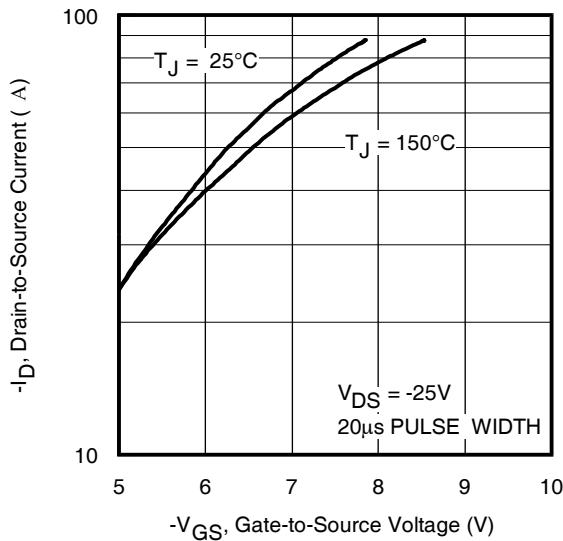


Fig 3. Typical Transfer Characteristics

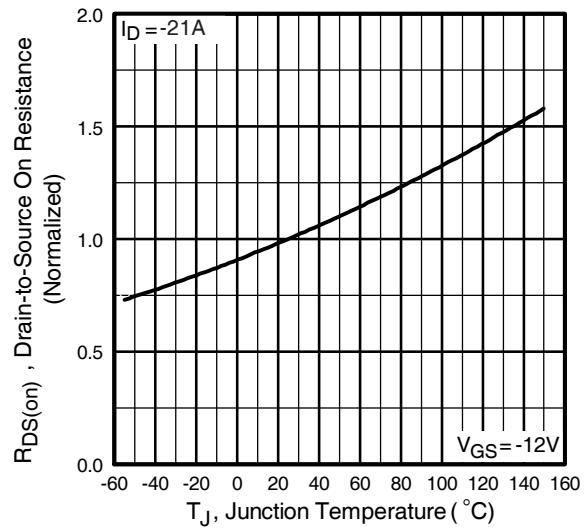


Fig 4. Normalized On-Resistance Vs. Temperature

Pre-Irradiation

IRHNJ597034, JANSR2N7520U3

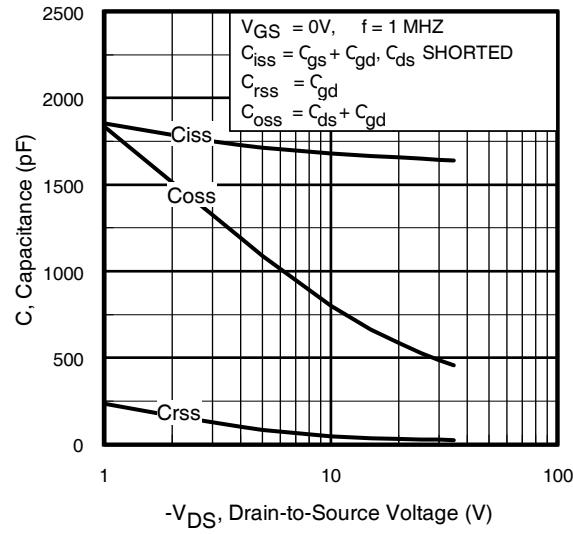


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

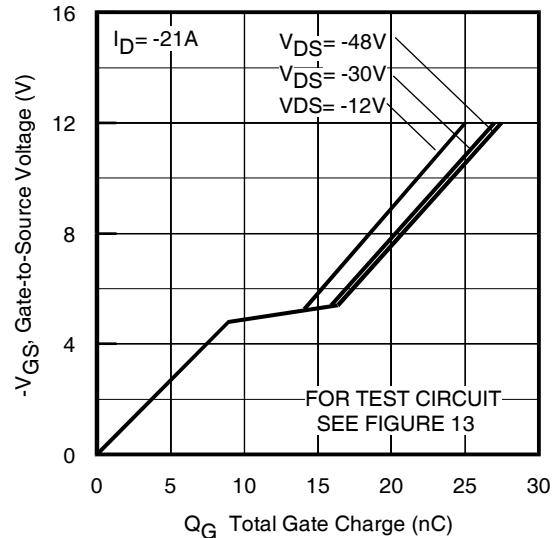


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

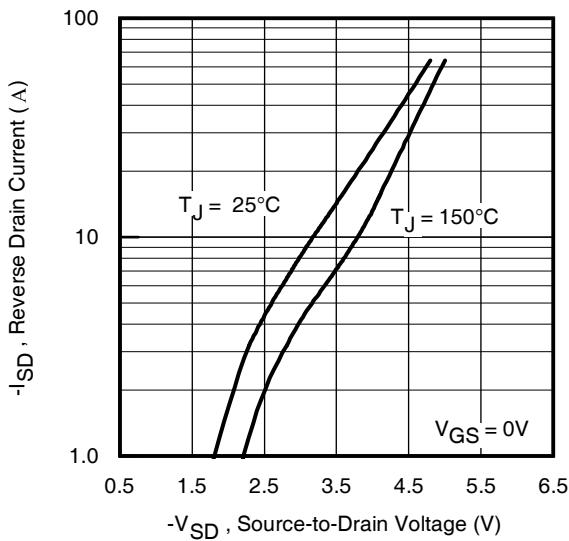


Fig 7. Typical Source-Drain Diode
Forward Voltage

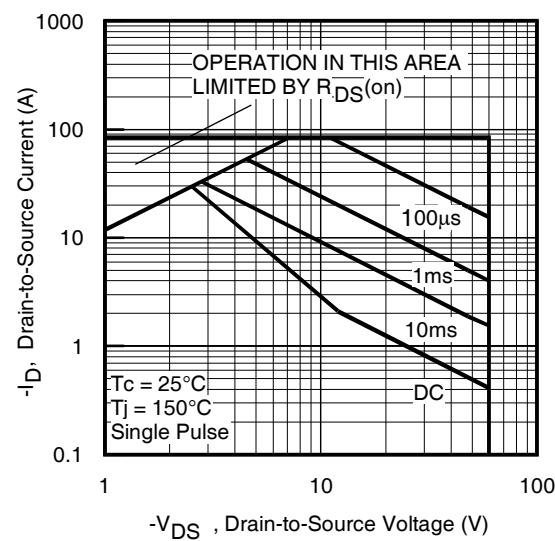


Fig 8. Maximum Safe Operating Area

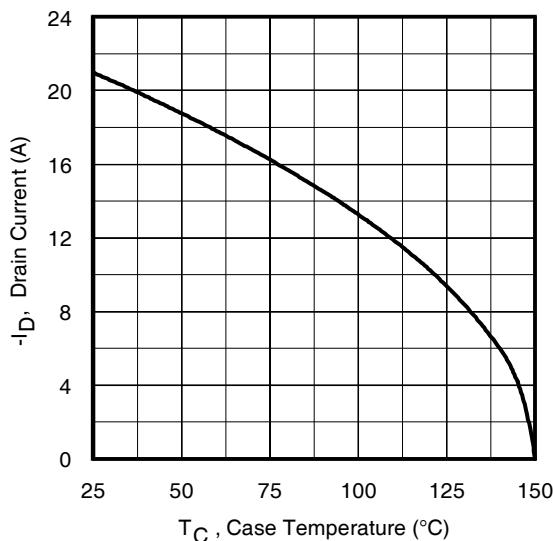


Fig 9. Maximum Drain Current Vs.
Case Temperature

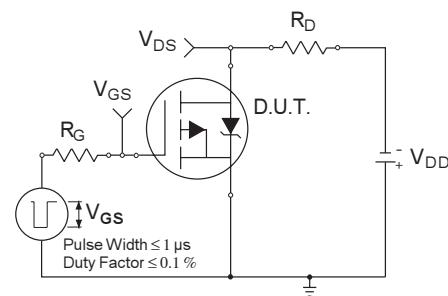


Fig 10a. Switching Time Test Circuit

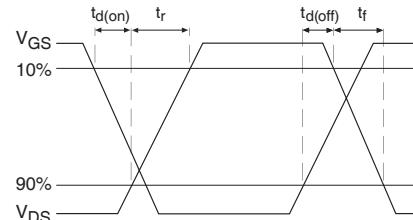


Fig 10b. Switching Time Waveforms

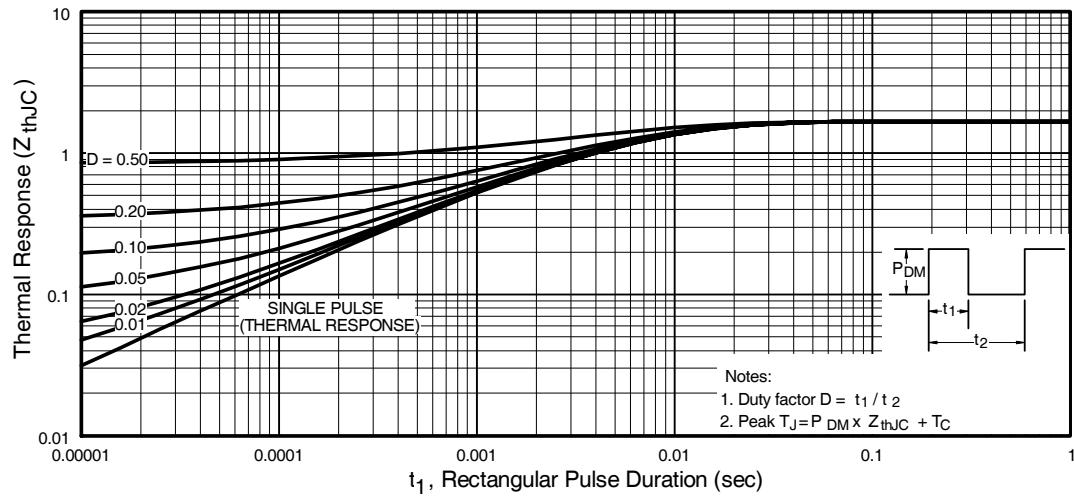


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Pre-Irradiation

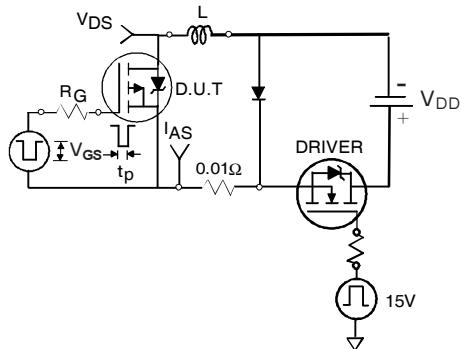


Fig 12a. Unclamped Inductive Test Circuit

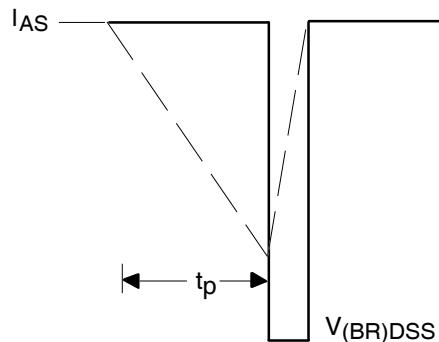


Fig 12b. Unclamped Inductive Waveforms

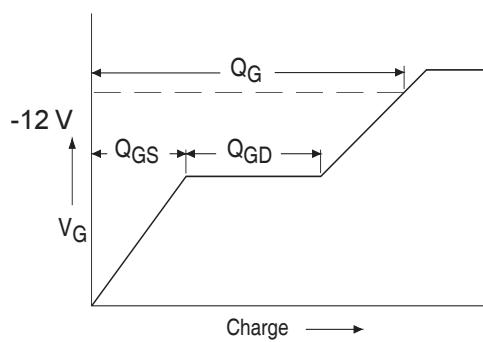


Fig 13a. Basic Gate Charge Waveform

IRHNJ597034, JANSR2N7520U3

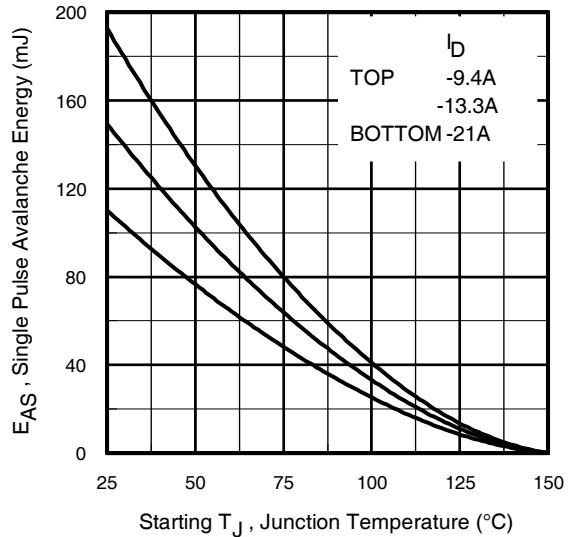


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

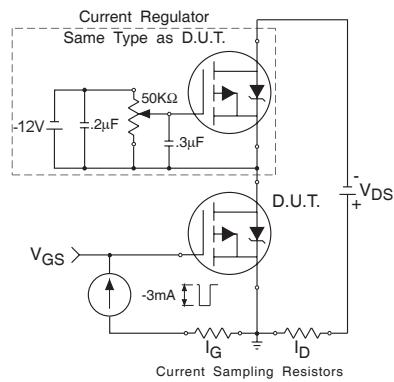


Fig 13b. Gate Charge Test Circuit

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Pre-Irradiation

Footnotes:

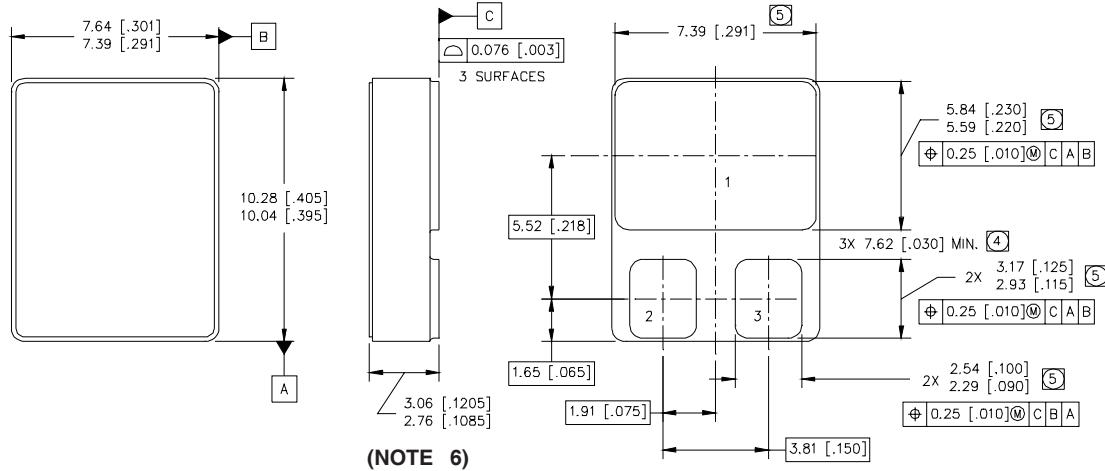
- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
 - ② $V_{DD} = -25V$, starting $T_J = 25^\circ C$, $L = 0.5mH$
Peak $I_L = -21A$, $V_{GS} = -12V$
 - ③ $ISD \leq -21A$, $dI/dt \leq -435A/\mu s$,
 $V_{DD} \leq -60V$, $T_J \leq 150^\circ C$
 - ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
 - ⑤ **Total Dose Irradiation with V_{GS} Bias.**
-12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
 - ⑥ **Total Dose Irradiation with V_{DS} Bias.**
-48 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Additional Product Summary (continued from page 1 and 3)

Product Summary

Part Number	Radiation Level	R _{D5(on)}	Id	QPL Part Number		SMD-0.5 (CERAMIC LID)
IRHNJC597034	100K Rads (Si)	0.085Ω	-21A	JANSR2N7520U3C		
IRHNJC593034	300K Rads (Si)	0.085Ω	-21A	JANSF2N7520U3C		

Case Outline and Dimensions — SMD-0.5 (Metal Lid)



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 ④ DIMENSION INCLUDES METALLIZATION FLASH.
 ⑤ DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.
 6. **For Ceramic Lid, all dimensions are the same, except overall thickness of Maximum 3.40 [.134]**

PAD ASSIGNMENTS

- 1 = DRAIN
2 = GATE
3 = SOURCE

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IR LEOMINSTER : 205 Crawford St., Leominster, Massachusetts 01453, USA Tel: (978) 534-5776

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8

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