



## **OptiMOS<sup>™</sup>3** Power MOS Transistor Chip

Туре	V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub>	Die size	Thickness
IPC302N25N3	250 V	$20 \text{ m}\Omega^{1)}$	6.7 * 4.5 mm <sup>2</sup>	250 μm

## DESCRIPTION

- N-channel enhancement mode
- For additional characteristic and max rating refer to the datasheet of IPP200N25N3 G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AICu system
- Passivation: nitride (only on edge structure)
- Package: sawn on foil

### **Electrical Characteristics on Wafer Level**

at  $T_j = 25 \text{ °C}$ , unless otherwise specified.

Parameter	Symbol	Value			Unit	Conditions
		min.	typ.	max.		
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	250	-	-	V	$V_{GS} = 0V$
						$I_D = 1 \text{ mA}$
Gate threshold voltage	V <sub>GS(th)</sub>	2	3	4	V	$V_{DS} = V_{GS}$
						I <sub>D</sub> = 270 μA
Zero gate voltage drain current	I <sub>DSS</sub>	-	0.1	1	μA	$V_{GS} = 0V$
						V <sub>DS</sub> = 200 V
Gate-source leakage current	I <sub>GSS</sub>	-	1	100	nA	V <sub>GS</sub> = 20 V
						$V_{DS} = 0 V$
Drain-source on-resistance	$R_{\rm DS(on)}$	-	16 <sup>3)</sup>	100 <sup>2)</sup>	mΩ	V <sub>GS</sub> = 10 V
						I <sub>D</sub> = 2 A
Reverse diode forward on-voltage	V <sub>SD</sub>	-	0.7	1.2	V	V <sub>GS</sub> =0 V
						I <sub>F</sub> = 1 A
Avalanche energy, single pulse	Eas	-	40 <sup>4)</sup>	-	mJ	$I_D$ = 30 A, $R_{GS}$ =25 $\Omega$

<sup>1)</sup> packaged in a PG-TO220-3 (see ref. product)

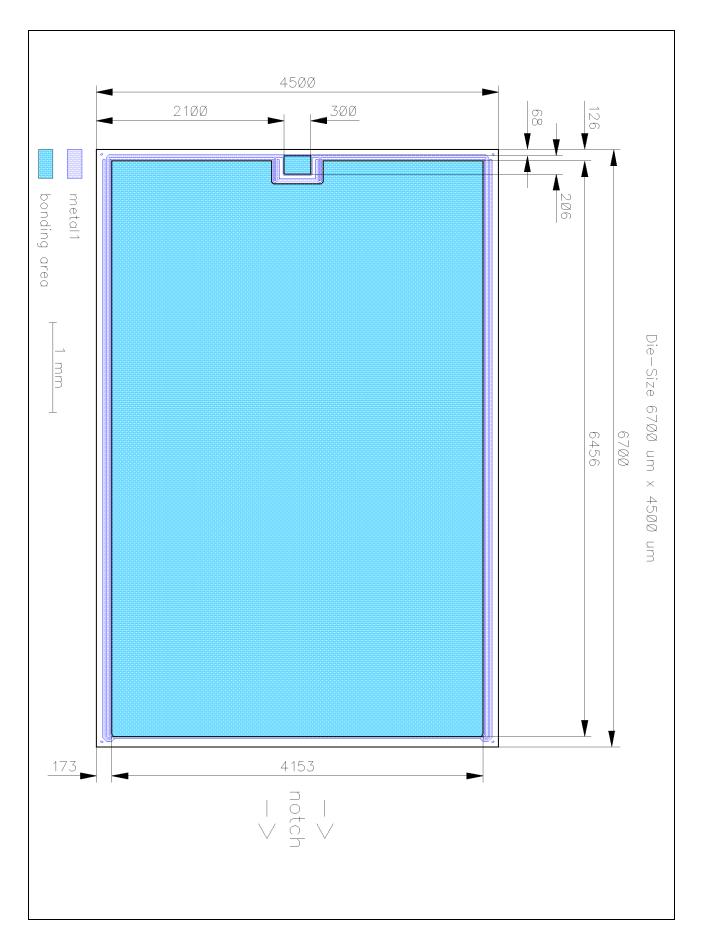
<sup>2)</sup> limited by wafer test-equipment

 $^{3)}$  typical bare die R<sub>DS(on)</sub>; V<sub>GS</sub>=10V

<sup>4)</sup> Wafer tested. For general avalanche capability refer to the datasheet of IPP200N25N3 G



# IPC302N25N3







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