

DirectFET™ N-Channel Power MOSFET

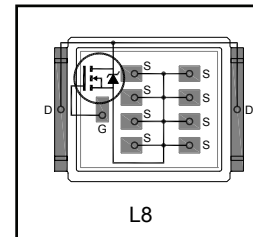
Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits

- Optimized for Logic Level Drive
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Lead-Free, RoHS Compliant

| | |
|--|---------------|
| V_{DSS} | 40V |
| R_{DS(on)} typ. max @ V_{GS} = 10V | 0.34mΩ |
| | 0.45mΩ |
| R_{DS(on)} typ. max @ V_{GS} = 4.5V | 0.52mΩ |
| | 0.70mΩ |
| I_D (Package Limited) | 375A① |



| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|------------------|---------------------------|---------------|----------|-----------------------|
| | | Form | Quantity | |
| IRL7472L1PbF | Direct FET Large Can (L8) | Tape and Reel | 4000 | IRL7472L1TRPbF |

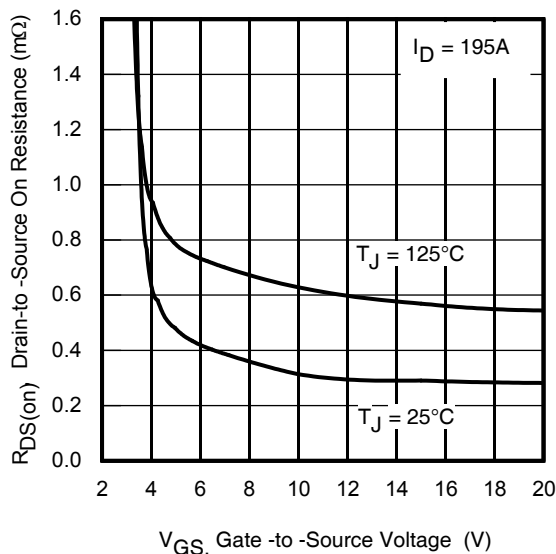


Fig 1. Typical On-Resistance vs. Gate Voltage

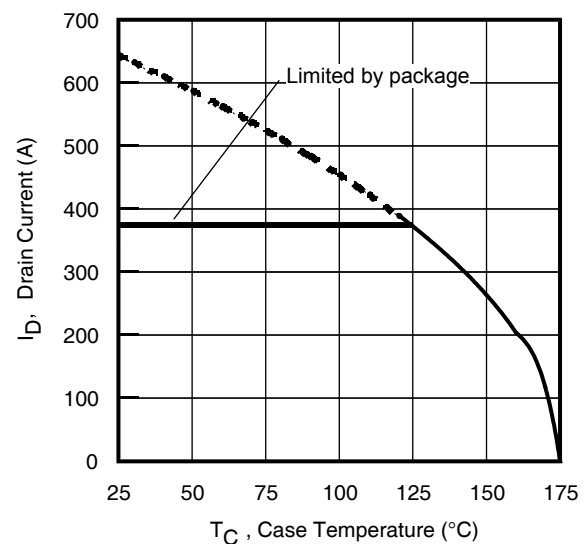


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Ratings

| Symbol | Parameter | Max. | Units |
|---------------------------------|---|--------------|-------|
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited) ① | 645⑩ | A |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited) ① | 456 | |
| $I_D @ T_A = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited) ① | 68 | |
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)④ | 375⑪ | |
| I_{DM} | Pulsed Drain Current ② | 1500 | A |
| $P_D @ T_C = 25^\circ\text{C}$ | Maximum Power Dissipation | 341 | W |
| $P_D @ T_A = 25^\circ\text{C}$ | Maximum Power Dissipation | 3.8 | |
| | Linear Derating Factor | 0.025 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| T_J T_{STG} | Operating Junction and Storage Temperature Range | -55 to + 175 | °C |

Avalanche Characteristics

| | | | |
|------------------------------|---------------------------------|-------------------------|----|
| E_{AS} (Thermally limited) | Single Pulse Avalanche Energy ③ | 308 | mJ |
| E_{AS} (Thermally limited) | Single Pulse Avalanche Energy ⑨ | 765 | |
| I_{AR} | Avalanche Current ② | See Fig.15,16, 23a, 23b | A |
| E_{AR} | Repetitive Avalanche Energy ② | | mJ |

Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|---------------------|-------------------------|------|------|-------|
| $R_{\theta JA}$ | Junction-to-Ambient ① | — | 40 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient ③ | 12.5 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient ② | 20 | — | |
| $R_{\theta JC}$ | Junction-to-Case ④⑧ | — | 0.44 | |
| $R_{\theta JA-PCB}$ | Junction-to-PCB Mounted | 1.0 | — | |

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

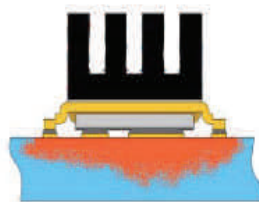
| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|------|------|-------|--|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 40 | — | — | V | $V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 30 | — | mV/°C | Reference to $25^\circ\text{C}, I_D = 5.0\text{mA}$ ② |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 0.34 | 0.45 | mΩ | $V_{GS} = 10\text{V}, I_D = 195\text{A}$ |
| | | — | 0.52 | 0.70 | | $V_{GS} = 4.5\text{V}, I_D = 98\text{A}$ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | 1.7 | 2.5 | V | $V_{DS} = V_{GS}, I_D = 250\mu\text{A}$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 1.0 | μA | $V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$ |
| | | — | — | 150 | | $V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 20\text{V}$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -20\text{V}$ |
| R_G | Internal Gate Resistance | — | 1.0 | — | Ω | |

Notes:

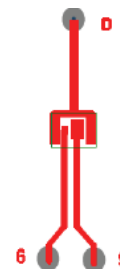
- ① Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ② Used double sided cooling , mounting pad with large heatsink.
- ③ TC measured with thermocouple mounted to top (Drain) of part.



① Surface mounted on 1 in. square Cu board (still air).



② Mounted to a PCB with small clip heatsink (still air)

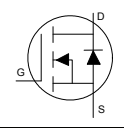


③ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

Dynamic @ T_J = 25°C (unless otherwise specified)

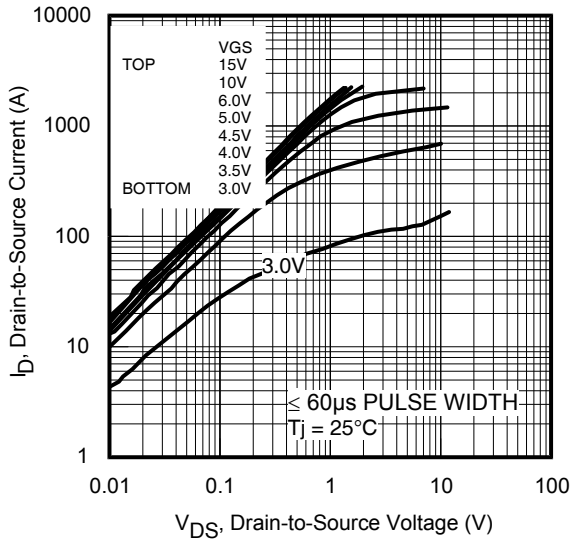
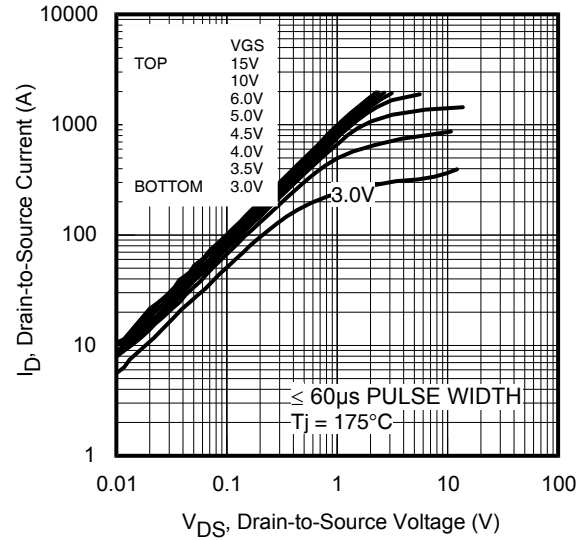
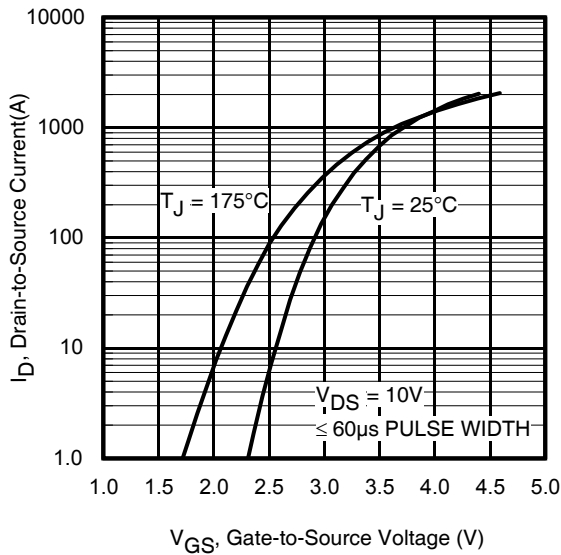
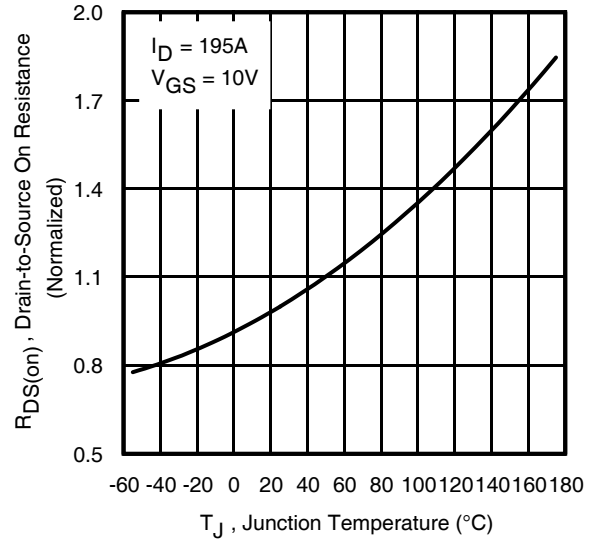
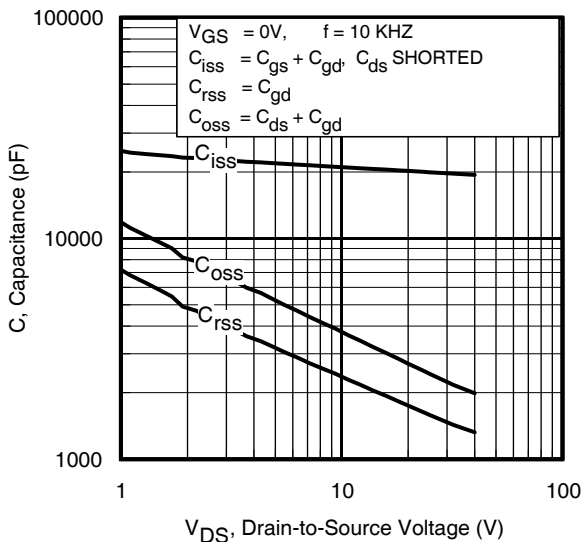
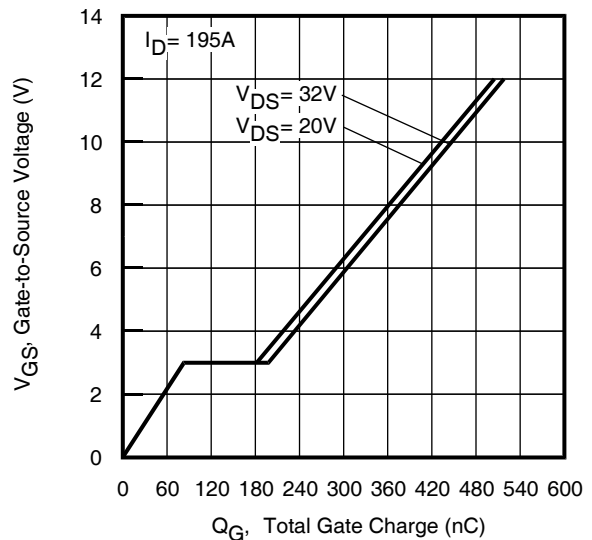
| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------------------------|---|------|-------|------|-------|---|
| g _{fs} | Forward Transconductance | 232 | — | — | S | V _{DS} = 10V, I _D = 195A |
| Q _g | Total Gate Charge | — | 220 | 330 | nC | I _D = 195A |
| Q _{gs} | Gate-to-Source Charge | — | 95 | — | | V _{DS} = 20V |
| Q _{gd} | Gate-to-Drain ("Miller") Charge | — | 87 | — | | V _{GS} = 4.5V ⑤ |
| Q _{sync} | Total Gate Charge Sync. (Q _g - Q _{gd}) | — | 133 | — | | I _D = 195A, V _{DS} = 0V, V _{GS} = 4.5V |
| t _{d(on)} | Turn-On Delay Time | — | 68 | — | ns | V _{DD} = 20V |
| t _r | Rise Time | — | 176 | — | | I _D = 30A |
| t _{d(off)} | Turn-Off Delay Time | — | 174 | — | | R _G = 2.7Ω |
| t _f | Fall Time | — | 137 | — | | V _{GS} = 4.5V ⑤ |
| C _{iss} | Input Capacitance | — | 20082 | — | pF | V _{GS} = 0V |
| C _{oss} | Output Capacitance | — | 2436 | — | | V _{DS} = 25V |
| C _{rss} | Reverse Transfer Capacitance | — | 1594 | — | | f = 10kHz |
| C _{oss} eff. (ER) | Effective Output Capacitance (Energy Related) | — | 2855 | — | | V _{GS} = 0V, V _{DS} = 0V to 32V ⑦ |
| C _{oss} eff. (TR) | Effective Output Capacitance (Time Related) | — | 3544 | — | | V _{GS} = 0V, V _{DS} = 0V to 32V ⑥ |

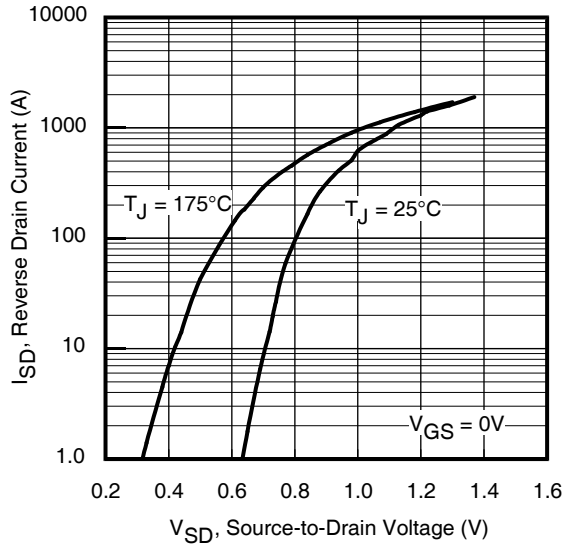
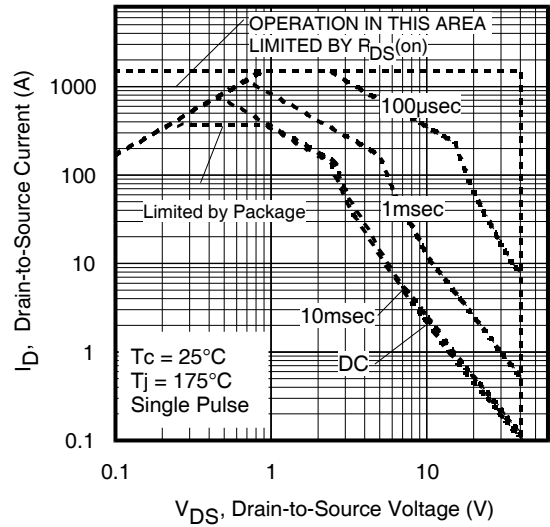
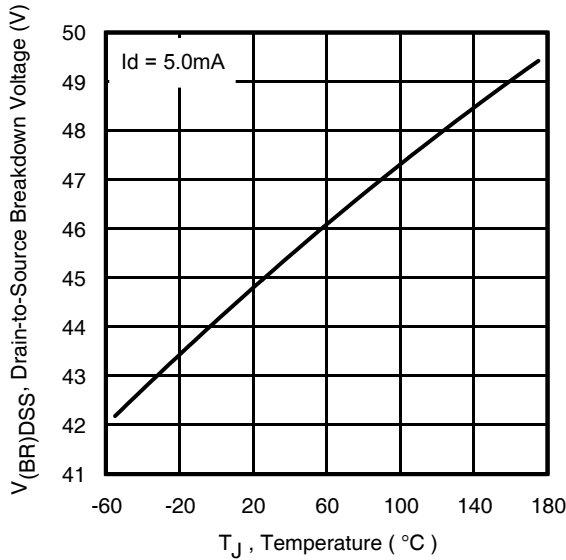
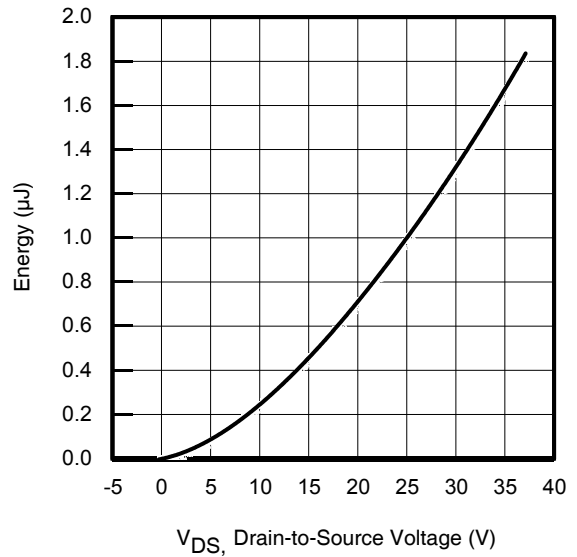
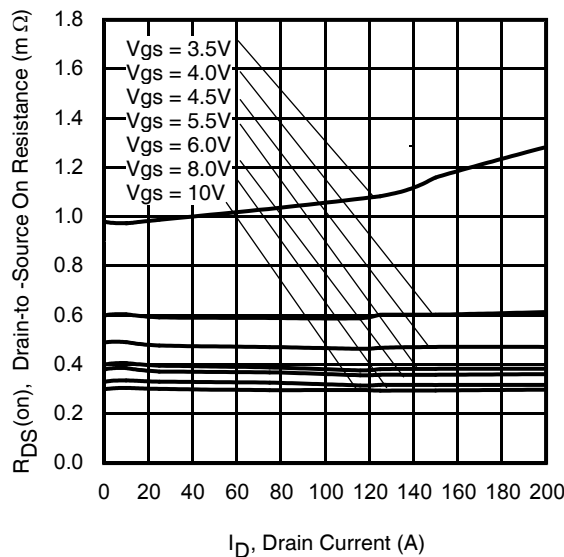
Diode Characteristics

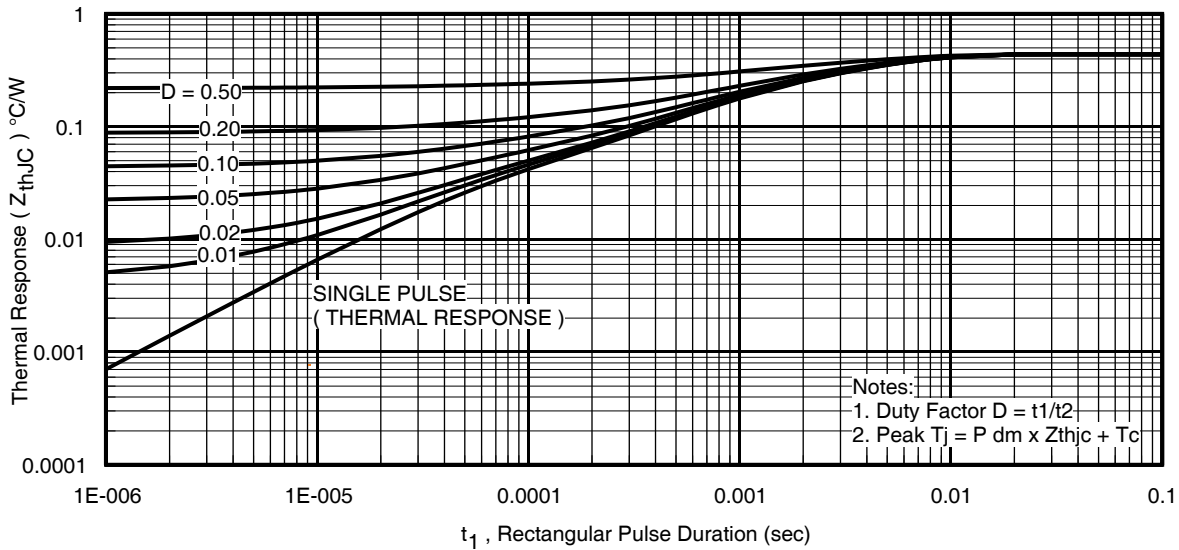
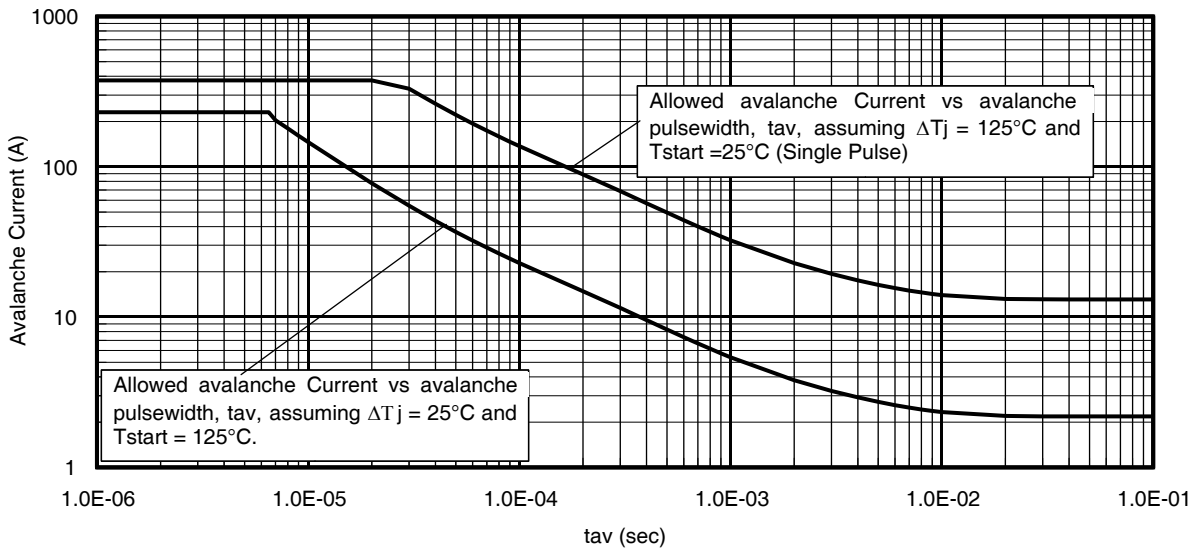
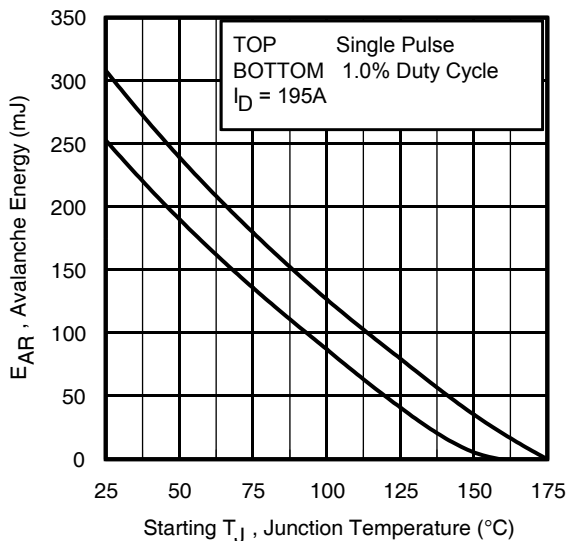
| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|------------------|--|------|------|-------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | 341 ① | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode) ② | — | — | 1500 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.2 | V | T _J = 25°C, I _S = 195A, V _{GS} = 0V ⑤ |
| dv/dt | Peak Diode Recovery ④ | — | 1.3 | — | V/ns | T _J = 175°C, I _S = 195A, V _{DS} = 40V |
| t _{rr} | Reverse Recovery Time | — | 57 | — | ns | T _J = 25°C V _R = 34V, T _J = 125°C I _F = 195A |
| Q _{rr} | Reverse Recovery Charge | — | 103 | — | | |
| | | — | 114 | — | | T _J = 25°C di/dt = 100A/μs ⑤ T _J = 125°C |
| I _{RRM} | Reverse Recovery Current | — | 3.1 | — | A | T _J = 25°C |

Notes:

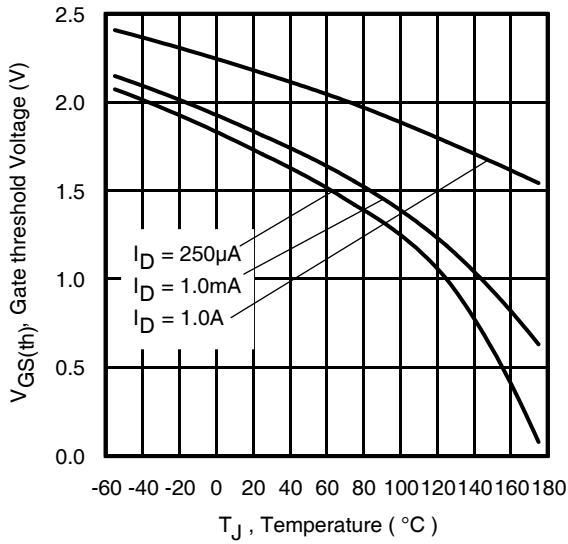
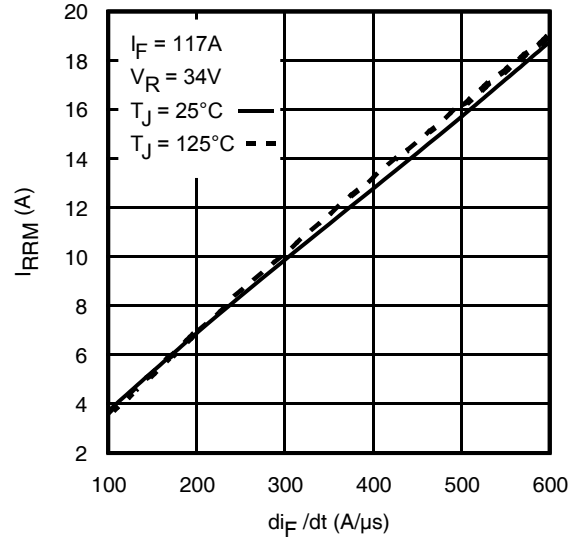
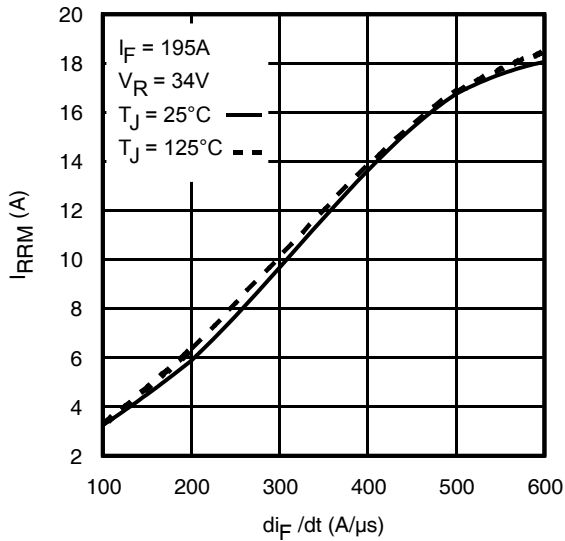
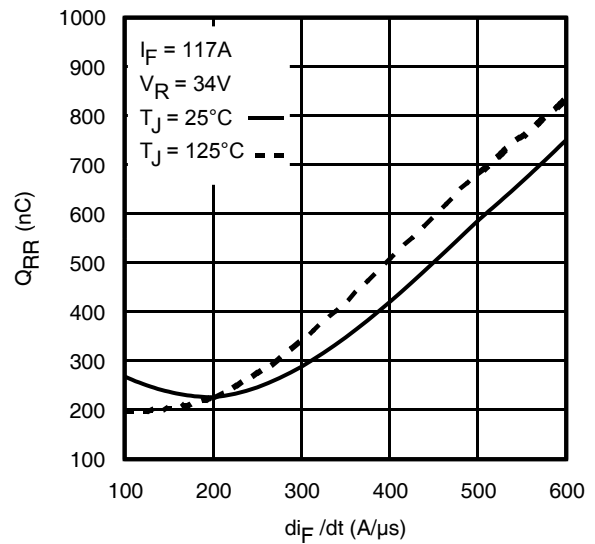
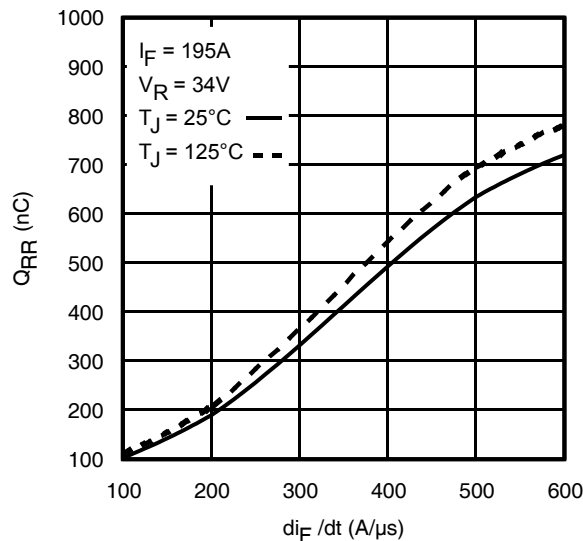
- ① Package limit current based on source connection technology
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.016mH, R_G = 50Ω, I_{AS} = 195A, V_{GS} = 10V.
- ④ I_{SD} ≤ 195A, di/dt ≤ 984A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑧ R_θ is measured at T_J approximately 90°C.
- ⑨ Limited by T_{Jmax}, starting T_J = 25°C, L = 1.0mH, R_G = 50Ω, I_{AS} = 39A, V_{GS} = 10V.
- ⑩ Silicon limit current based on maximum allowable junction temperature T_{Jmax}.

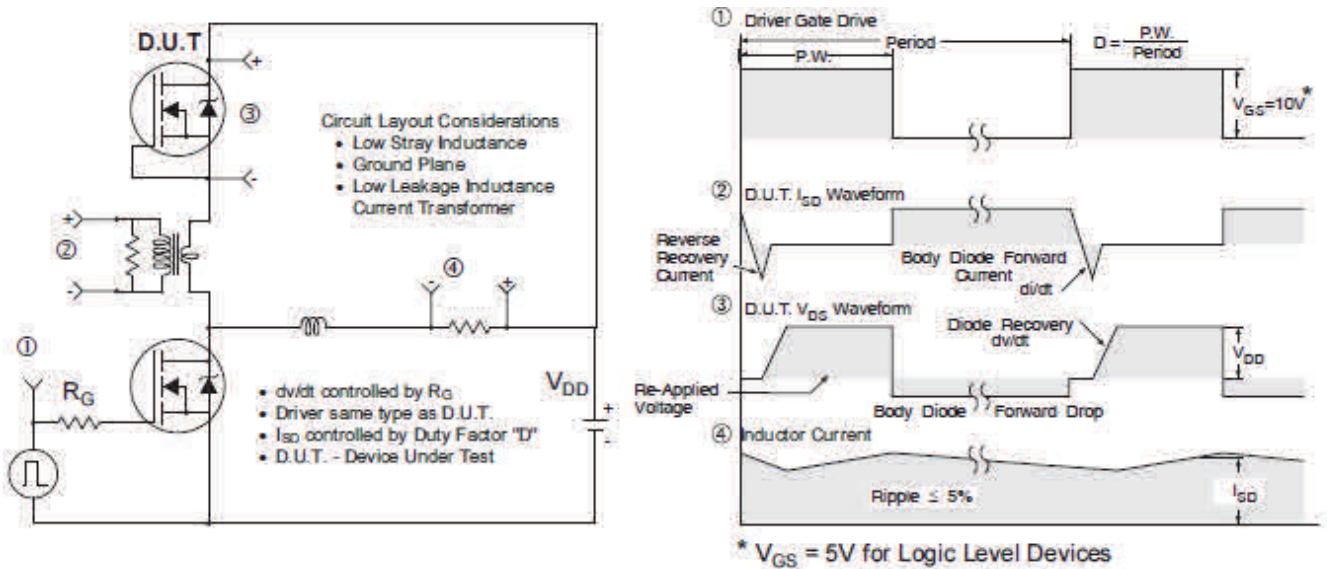
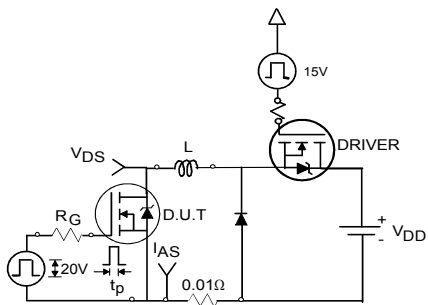
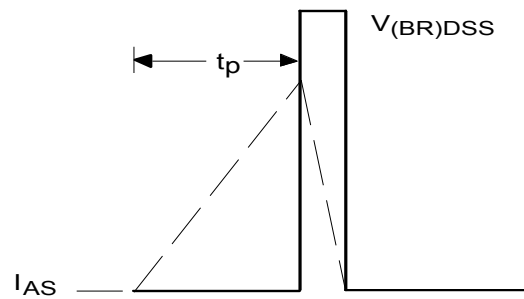
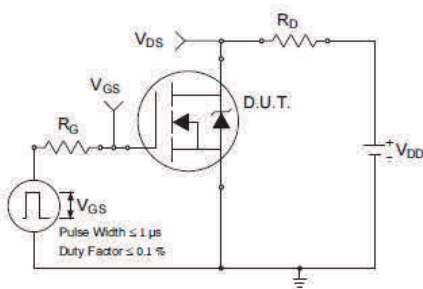
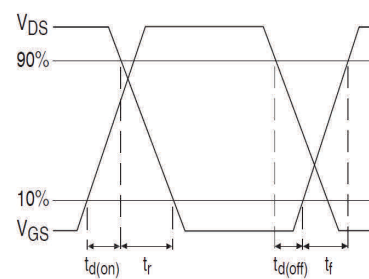
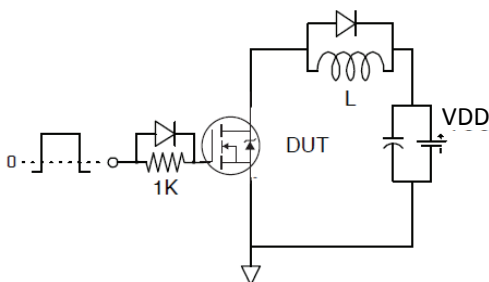
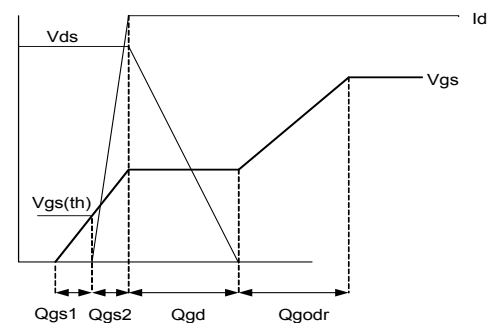

Fig 3. Typical Output Characteristics

Fig 4. Typical Output Characteristics

Fig 5. Typical Transfer Characteristics

Fig 6. Normalized On-Resistance vs. Temperature

Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 9. Typical Source-Drain Diode Forward Voltage

Fig 10. Maximum Safe Operating Area

Fig 11. Drain-to-Source Breakdown Voltage

Fig 12. Typical C_{OSS} Stored Energy

Fig 13. Typical On-Resistance vs. Drain Current


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 15. Avalanche Current vs. Pulse Width

Fig 16. Maximum Avalanche Energy vs. Temperature
**Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005)**

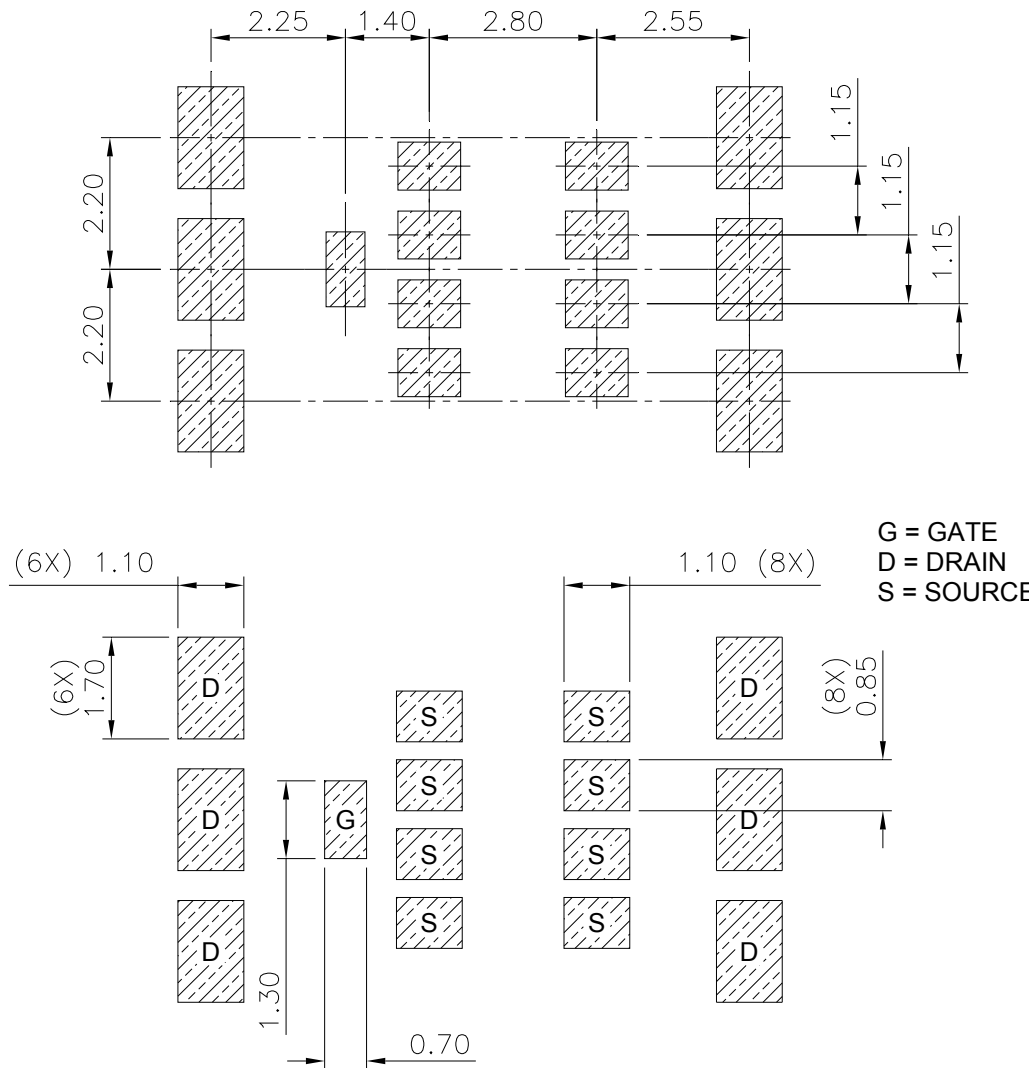
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thjC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thjC}$
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thjC}]$
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


Fig 17. Threshold Voltage vs. Temperature

Fig 18. Typical Recovery Current vs. dif/dt

Fig 19. Typical Recovery Current vs. dif/dt

Fig 20. Typical Stored Charge vs. dif/dt

Fig 21. Typical Stored Charge vs. dif/dt


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 23a. Unclamped Inductive Test Circuit

Fig 23b. Unclamped Inductive Waveforms

Fig 24a. Switching Time Test Circuit

Fig 24b. Switching Time Waveforms

Fig 25a. Gate Charge Test Circuit

Fig 25b. Gate Charge Waveform

**DirectFET™ Board Footprint, L8 Outline
(Large Size Can, 8-Source Pads)**

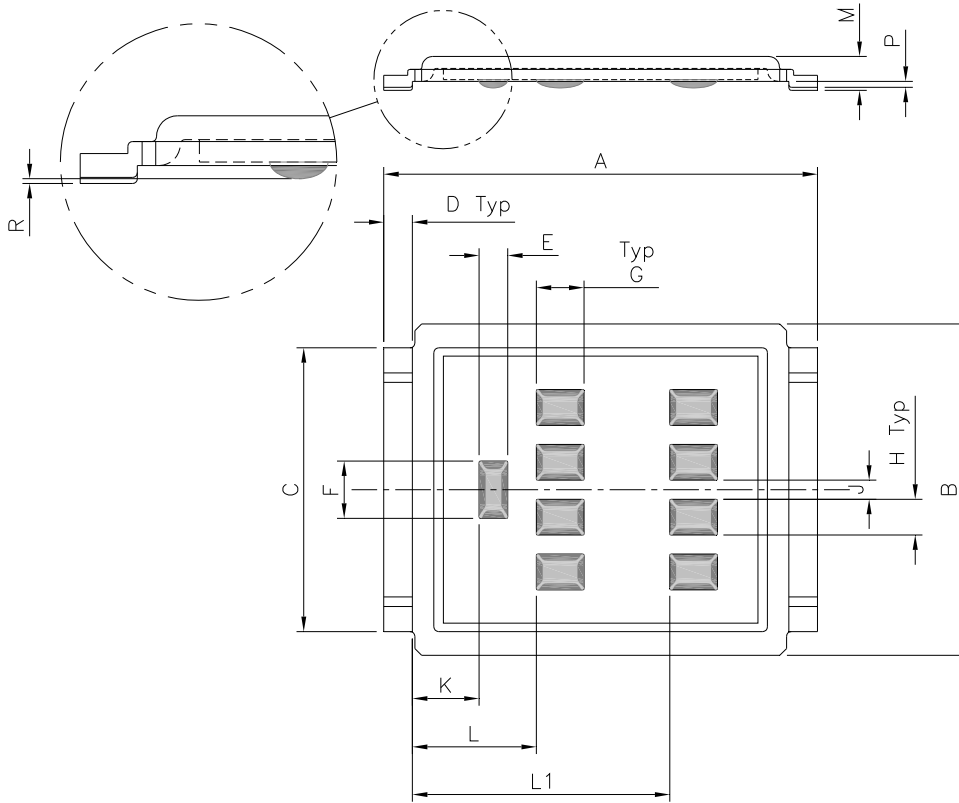
Please see DirectFET™ application note [AN-1035](#) for all details regarding the assembly of DirectFET™. This includes all recommendations for stencil and substrate designs.



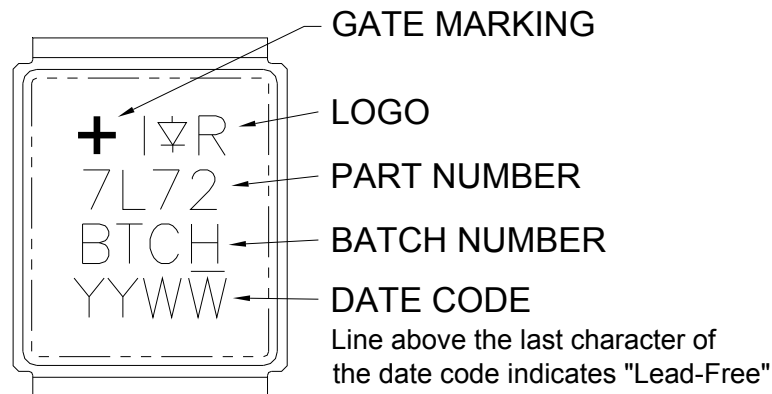
Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

**DirectFET™ Outline Dimension, L8 Outline
(Large Size Can, 8-Source Pads)**

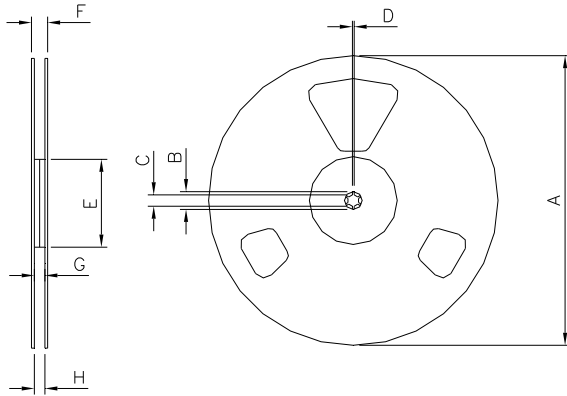
Please see DirectFET™ application note [AN-1035](#) for all details regarding the assembly of DirectFET™. This includes all recommendations for stencil and substrate designs.



| CODE | METRIC | | IMPERIAL | |
|------|--------|------|----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.05 | 9.15 | 0.356 | 0.360 |
| B | 6.85 | 7.10 | 0.270 | 0.280 |
| C | 5.90 | 6.00 | 0.232 | 0.236 |
| D | 0.55 | 0.65 | 0.022 | 0.026 |
| E | 0.58 | 0.62 | 0.023 | 0.024 |
| F | 1.18 | 1.22 | 0.046 | 0.048 |
| G | 0.98 | 1.02 | 0.039 | 0.040 |
| H | 0.73 | 0.77 | 0.029 | 0.030 |
| J | 0.38 | 0.42 | 0.015 | 0.017 |
| K | 1.35 | 1.45 | 0.053 | 0.057 |
| L | 2.55 | 2.65 | 0.100 | 0.104 |
| L1 | 5.35 | 5.45 | 0.211 | 0.215 |
| M | 0.68 | 0.74 | 0.027 | 0.029 |
| P | 0.09 | 0.17 | 0.003 | 0.007 |
| R | 0.02 | 0.08 | 0.001 | 0.003 |

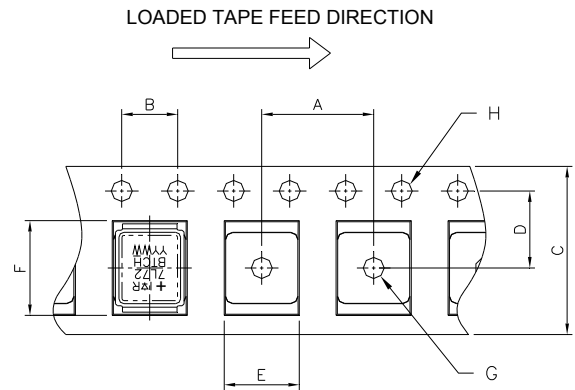
DirectFET™ Part Marking


Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

DirectFET™ Tape & Reel Dimension (Showing component orientation).


NOTE: Controlling dimensions in mm
Std reel quantity is 4000 parts. Order as IRL7472L1TRPbF).

| REEL DIMENSIONS | | | | |
|----------------------------|--------|--------|----------|-------|
| STANDARD OPTION (QTY 4000) | | | | |
| CODE | METRIC | | IMPERIAL | |
| | MIN | MAX | MIN | MAX |
| A | 330.00 | N.C | 12.992 | N.C |
| B | 20.20 | N.C | 0.795 | N.C |
| C | 12.80 | 13.20 | 0.504 | 0.520 |
| D | 1.50 | N.C | 0.059 | N.C |
| E | 99.00 | 100.00 | 3.900 | 3.940 |
| F | N.C | 22.40 | N.C | 0.880 |
| G | 16.40 | 18.40 | 0.650 | 0.720 |
| H | 15.90 | 19.40 | 0.630 | 0.760 |



NOTE: CONTROLLING DIMENSIONS IN MM

| CODE | DIMENSIONS | | | |
|------|------------|-------|----------|-------|
| | METRIC | | IMPERIAL | |
| | MIN | MAX | MIN | MAX |
| A | 11.90 | 12.10 | 4.69 | 0.476 |
| B | 3.90 | 4.10 | 0.154 | 0.161 |
| C | 15.90 | 16.30 | 0.623 | 0.642 |
| D | 7.40 | 7.60 | 0.291 | 0.299 |
| E | 7.20 | 7.40 | 0.283 | 0.291 |
| F | 9.90 | 10.10 | 0.390 | 0.398 |
| G | 1.50 | N.C | 0.059 | N.C |
| H | 1.50 | 1.60 | 0.059 | 0.063 |

Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

Qualification Information

| | | |
|-----------------------------------|---|--|
| Qualification Level | Industrial * (per JEDEC JESD47F [†] guidelines) | |
| Moisture Sensitivity Level | DirectFET (Large -Can) | MSL1 (per JEDEC J-STD-020D [†]) |
| RoHS Compliant | Yes | |

[†] Applicable version of JEDEC standard at the time of product release.

* Industrial qualification standards except autoclave test conditions.

Revision History

| Date | Comments |
|------------|--|
| 08/09/2016 | <ul style="list-style-type: none"> • Changed datasheet with Infineon logo - all pages. • Changed max Rdson @ 10V/4.5V from “0.59mΩ /0.97mΩ” to “0.45mΩ” / 0.7mΩ” - on pages 1 & 2. • Changed ID @ TC 25C/100C from “564A/399A” to “645A/456A” - on pages 1 & 2. • Changed ID @ TA 25C from “59A” to “68A” - on pages 1 & 2. • Changed Fig.2 -on page 2. |
| 10/14/2016 | <ul style="list-style-type: none"> • Corrected Outline Dimension, L8 Outline on page 10. |

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