Ultra Low Quiescent Current Linear Voltage Regulator

TLS810A1

TLS810A1LDV50

Linear Voltage Regulator

Data Sheet

Rev. 1.0, 2016-03-15

Automotive Power

1 Overview

Features

- Ultra Low Quiescent Current of 5 µA
- Wide Input Voltage Range of 2.75 V to 42 V
- Output Current Capacity up to 100 mA
- Low Drop Out Voltage of typ. 200 mV @ 100 mA
- Output Current Limit Protection
- Overtemperature Shutdown
- Available in PG-TSON-10 Package
- Wide Temperature Range
- Green Product (RoHS Compliant)
- AEC Qualified

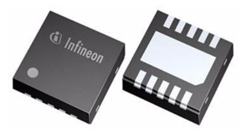


Figure 1 PG-TSON-10

Type	Package	Marking
TLS810A1LDV50	PG-TSON-10	810A1V5

Description

The TLS810A1 is a linear voltage regulator featuring wide input voltage range, low drop out voltage and ultra low quiescent current.

With an input voltage range of 2.75 V to 42 V and ultra low quiescent of only 5 µA, the regulator is perfectly suitable for automotive or any other supply systems connected permanently to the battery.

The TLS810A1LDV50 is the fixed 5 V output version with an accuracy of 2 % and output current capability up to 100 mA.

The new regulation concept implemented in TLS810A1 combines fast regulation and very good stability while requiring only a small ceramic capacitor of 1 µF at the output.

The tracking region starts already at input voltages of 2.75 V (extended operating range). This makes the TLS810A1 also suitable to supply automotive systems that need to operate during cranking condition.

Internal protection features like output current limitation and overtemperature shutdown are implemented to protect the device against immediate damage due to failures like output short circuit to GND, over-current and over-temperature.

Choosing External Components

An input capacitor C_I is recommended to compensate line influences. The output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values $C_Q \geq 1$ µF and an ESR ≤ 100 Ω within the whole operating range.

2 Block Diagram

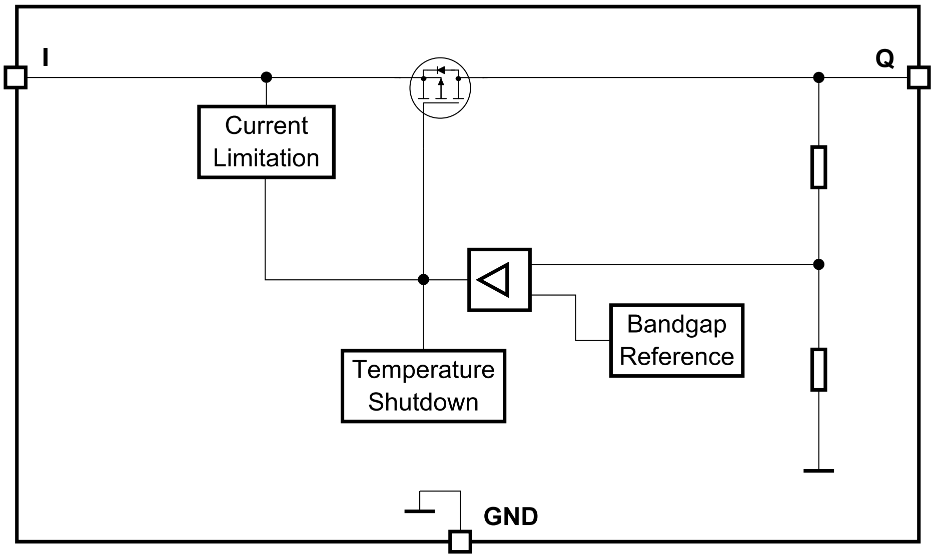


Figure 2 Block Diagram TLS810A1

3 Pin Configuration

3.1 Pin Assignment in PG-TSON-10 Package

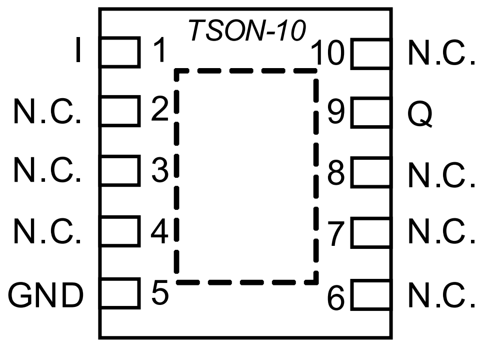


Figure 3 Pin Configuration TLS805A1TLS810A1 in PG-TSON-10 package

3.2 Pin Definitions and Functions in PG-TSON-10 Package

Pin	Symbol	Function
1	I	**Input** It is recommended to place a small ceramic capacitor (e.g. 100 nF) to GND, close to the IC terminals, in order to compensate line influences.
2	N.C.	**Not connected**
3	N.C.	**Not connected**
4	N.C.	**Not connected**
5	GND	**Ground**
6	N.C.	**Not connected**
7	N.C.	**Not connected**
8	N.C.	**Not connected**
9	Q	**Output** Connect an output capacitor C_Q to GND close to the IC's terminals, respecting the values specified for its capacitance and ESR in **Table 2 "Functional Range" on Page 8**.

Pin	Symbol	Function
10	N.C.	**Not connected**
Pad	–	**Exposed Pad** Connect to heatsink area. Connect to GND.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage Input I							
Voltage	V_I	-0.3	–	45	V	–	P_4.1.1
Voltage Output Q							
Voltage	V_Q	-0.3	–	7	V	–	P_4.1.2
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.3
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.4
ESD Absorption							
ESD Susceptibility to GND	$V_{ESD,HBM}$	-2	–	2	kV	HBM[2)]	P_4.1.5
ESD Susceptibility to GND	$V_{ESD,CDM}$	-750	–	750	V	CDM[3)] at all pins	P_4.1.6

1) Not subject to production testing, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage Range	V_I	$V_{Q,nom}+V_{dr}$	–	42	V	–[1)]	P_4.2.1
Extended Input Voltage Range	$V_{I,ext}$	2.75	–	42	V	–[2)]	P_4.2.2
Output Capacitor	C_Q	1	–	–	µF	–[3)4)]	P_4.2.3
Output Capacitor's ESR	ESR(C_Q)	–	–	100	Ω	–[4)]	P_4.2.4
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.5

1) Output current is limited internally and depends on the input voltage, see Electrical Characteristics for more details.
2) When V_I is between $V_{I,ext.min}$ and $V_{Q,nom}$ + V_{dr}, $V_Q = V_I - V_{dr}$. When V_I is below $V_{I,ext,min}$, V_Q can drop down to 0 V.
3) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
4) Not subject to production testing, specified by design.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 3 Thermal Resistance TLS810A1 in PG-TSON-10 Package

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Package Version							
Junction to Case[1)]	R_{thJC}	–	13	–	K/W	–	P_4.3.1
Junction to Ambient[1)]	R_{thJA}	–	60	–	K/W	2s2p board[2)]	P_4.3.2
Junction to Ambient[1)]	R_{thJA}	–	184	–	K/W	1s0p board, footprint only[3)]	P_4.3.3
Junction to Ambient[1)]	R_{thJA}	–	75	–	K/W	1s0p board, 300 mm^2 heatsink area on PCB[3)]	P_4.3.4
Junction to Ambient[1)]	R_{thJA}	–	64	–	K/W	1s0p board, 600 mm^2 heatsink area on PCB[3)]	P_4.3.5

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

5 Block Description and Electrical Characteristics

5.1 Voltage Regulation

The output voltage V_Q is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and the pass transistor is driven accordingly.

The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the internal circuit structure. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in **"Functional Range" on Page 8** have to be maintained. For details see the typical performance graph **Output Capacitor Series Resistor ESR(C_Q) versus Output Current I_Q**. Since the output capacitor is used to buffer load steps, it should be sized according to the application's needs.

An input capacitor C_I is not required for stability, but is recommended to compensate line fluctuations. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used, in case the input is connected directly to the battery line. Connect the capacitors close to the regulator terminals.

In order to prevent overshoots during start-up, a smooth ramping up function is implemented. This ensures almost no overshoots during start-up, mostly independent from load and output capacitance.

Whenever the load current exceeds the specified limit, e.g. in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuit) by switching off the power stage. After the chip has cooled down, the regulator restarts. This oscillatory thermal behaviour causes the junction temperature to exceed the maximum rating of 150°C and can significantly reduce the IC's lifetime.

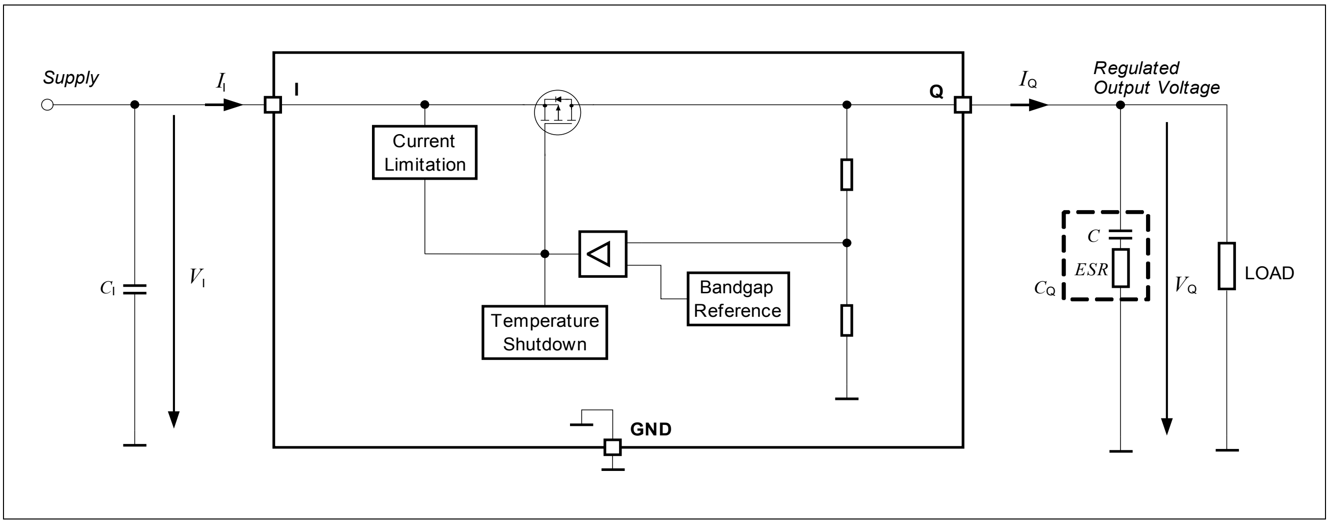


Figure 4 Block Diagram Voltage Regulation

Table 4 Electrical Characteristics

T_j = -40 °C to +150 °C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified).
Typical values are given at T_j = 25 °C, V_I = 13.5 V.

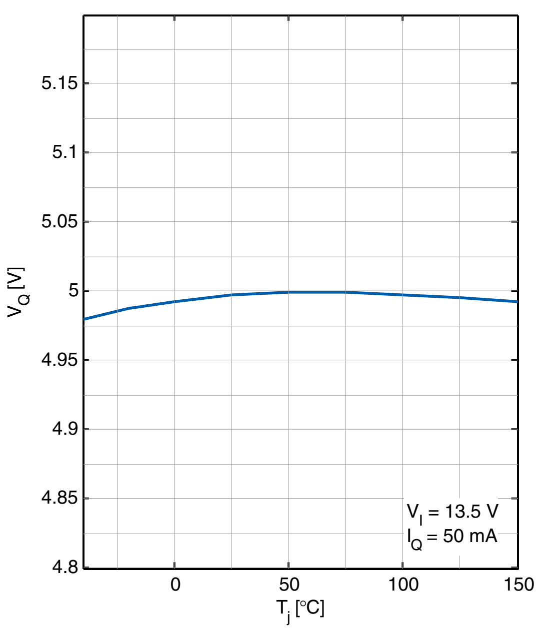
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage Precision	V_Q	4.90	5.00	5.10	V	50 µA ≤ I_Q ≤ 100 mA, 5.7 V ≤ V_I ≤ 28 V	P_5.1.1
Output Voltage Precision	V_Q	4.90	5.00	5.10	V	50 µA ≤ I_Q ≤ 50 mA, 5.7 V ≤ V_I ≤ 42 V	P_5.1.2
Output Current Limitation	$I_{Q,lim}$	110	190	260	mA	0 V ≤ V_Q ≤ $V_{Q,nom}$ - 0.1 V	P_5.1.3
Line Regulation steady-state	$\Delta V_{Q,line}$	–	1	20	mV	I_Q = 1 mA, 6 V ≤ V_I ≤ 32 V	P_5.1.4
Load Regulation steady-state	$\Delta V_{Q,load}$	-20	-1	–	mV	V_I = 6 V, 50 µA ≤ I_Q ≤ 100 mA	P_5.1.5
Dropout Voltage[1) $V_{dr} = V_I - V_Q$	V_{dr}	–	200	550	mV	I_Q = 100 mA	P_5.1.6
Ripple Rejection[2)	*PSRR*	–	55	–	dB	I_Q = 50 mA, f_{ripple} = 100 Hz, V_{ripple} = 0.5 V_{p-p}	P_5.1.7
Overtemperature Shutdown Threshold[2)	$T_{j,sd}$	151	175	–	°C	T_j increasing	P_5.1.8
Overtemperature Shutdown Threshold Hysteresis[2)	$T_{j,sdh}$	–	10	–	K	T_j decreasing	P_5.1.9

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5V
2) Not subject to production test, specified by design

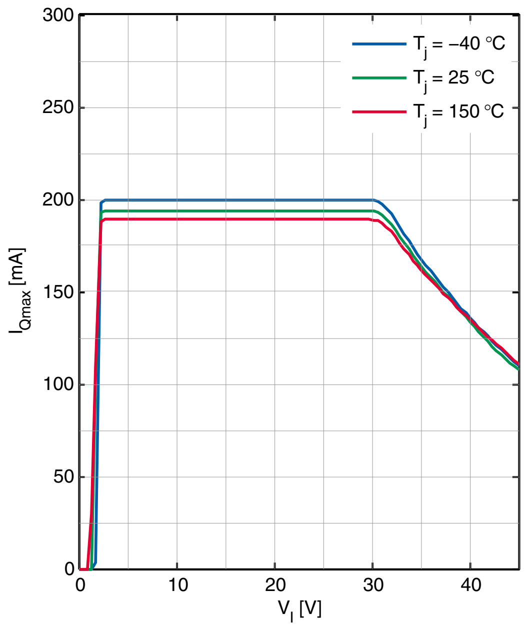
5.2 Typical Performance Characteristics Voltage Regulation

Typical Performance Characteristics

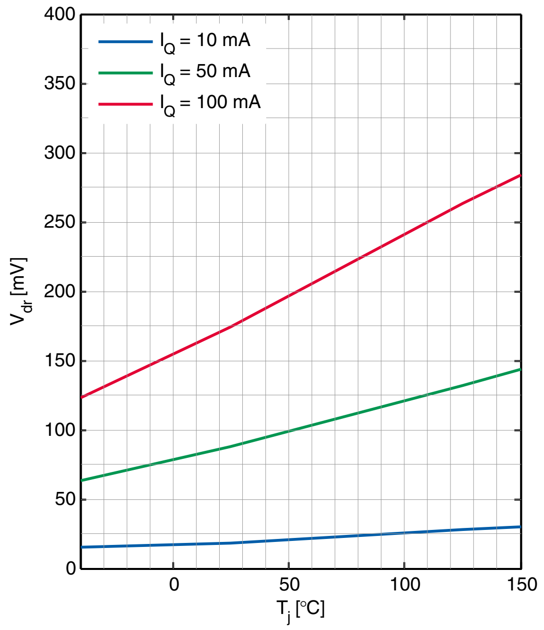
Output Voltage V_Q versus Junction Temperature T_j



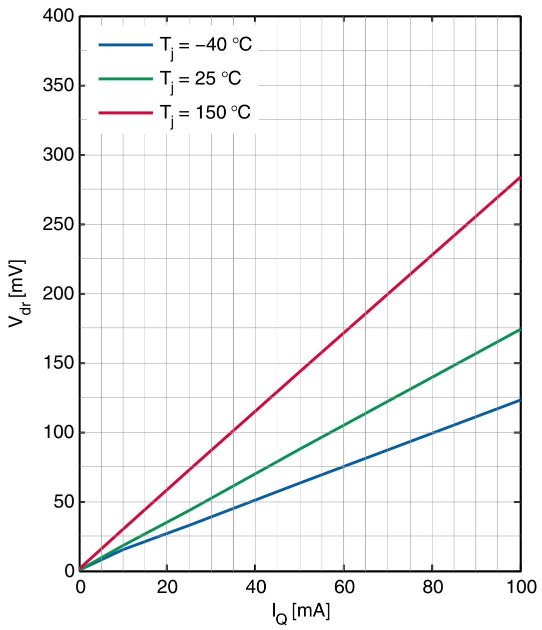
Output Current I_Q versus Input Voltage V_I



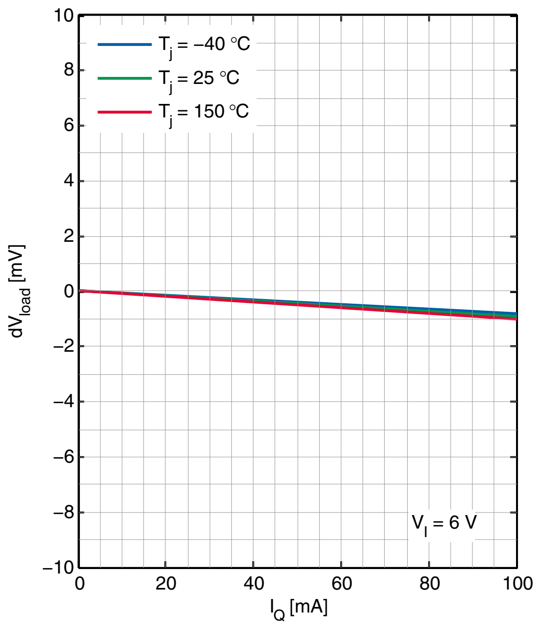
Dropout Voltage V_{dr} versus Junction Temperature T_j



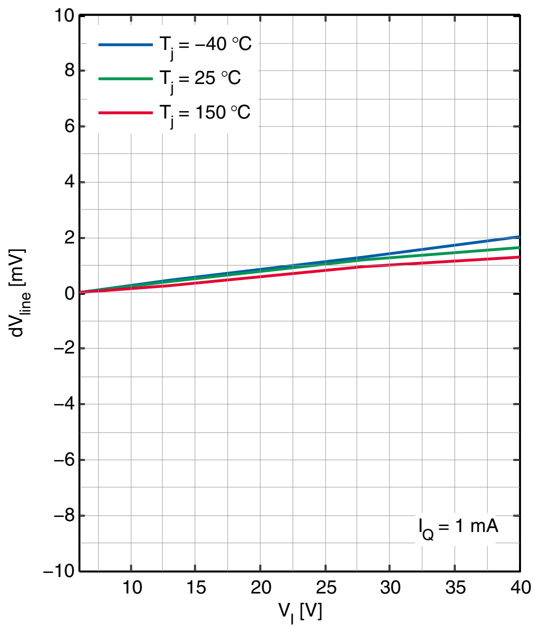
Dropout Voltage V_{dr} versus Output Current I_Q



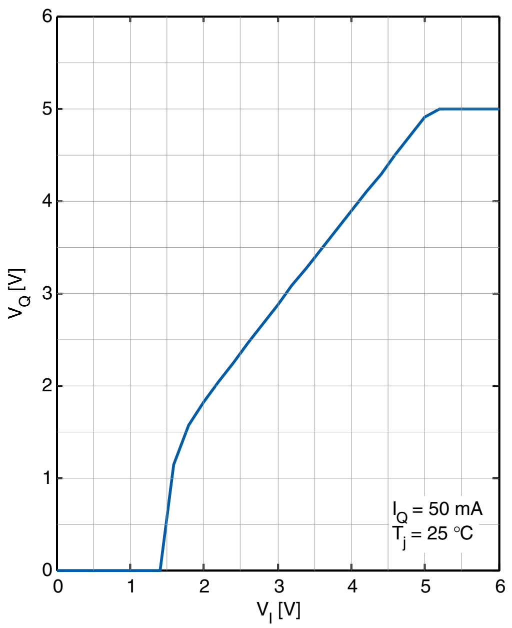
Load Regulation $\Delta V_{Q,load}$ versus Output Current I_Q



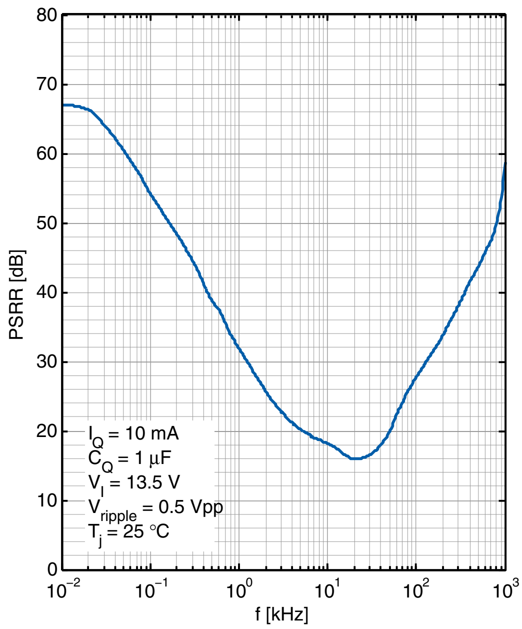
Line Regulation $\Delta V_{Q,line}$ versus Input Voltage V_I



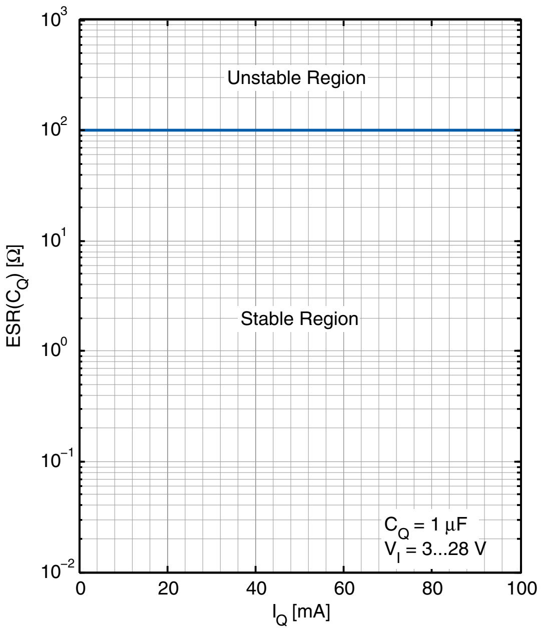
Output Voltage V_Q versus Input Voltage V_I



Power Supply Ripple Rejection *PSRR* versus Ripple Frequency f_r



Output Capacitor Series Resistor *ESR*(C_Q) versus Output Current I_Q



5.3 Current Consumption

Table 5 Electrical Characteristics Current Consumption

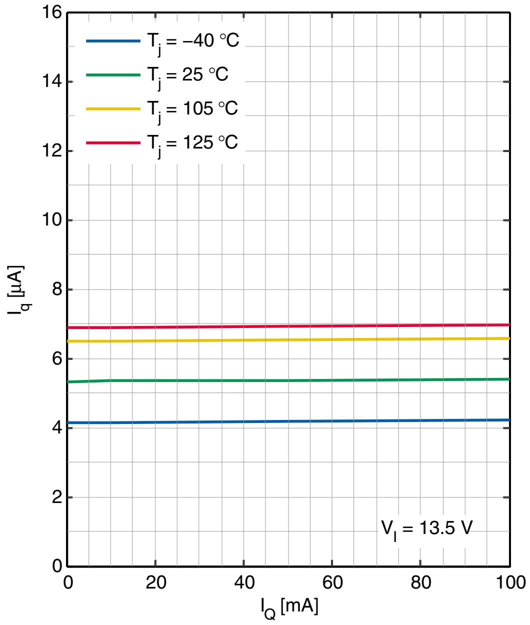
T_j = -40 °C to +150 °C, V_I = 13.5 V (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption $I_q = I_I - I_Q$	I_q	–	5	7.5	µA	I_Q = 50 µA, T_j = 25 °C	P_5.2.1
Current Consumption $I_q = I_I - I_Q$	I_q	–	6.5	10	µA	I_Q = 50 µA, T_j < 105 °C	P_5.2.2
Current Consumption $I_q = I_I - I_Q$	I_q	–	7	11	µA	I_Q = 50 µA, T_j < 125 °C	P_5.2.3
Current Consumption $I_q = I_I - I_Q$	I_q	–	7	11	µA	I_Q= 100 mA, T_j < 125 °C	P_5.2.4

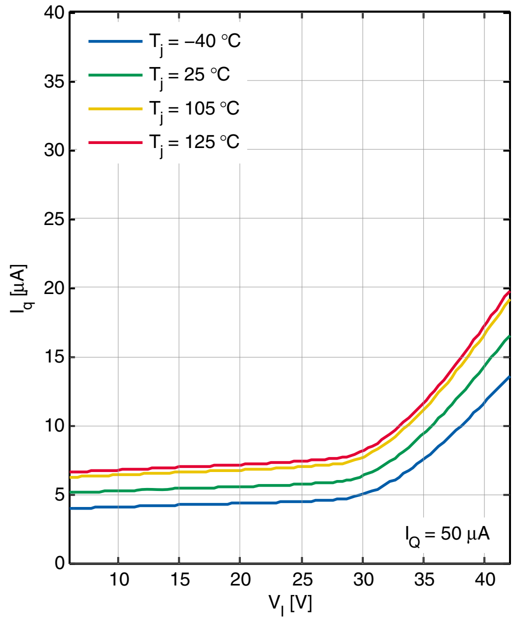
5.4 Typical Performance Characteristics Current Consumption

Typical Performance Characteristics

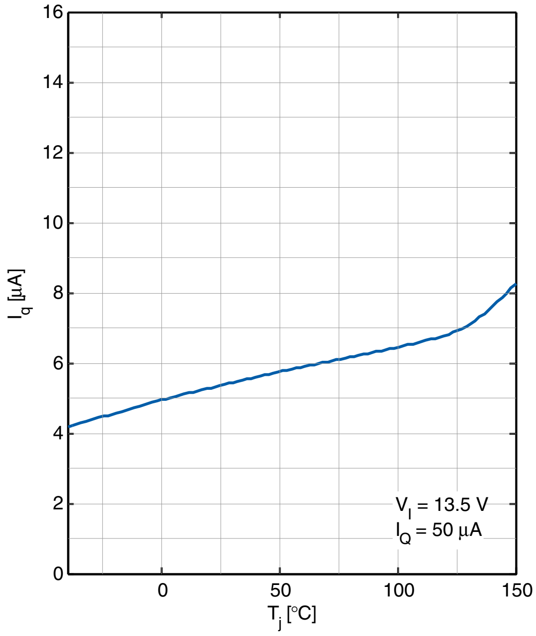
Current Consumption I_q versus Output Current I_Q



Current Consumption I_q versus Input Voltage V_I



Current Consumption I_q versus Junction Temperature T_j



6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

6.1 Application Diagram

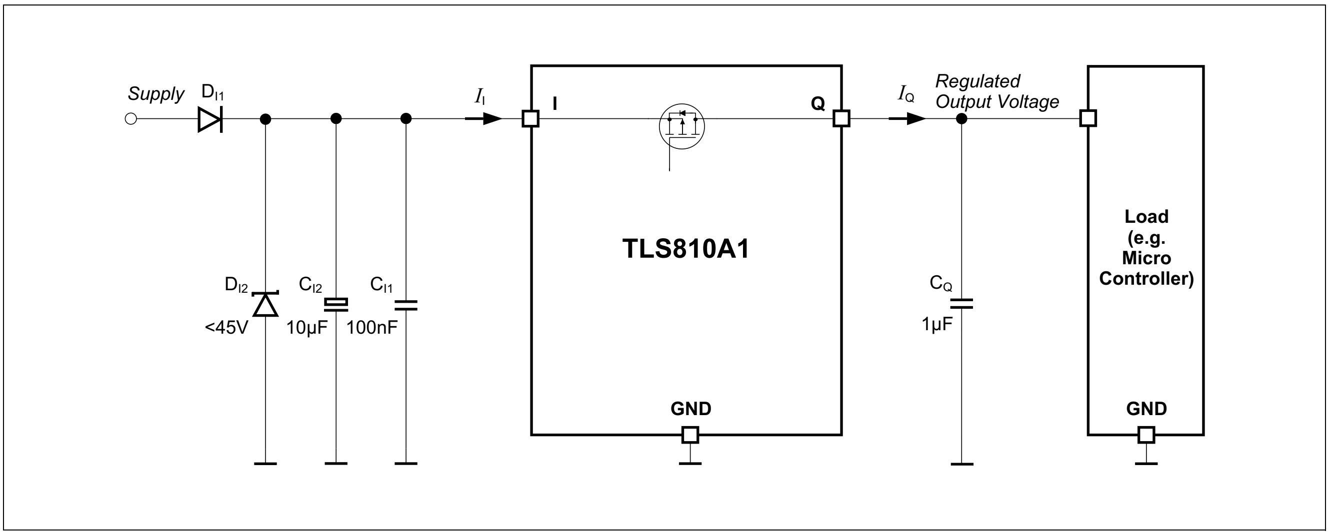


Figure 5 Application Diagram

6.2 Selection of External Components

6.2.1 Input Pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

6.2.2 Output Pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **"Functional Range" on Page 8**. The graph **"Output Capacitor Series Resistor ESR(C_Q) versus Output Current I_Q" on Page 14** shows the stable operation range of the device.

TLS810A1 is designed to be stable with extremely low ESR capacitors. According to the automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

6.3 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \tag{6.1}$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,\,max} = \frac{T_{j,\,max} - T_a}{P_D} \tag{6.2}$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **"Thermal Resistance" on Page 9**.

Example

Application conditions:

V_I = 13.5 V

V_Q = 5 V

I_Q = 80 mA

T_a = 105 °C

Calculation of $R_{thJA,max}$:

$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$

$= (13.5V - 5V) \times 80\ mA + 13.5\ V \times 0.016\ mA$

$= 0.68\ W$

$R_{thJA,max} = (T_{j,max} - T_a) / P_D$

$= (150\ °C - 105\ °C) / 0.68\ W$

$= 66.2\ K/W$

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 66.2 K/W. According to **"Thermal Resistance" on Page 9**, at least 600 mm^2 heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

6.4 Reverse Polarity Protection

TLS810A1 is not self protected against reverse polarity faults. To protect the device against negative supply voltage, an external reverse polarity diode is needed, as shown in **Figure 5**. The absolute maximum ratings of the device as specified in **"Absolute Maximum Ratings" on Page 7** must be kept.

6.5 Further Application Information

- For further information you may contact **http://www.infineon.com/**

7 Package Outlines

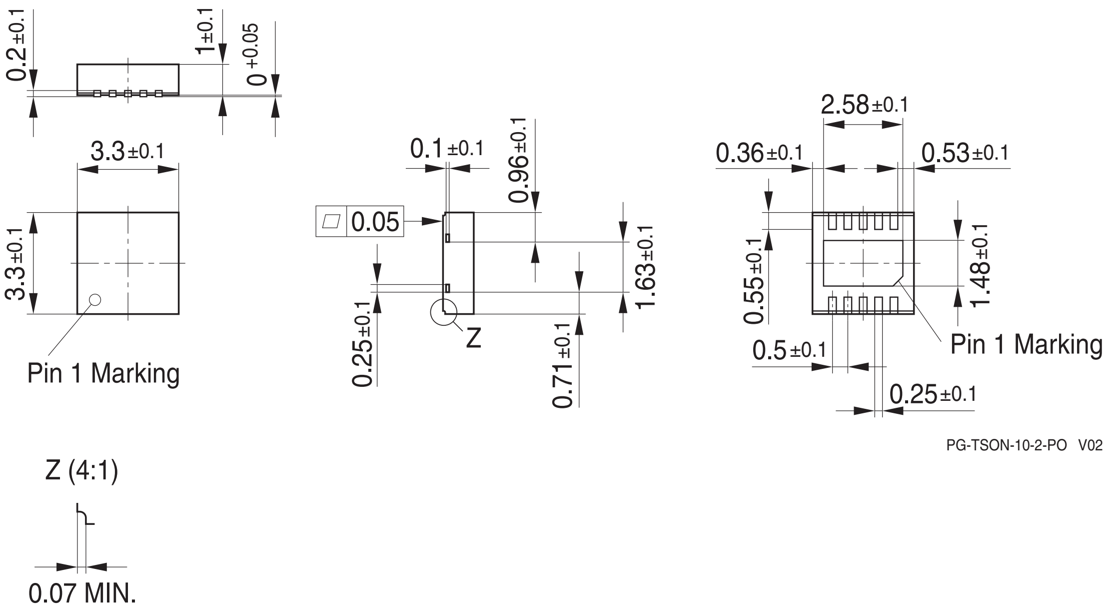


Figure 6 **PG-TSON-10**

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision History

Revision	Date	Changes
1.0	2016-03-15	Datasheet - Initial version

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