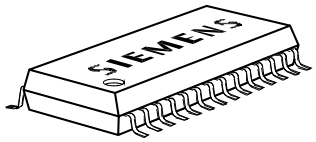
Data Sheet

1 Overview



P-DSO-28-14

1.1 Features

- Quad D-MOS switch driver
- Free configurable as bridge or quad-switch
- Optimized for DC motor management applications
- Low $R_{DS\,ON}$: 110 mΩ high-side switch, 90 mΩ low-side switch (typical values @ 25 °C)
- Maximum peak current: typ. 9 A @ 25 °C
- Very low quiescent current: typ. 5 µA @ 25 °C
- Small outline, enhanced power P-DSO-package
- Load and GND-short-circuit-protection
- Operates up to 40 V
- Status flag diagnosis
- Overtemperature shut down with hysteresis
- Internal clamp diodes
- Isolated sources for external current sensing
- Under-voltage detection with hysteresis
- PWM frequencies up to 50 kHz

Type	Ordering Code	Package
BTS 7700 G	Q67007-A9375	P-DSO-28-14

1.2 Description

The **BTS 7700 G** is part of the **TrilithIC** family containing three dies in one package: One double high-side switch and two low-side switches. The drains of these three vertical DMOS chips are mounted on separated leadframes. The sources are connected to individual pins, so the **BTS 7700 G** can be used in H-bridge- as well as in any other configuration. The double high-side is manufactured in **SMART SIPMOS**® technology which combines low $R_{DS\,ON}$ vertical DMOS power stages with CMOS control circuitry. The high-side switch is fully protected and contains the control and diagnosis circuitry. To achieve low $R_{DS\,ON}$ and fast switching performance, the low-side switches are manufactured in **S-FET** logic level technology. The equivalent standard product is the **BUZ 104 SL**.

In contrast to the **BTS 7710 G**, which consists of lower ohmic chips in the same package, the **BTS 7700 G** offers a lower price for applications, which do not need the high current capability of the **BTS 7710 G** or **BTS 7710 GP**.

1.3 Pin Configuration
(top view)

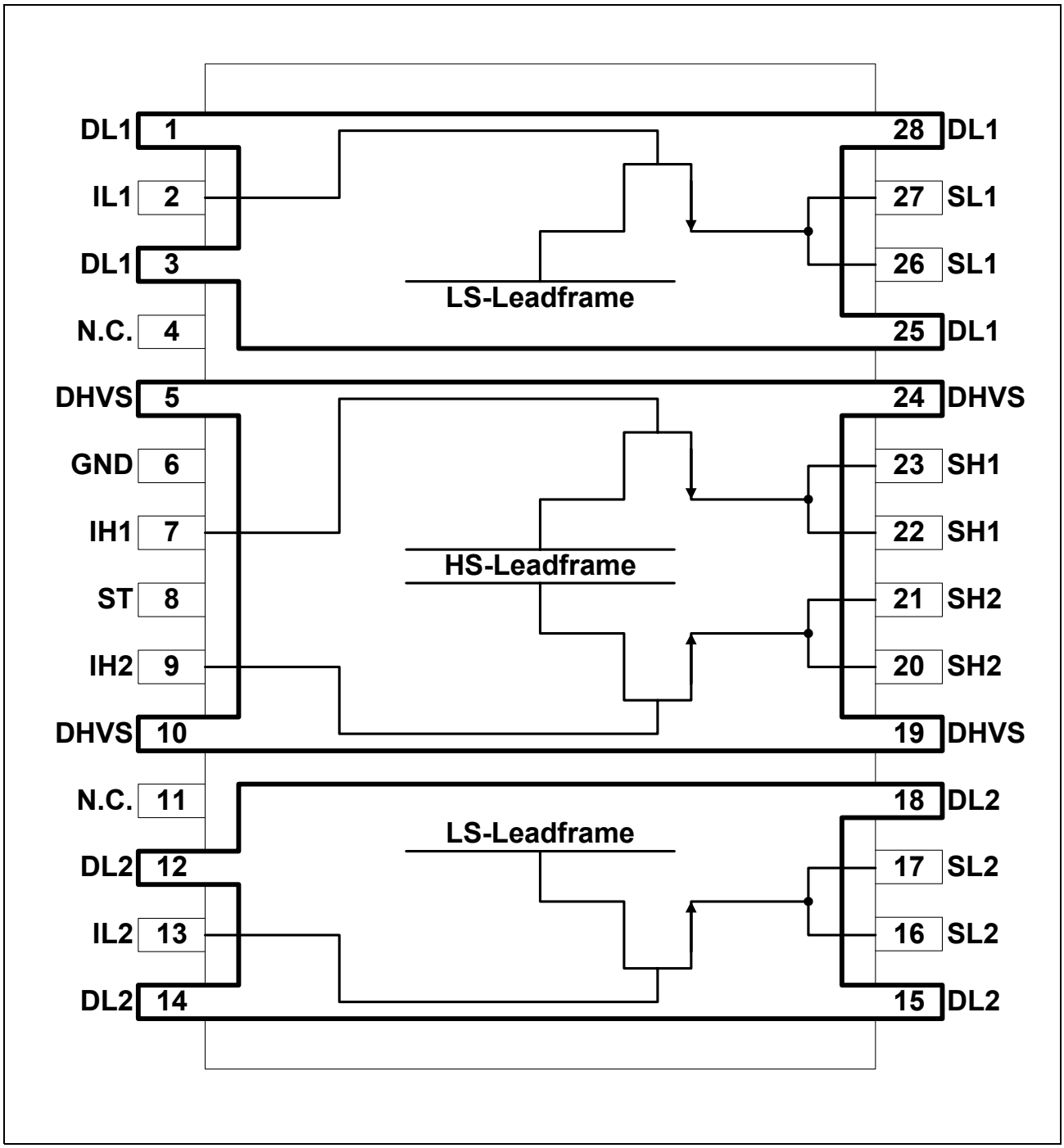


Figure 1

1.4 Pin Definitions and Functions

Pin No.	Symbol	Function
1, 3, 25, 28	**DL1**	**Drain of low-side switch1, leadframe 1** [1)]
2	IL1	Analog input of low-side switch1
4	N.C.	not connected
5, 10, 19, 24	**DHVS**	**Drain of high-side switches and power supply voltage, leadframe 2** [1)]
6	GND	Ground
7	IH1	Digital input of high-side switch1
8	ST	Status of high-side switches; open Drain output
9	IH2	Digital input of high-side switch2
11	N.C.	not connected
12, 14, 15, 18	**DL2**	**Drain of low-side switch2, leadframe 3** [1)]
13	IL2	Analog input of low-side switch2
16,17	**SL2**	**Source of low-side switch2**
20,21	**SH2**	**Source of high-side switch2**
22,23	**SH1**	**Source of high-side switch1**
26,27	**SL1**	**Source of low-side switch1**

[1)] To reduce the thermal resistance these pins are direct connected via metal bridges to the leadframe.

Pins written in **bold type** need power wiring.

1.5 Functional Block Diagram

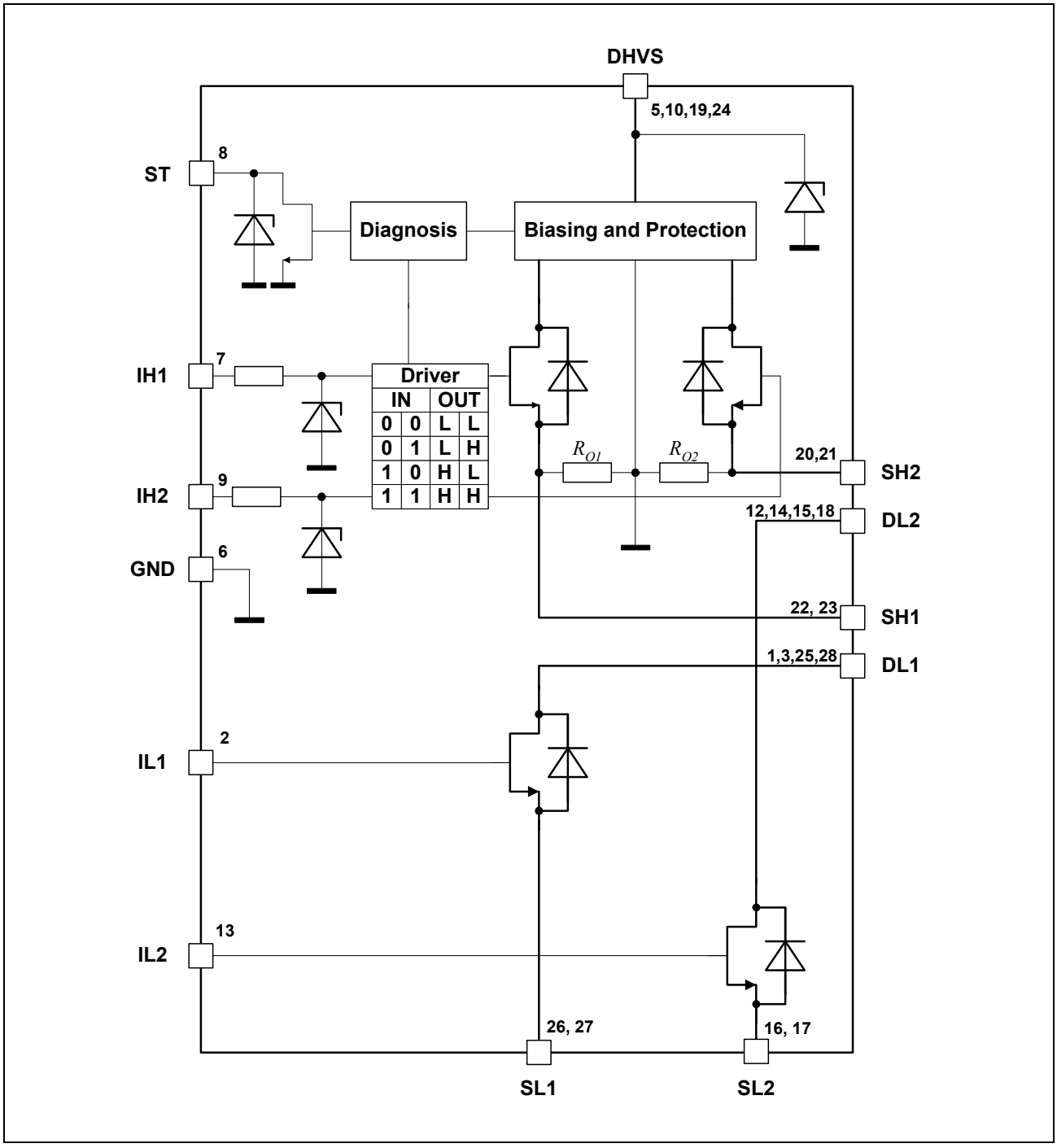


Figure 2
Block Diagram

1.6 Circuit Description

Input Circuit

The control inputs IH1,2 consist of TTL/CMOS compatible Schmitt-Triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages. The inputs are protected by ESD clamp-diodes.

The inputs IL1 and IL2 are connected to the gates of the standard N-channel vertical power-MOS-FETs.

Output Stages

The output stages consist of an low $R_{DS\ ON}$ Power-MOS H-bridge. In H-bridge configuration, the D-MOS body diodes can be used for freewheeling when commutating inductive loads. If the high-side switches are used as single switches, positive and negative voltage spikes which occur when driving inductive loads are limited by integrated power clamp diodes.

Short Circuit Protection

The outputs are protected against

– output short circuit to ground
– overload (load short circuit).

An internal OP-Amp controls the Drain-Source-Voltage by comparing the DS-Voltage-Drop with an internal reference voltage. Above this trippoint the OP-Amp reduces the output current depending on the junction temperature and the drop voltage.

In the case of overloaded high-side switches the status output is set to low.

Overtemperature Protection

The high-side switches incorporate an overtemperature protection circuit with hysteresis which switches off the output transistors and sets the status output to low.

Undervoltage-Lockout (UVLO)

When V_S reaches the switch-on voltage V_{UVON} the IC becomes active with a hysteresis. The High-Side output transistors are switched off if the supply voltage V_S drops below the switch off value $V_{UVOFF.}$

Status Flag

The status flag output is an open drain output with Zener-diode which requires a pull-up resistor, c.f. the application circuit on page 14. Various errors as listed in the table “Diagnosis” are detected by switching the open drain output ST to low. A open load detection is not available. Freewheeling condition does not cause an error.

2 Truthtable and Diagnosis (valid only for the High-Side-Switches)

Flag	IH1	IH2	SH1	SH2	ST	Remarks
	Inputs		Outputs			
Normal operation; identical with functional truth table	0 0 1 1	0 1 0 1	L L H H	L H L H	1 1 1 1	stand-by mode switch2 active switch1 active both switches active
Overtemperature high-side switch1	0 1	X X	L L	X X	1 0	 detected
Overtemperature high-side switch2	X X	0 1	X X	L L	1 0	 detected
Overtemperature both high-side switches	0 X 1	0 1 X	L L L	L L L	1 0 0	 detected detected
Undervoltage	X	X	L	L	1	not detected

Inputs:
0 = Logic LOW
1 = Logic HIGH
X = don’t care

Outputs:
Z = Output in tristate condition
L = Output in sink condition
H = Output in source condition
X = Voltage level undefined

Status:
1 = No error
0 = Error

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

– 40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
High-Side-Switches (Pins DHVS, IH1,2 and SH1,2)					
Supply voltage	V_S	– 0.3	42	V	–
Supply voltage for full short circuit protection	$V_{S(SCP)}$		28	V	–
HS-drain current*	I_S	– 7	**	A	T_A = 25°C; t < 100 ms
HS-input current	I_{IH}	– 5	5	mA	Pin IH1 and IH2
HS-input voltage	V_{IH}	– 10	16	V	Pin IH1 and IH2
*Note: * single pulse ** internally limited*					
Status Output ST					
Status pull up voltage	V_{ST}	– 0.3	5.4	V	–
Status Output current	I_{ST}	– 5	5	mA	Pin ST
Low-Side-Switches (Pins DL1,2, IL1,2 and SL1,2)					
Drain- source break down voltage	V_{DSL}	55	–	V	V_{IL} = 0 V; I_D ≤ 1 mA
LS-drain current* T_A = 25°C	I_{DL}	–7	6	A	t < 100 ms
		–	8	A	t < 10 ms
		–	18	A	t < 1 ms
LS-input voltage	V_{IL}	– 20	20	V	Pin IL1 and IL2
*Note: * single pulse*					
Temperatures					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 55	150	°C	–

3.1 Absolute Maximum Ratings (cont'd)

– 40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Thermal Resistances (one HS-LS-Path active)					
LS-junction case	$R_{thjC\ L}$	–	20	K/W	measured to pin 3 or 12
HS-junction case	$R_{thjC\ H}$	–	20	K/W	measured to pin 19
Junction ambient $R_{thja} = T_{j(HS)}/(P_{(HS)}+P_{(LS)})$	R_{thja}	–	60	K/W	device soldered to reference PCB with 6 cm² cooling area
ESD Protection (Human Body Model acc. MIL STD 883D, method 3015.7 and EOS/ ESD assn. standard S5.1 - 1993)					
Input LS-Switch	V_{ESD}	–	0.5	kV	
Input HS-Switch	V_{ESD}	–	1	kV	
Status HS-Switch	V_{ESD}	–	2	kV	
Output LS and HS-Switch	V_{ESD}	–	8	kV	all other pins connected to Ground

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

– 40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	V_{UVOFF}	42	V	After V_S rising above V_{UVON}
Input voltages HS	V_{IH}	– 0.3	15	V	–
Input voltages LS	V_{IL}	– 0.3	20	V	–
Output current	I_{ST}	0	2	mA	–
Junction temperature	T_j	– 40	150	°C	–

Note: In the operating range the functions given in the circuit description are fulfilled.

3.3 Electrical Characteristics

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 150 °C; 8 V < V_S < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption HS-switch						
Quiescent current	I_S	–	5	8	µA	IH1 = IH2 = 0 V T_j = 25 °C
		–	–	12	µA	IH1 = IH2 = 0 V
Supply current	I_S	–	1	2	mA	IH1 or IH2 = 5 V V_S = 12 V
		–	2	4	mA	IH1 and IH2 = 5 V V_S = 12 V
Leakage current of highside switch	$I_{SH\ LK}$	–	–	6	µA	$V_{IH} = V_{SH}$ = 0 V
Leakage current through logic GND in free wheeling condition	$I_{LKCL} = I_{FH} + I_{SH}$	–	–	10	mA	I_{FH} = 3 A
Current Consumption LS-switch						
Input current	I_{IL}	–	10	100	nA	V_{IL} = 20 V; V_{DSL} = 0 V T_j = 25 °C
Leakage current of lowside switch	$I_{DL\ LK}$	–	–	10	µA	V_{IL} = 0 V V_{DSL} = 40 V
Under Voltage Lockout (UVLO) HS-switch						
Switch-ON voltage	V_{UVON}	–	–	4.5	V	V_S increasing
Switch-OFF voltage	V_{UVOFF}	1.8	–	3.2	V	V_S decreasing
Switch ON/OFF hysteresis	V_{UVHY}	–	1	–	V	$V_{UVON} - V_{UVOFF}$

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 150 °C; 8 V < V_S < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output stages						
Inverse diode of high-side switch; Forward-voltage	V_{FH}	–	0.8	1.2	V	I_{FH} = 3A
Inverse diode of lowside switch; Forward-voltage	V_{FL}	–	0.8	1.2	V	I_{FL} = 3 A
Static drain-source on-resistance of highside switch	$R_{DS\ ON\ H}$	–	110	140	mΩ	I_{SH} = 1 A T_j = 25 °C
Static drain-source on-resistance of lowside switch	$R_{DS\ ON\ L}$	–	80	110	mΩ	I_{SL} = 1 A; V_{IL} = 5 V T_j = 25 °C
Static path on-resistance	$R_{DS\ ON}$	–	–	480	mΩ	$R_{DS\ ON\ H} + R_{DS\ ON\ L}$ I_{SH} = 1 A;
Short Circuit of highside switch to GND						
Initial peak SC current	$I_{SCP\ H}$	9	11	13	A	T_j = – 40 °C
Initial peak SC current	$I_{SCP\ H}$	7.5	9	11	A	T_j = + 25 °C
Initial peak SC current	$I_{SCP\ H}$	5.5	7	9	A	T_j = + 150 °C
Short Circuit of highside switch to V_S						
Output pull-down-resistor	R_O	12	22	50	kΩ	V_{DSL} = 3 V
Thermal Shutdown						
Thermal shutdown junction temperature	$T_{j\ SD}$	155	180	190	°C	–
Thermal switch-on junction temperature	$T_{j\ SO}$	150	170	180	°C	–
Temperature hysteresis	ΔT	–	10	–	°C	$\Delta T = T_{jSD} - T_{jSO}$

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 150 °C; 8 V < V_S < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Status Flag Output ST of highside switch						
Low output voltage	$V_{ST\,L}$	–	0.2	0.6	V	I_{ST} = 1.6 mA
Leakage current	$I_{ST\,LK}$	–	–	10	µA	V_{ST} = 5 V
Zener-limit-voltage	$V_{ST\,Z}$	5.4		–	V	I_{ST} = 1.6 mA
Switching times of highside switch						
Turn-ON-time; to 90% V_{SH}	t_{ON}	–	75	160	µs	R_{Load} = 12 Ω V_S = 12 V
Turn-OFF-time; to 10% V_{SH}	t_{OFF}	–	60	160	µs	R_{Load} = 12 Ω V_S = 12 V
Slew rate on 10 to 30% V_{SH}	dV/dt_{ON}	–	–	1.7	V/µs	R_{Load} = 12 Ω V_S = 12 V
Slew rate off 70 to 40% V_{SH}	$-dV/dt_{OFF}$	–	–	2.5	V/µs	R_{Load} = 12 Ω V_S = 12 V
Switching times of low-side switch						
Turn-ON delay time; V_{IL} = 5V; R_G = 16Ω	$t_{d\_ON\_L}$	–	7	11	ns	resistive load I_{SL} = 3 A; V_S = 30 V
Switch-ON time; V_{IL}= 5V; R_G = 16Ω	t_{ON_L}	–	28	45	ns	resistive load I_{SL} = 3 A; V_S = 30 V
Switch-OFF delay time; V_{IL}= 5V; R_G = 16Ω	$t_{d\_OFF\_L}$	–	23	35	ns	resistive load I_{SL} = 3 A; V_S = 30 V
Switch-OFF time; V_{IL}= 5V; R_G = 16Ω	t_{OFF_L}	–	18	28	ns	resistive load I_{SL} = 3 A; V_S = 30 V

Note: switching times are guaranteed by design

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 150 °C; 8 V < V_S < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Gate charge of lowside switch						
Input to source charge;	Q_{IS}	–	1.5	2.3	nC	I_{SL} = 3 A; V_S = 14 V
Input to drain charge;	Q_{ID}	–	5	7	nC	I_{SL} = 3 A; V_S = 14 V
Input charge total;	Q_I	–	11	17	nC	I_{SL} = 3 A; V_S = 14 V V_{IL} = 0 to 10 V
Input plateau voltage;	$V_{(plateau)}$	–	3.1	-	V	I_{SL} = 3 A; V_S = 14 V
Note: switching times and input charges are guaranteed by design						
Control Inputs of highside switches IH 1, 2						
H-input voltage	$V_{IH\ High}$	–	–	2.5	V	–
L-input voltage	$V_{IH\ Low}$	1	–	–	V	–
Input voltage hysterese	$V_{IH\ HY}$	–	0.3	–	V	–
H-input current	$I_{IH\ High}$	15	30	60	µA	V_{GH} = 5 V
L-input current	$I_{IH\ Low}$	5	–	20	µA	V_{GH} = 0.4 V
Input series resistance	R_I	2.7	4	5.5	kΩ	–
Zener limit voltage	$V_{IH\ Z}$	5.4	–	–	V	I_{GH} = 1.6 mA
Control Inputs IL1, 2						
Gate-threshold-voltage	$V_{IL\ th}$	0.9	1.7	2.2	V	I_{DL} = 0.5 mA

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

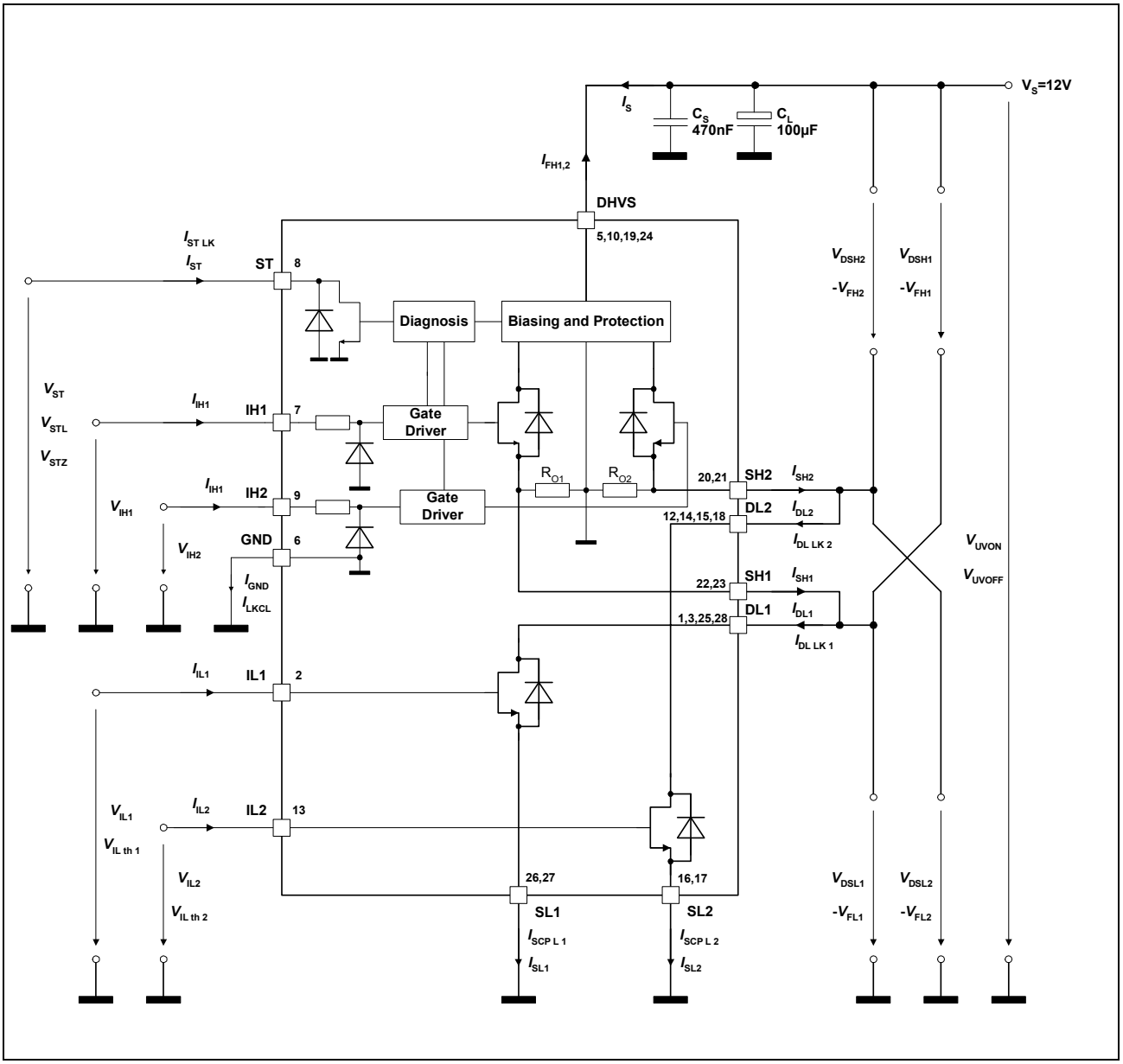


Figure 3
Test Circuit

HS-Source-Current	Named during Short Circuit	Named during Leakage-Cond.
$I_{SH1,2}$	$I_{SCP\ H}$	$I_{DL\ LK}$

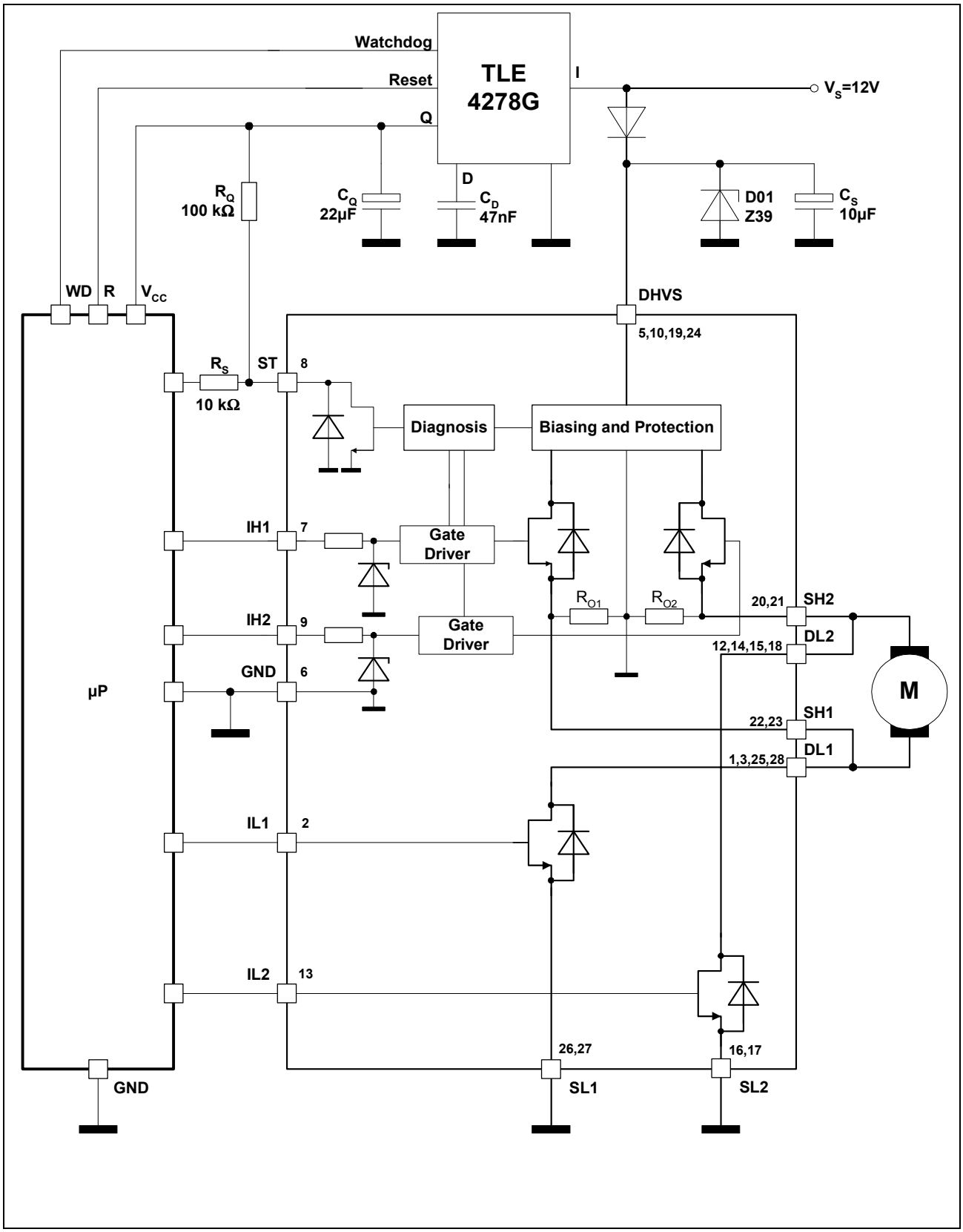
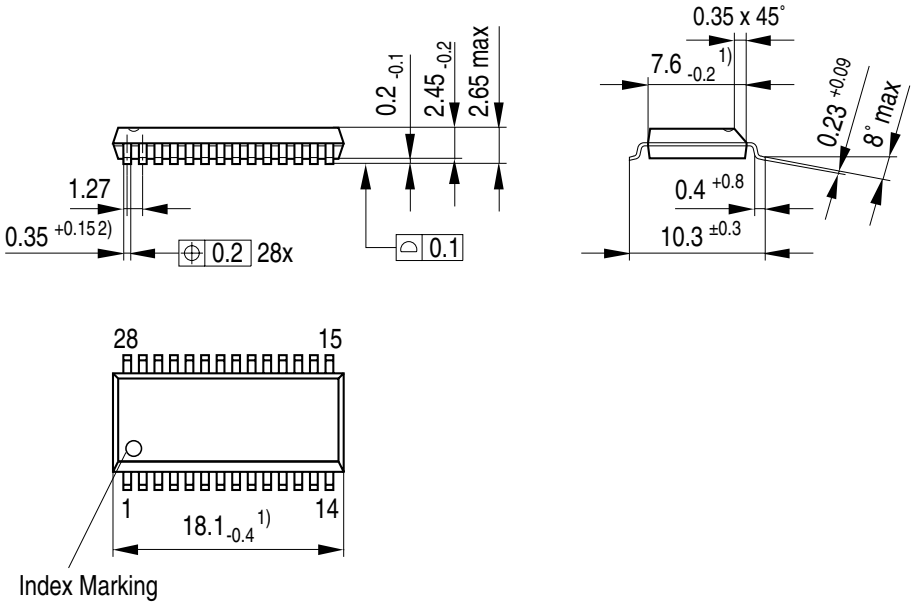


Figure 4
Application Circuit

4 Package Outlines

P-DSO-28-14
(Plastic Transistor Single Outline Package)



1) Does not include plastic or metal protrusions of 0.15 max rer side
2) Does not include dambar protrusion of 0.05 max per side

GPS05123

GPS05123

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Published by
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Bereichs Kommunikation
St.-Martin-Strasse 53,
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